LINEAR TECHNOLOGY

IN THIS ISSUE…

Monolithic Synchronous Step-Down Regulators Pack >500mA Output Current in an MS8 Package

by Jaime Tseng and Gary Shockey

Introduction

The quest to pack more power into portable electronic devices while shrinking their size has placed increased demands on power management products. Not only must they be physically smaller, but they must also retain the power handling capability of their older, larger counterparts. The LTC1877, LTC1878 and LT®1612 are the first of a new generation of monolithic synchronous step-down switching regulators capable of supplying more than 500mA of output current in an MS8 package. Their internal synchronous switches increase efficiency and eliminate the need for external Schottky diodes, saving external components and board space. Optimized for battery-powered applications, the LTC1877 works with a supply range of 2.65V to 10V, the LTC1878 works with supplies of 2.65V to 6V and the LT1612 works with supplies of 2V to 5.5V. This wide operating supply range covered by the two parts allows the use of a single or dual Li-Ion battery or 2- to 6-cell NiCd and NiMH battery packs.

LTC1877/LTC1878 vs LT1612

The LTC1877and LTC1878 are designed in Linear Technology's high performance BiCMOS process and are optimized for ultrahigh efficiency at low load currents. The DC supply currents of both parts are only 10µA while maintaining the output voltage (using Burst Mode™ operation) at no load. This enables both parts to maintain better than 90% efficiency over three decades of output load current. The LT1612, designed in Linear Technology's high speed bipolar process, is optimized for low voltage operation and is a lower cost alternative to the LTC1877/LTC1878. The LT1612 can still regulate the output while supplying 500mA to the load with input supply voltages as low as 2V. The internal frequency is set to 800kHz, compared to 550kHz for the LTC1877. The DC supply current is 150µA. Placing the part in shutdown reduces the current to 1µA.

A Detailed Look at the LTC1877/LTC1878

The LTC1877 and LTC1878 are two nearly identical parts in that they have exactly the same functionality, architecture and pinout. What distinguishes the two parts is their maximum supply voltages: the

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Issue Highlights

Our feature article this issue introduces three new synchronous step-down regulators. The LTC1877/ LTC1878 and LT1612 are new monolithic synchronous step-down switching regulators capable of supplying 500mA of output current in an MS8 package. Their internal synchronous switches increase efficiency and eliminate the need for external Schottky diodes, saving components and board space. Optimized for battery-powered applications, the LTC1877/LTC1878 work with supply ranges of 2.65V to 10V and 2.65V to 6V, respectively, and the LT1612 works with supplies of 2V to 5.5V.

Another power product introduced in this issue is the LT1930. The LT1930 is the only SOT-23 switching regulator in the industry with an integrated 1A switch. The LT1930 uses a constant frequency, internally compensated, current mode PWM architecture. Its 1.2MHz switching frequency allows the use of tiny, low cost capacitors and low profile inductors. With an input voltage range of 2.6V to 16V, the LT1930 is a good fit for a variety of applications. The onboard switch features a low V_{CESAT} voltage of 400mV at 1A, resulting in very good efficiency even at high load currents.

This issue is strong on signal conditioning products, including a number of new op amps, a new instrumentation amp and an RC active lowpass filter.

The LT1677 and the LT1881, LT1882, LT1884 and LT1885 are precision op amps designed for use in low voltage systems. The LT1677 is a rail-to-rail input, rail-to-rail output, single-supply version of the industry-standard LT1007. It features the lowest noise available for a rail-to-rail op amp. Low noise is combined with outstanding precision: the CMRR and PSRR are 130dB, the offset voltage is only 20µV and the open-loop gain is twenty million. The LT1677 is unity-gain stable and has a gain bandwidth product of 7.2MHz.

The LT1881 dual and LT1882 quad op amps feature 150pA input bias currents, whereas the similar LT1884 and LT1885 dual and quad op amps trade slightly higher input bias currents of 500pA for three times higher speed. Their bias current specifications, coupled with 50µV offset voltage, open-loop gains of over one million and high common mode rejection, allows precision accuracy to be maintained in systems with high source impedances.

Another new op amp debuted in this issue is the LT1469, a dual operational amplifier that is optimized for accuracy and speed in 16-bit systems. The amplifier settles in just 900ns to 150µV for a 10V step. The LT1469 also features the excellent DC specifications required for 16-bit designs. Input offset voltage is 125µV maximum, input bias current is 10nA maximum for the inverting input and minimum DC gain is 300V/mV.

LTC's newest instrumentation amplifier, the LT1168, is a low power, single-resistor gain-programmable instrumentation amplifier that is easy to apply. With negligible 60µV (Max) offset voltage and ultrahigh 1TΩ input impedance, it can sense bridges with source impedances from 10Ω to 100k without degrading the signal. Its 120dB CMRR at 60Hz is achieved even with a 1k source impedance imbalance. Matching the LT1168's CMRR using discrete op amps would require the use of 0.001% resistors.

The LTC1563-2 and LTC1563-3 comprise a new family of extremely easy to use, 4th order active RC lowpass filters. Their cutoff frequencies range from 256Hz to 256kHz while operating at supplies from as low as a single 3V up to ±5V. The LTC1563 also features rail-to-rail input and output operation with, typically, 1mV of DC offset. The design of the most popular filter responses is trivial, requiring only six resistors of identical value and no external capacitors.

Our Design Ideas section features an SMBus fan controller for portable

devices, a VID-controlled 42A supply for the AMD Athlon™ processor, the conclusion of the ADSL Line Driver Design Guide, begun in the February issue, and a resistance-measuring circuit using the new LT1168 instrumentation amp. The issue concludes with six New Device Cameos. *LT*

Athlon is a trademark of Advanced Micro Devices, Inc.

LTC in the News...

On April 19th, Linear Technology Corporation announced its financial results for the third quarter of fiscal year 2000. Robert H. Swanson, Chairman and CEO, stated, "The March quarter was an outstanding quarter for us, as we achieved record levels of bookings, sales and profits, with sales increasing 14% and profits 17% sequentially from the December quarter. Our return on sales was a record 41%. Demand from our customers was very robust, escalating during the quarter and increasing in all major geographical areas and all major end markets. Given this robust business activity, we expect the upcoming June quarter to also have continuous sequential sales and profit growth." The Company reported sales of $185,075,000 and net income of $75,867,000 compared with $49,828,000 a year ago. Net sales were up 42% over last year.

The Company was named to the S&P 500 on March 31st. According to Robert H. Swanson, Chairman of the Board and CEO, "We are honored to be added to the prestigious S&P 500. This is a very significant milestone in the development of Linear Technology Corporation. We were founded in 1981 with the belief that a pure play analog semiconductor company could be both very profitable and a large company. The S&P 500 listing acknowledges that the Company is one of the most significant 500 publicly traded companies, since it lists companies that are considered leading companies in leading industries within the US economy. This will benefit our shareholders in that it should broaden the holding of our stock. It is also a gratifying accomplishment to the many dedicated employees whose efforts made it happen." *LT*
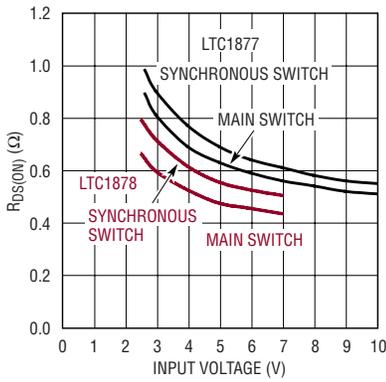
Figure 1. $R_{DS(ON)}$ for both switches vs input voltage

LTC1877/LT1612, continued from page 1

LTC1877 is designed for higher input voltage applications, whereas the LTC1878 is optimized for lower input voltage applications. For example, the LTC1877 provides up to 600mA of output current at an input voltage of 5V, whereas the LTC1878 provides the same amount of current at an input voltage of only 3.3V.

Both the LTC1877 and LTC1878 incorporate a constant frequency, current mode step-down architecture with on-chip power MOSFETs.

The LTC1877/LTC1878 include protection against output overvoltage, output short-circuit and power overdissipation conditions. When an overvoltage condition at the output (>6.25% above nominal) is sensed, the top MOSFET is turned off until the fault is removed. When the output is shorted to ground, the frequency of the oscillator slows to prevent inductor-current runaway. The frequency slows to about 80kHz or one-seventh of the nominal frequency. The frequency returns to 550kHz (or the
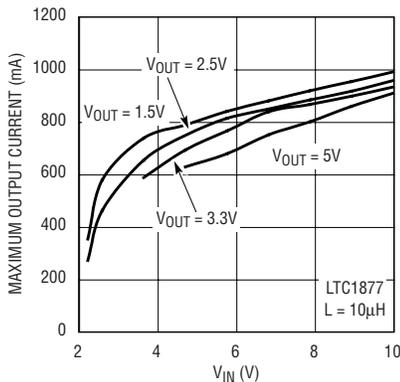
external synchronized frequency) when V_{FB} is allowed to rise to 0.8V. When there is a power overdissipation condition and the junction temperature reaches approximately 145°C, the thermal protection circuit turns off the power MOSFETs allowing the LTC1877/LTC1878 to cool. Normal operation resumes when the temperature drops by 10°C.

Burst Mode Operation

The LTC1877/LTC1878's Burst Mode operation is enabled by simply strapping the SYNC/MODE pin to V_{IN} or connecting it to a logic high ($V_{SYNC/MODE}$ >1.2V). In this mode, the peak current of the inductor is set to approximately 250mA, even though the voltage at the I_{TH} pin (the output of the error amplifier) would reflect a lower value. The voltage at the I_{TH} pin drops when the inductor's average current is greater than the load requirement. When the I_{TH} voltage drops below approximately 0.6V, a sleep signal is generated, turning off both power MOSFETs. The I_{TH} pin is

then disconnected from the output of the error amplifier and "parked" a diode voltage above ground. During this time, the internal circuitry is partially turned off, reducing the quiescent current to 10μA; the load current is now supplied by the output capacitor. When the output voltage drops by an amount dependent on the output voltage (on the order of 10mV for a 2.5V output), the I_{TH} pin reconnects to the output of the error amplifier, the top MOSFET is again turned on and the process repeats.

For frequency-sensitive applications, Burst Mode operation is disabled by connecting the SYNC/MODE pin to GND. In this case, constant-frequency operation is maintained at lower load currents together with lower output ripple. If the load current is low enough, cycle skipping will eventually occur to maintain regulation. In this mode, the efficiency will be lower at light loads, but becomes comparable to Burst Mode operation when the output load exceeds 50mA.

Figure 3. 2.5V/500mA step-down regulator

Figure 2. Maximum output current vs input voltage

Figure 4. Efficiency vs load current for Figure 3's circuit (Burst Mode operation enabled)
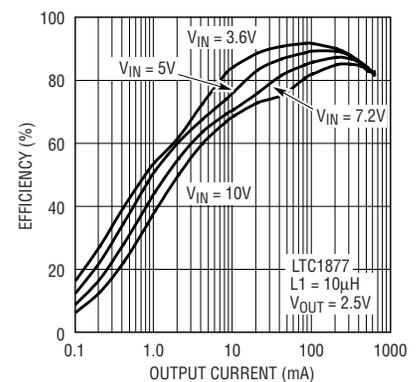
Figure 5. Efficiency vs load current for Figure 3's circuit (Burst Mode operation disabled)
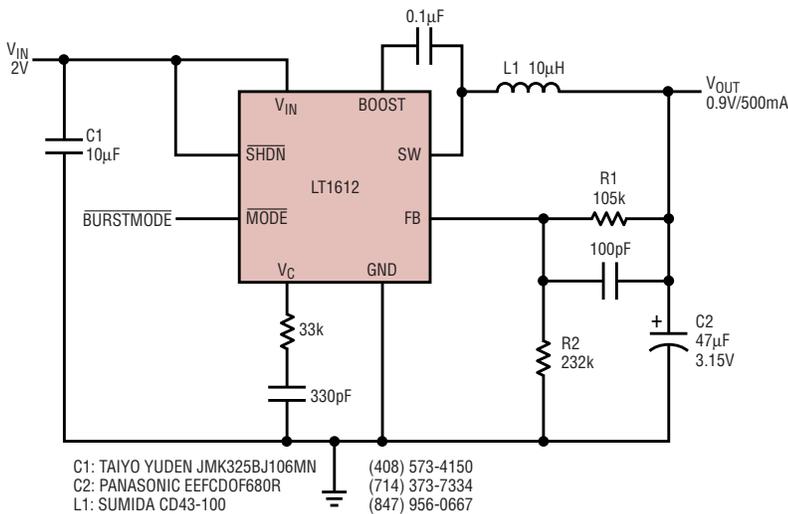
Figure 6. 2V to 0.9V step-down converter

C1: TAIYO YUDEN JMK325BJ106MN (408) 573-4150
C2: PANASONIC EEFCDOF680R (714) 373-7334
L1: SUMIDA CD43-100 (847) 956-0667

Figure 7. Efficiency curves for the LT1612 2V to 0.9V converter and a theoretical linear regulator

Frequency Synchronization

A phase-locked loop (PLL) on the LTC1877/LTC1878 allows the oscillator to be synchronized to an external source connected to the SYNC/MODE pin. The output of the phase detector at the PLL LPF pin operates over a 0V to 2.4V, range corresponding to 400kHz to 700kHz. When locked, the PLL aligns the turn-on of the top MOSFET to the rising edge of the synchronizing signal. Burst Mode operation is disabled when the LTC1877/LTC1878 is synchronized to an external source. Frequency synchronization is inhibited when the feedback voltage, V_{FB}, is below 0.6V. This prevents the external clock from interfering with the frequency foldback for short-circuit protection.

Low Input Supply and Operation in Dropout

The LTC1877/LTC1878 can operate on an input supply voltage as low as 2.65V. However, the maximum allowable output current is reduced at this low voltage due to an increase in the $R_{DS(ON)}$ of the P-channel MOSFET. See Figure 1 for a graph of switch resistance vs input voltage. Figure 2 shows the reduction in the maximum output current as a function of input voltage for various output voltages.

The LTC1877/LTC1878 is capable of turning the main P-channel MOSFET on continuously (100% duty cycle) when the input voltage falls to near the output voltage. In this dropout mode, the output voltage is determined by the input voltage minus the voltage drop across the internal MOSFET and the inductor resistance.

2.5V/500mA Step-Down Regulator

A typical circuit using the LTC1877 is shown in Figure 3. This design supplies a 500mA load at 2.5V with an input supply between 3.6V and 10V. The circuit operates at the internally set frequency of 550kHz. A 10µH inductor is chosen so that the inductor's current remains continuous during burst periods at low load current. For low output voltage ripple, a low ESR capacitor is used. All the components shown in this schematic are surface mount and have been selected to minimize the board space and height.

Efficiency Considerations

The efficiency curves for the 2.5V/500mA regulator at various supply voltages are shown in Figure 4. Note

C1: TAIYO YUDEN JMK325BJ106MN (408) 573-4150
C2: TAIYO YUDEN JMK325BJ226MN
L1: SUMIDA CD43-100 (847) 956-0667
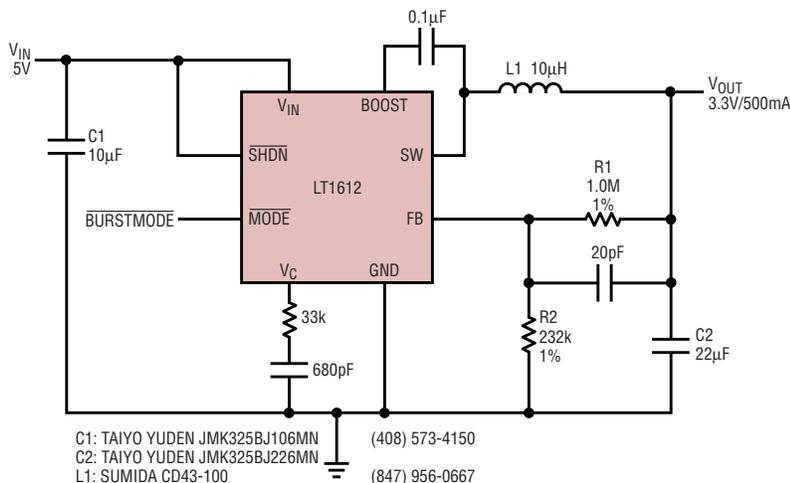
Figure 8. 5V to 3.3V/500mA converter
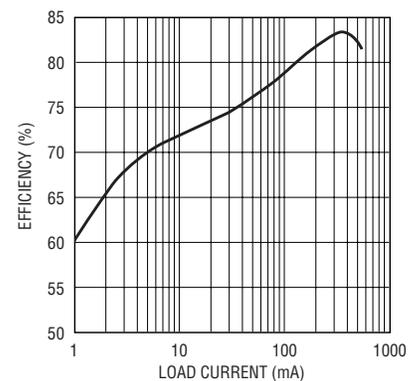
Figure 9. 5V to 3.3V converter efficiency peaks at 83%
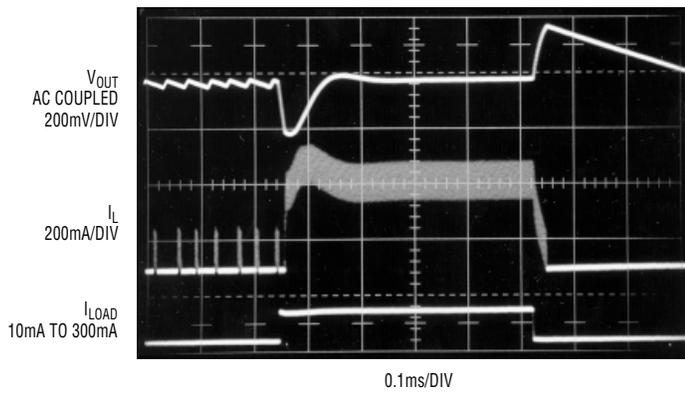
Figure 10. Transient response for Figure 9's circuit
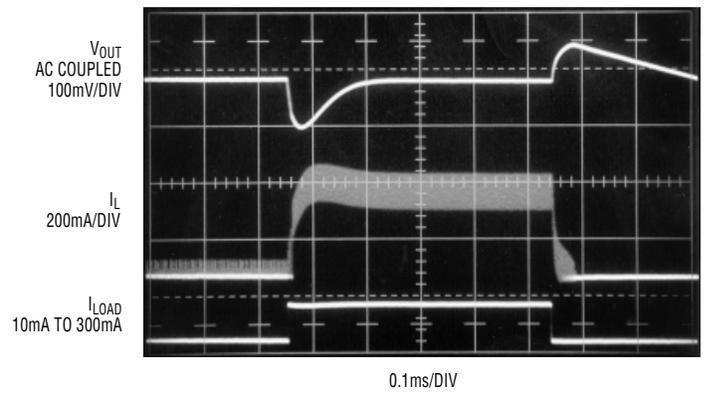
Figure 11. With the $\overline{\text{MODE}}$ pin high, low frequency ripple at V_{OUT} is eliminated

the flatness of the curves over the upper three decades of load current and that the efficiency remains high down to extremely light loads. Efficiency at light loads requires low quiescent current. The curves are flat because all significant sources of loss except for the 10μA standby current—I^2R losses in the switch, internal gate charge losses (to turn on the switch) and burst cycle DC supply current losses—are identical during each burst cycle. The only variable is the rate at which the burst cycles occur. Since burst frequency is proportional to load, the loss as a percentage of load remains relatively constant. The efficiency drops off as the load decreases below about 1mA because the non-load-dependent 10μA standby current loss then constitutes a more significant percentage of the output power. This loss is proportional to V_{IN} and thus its effect is more pronounced at higher input voltages. Figure 5 shows the effect on efficiency of disabling Burst Mode operation.

LT1612 Details

Like the LTC1877/LTC1878, the LT1612 also uses constant-frequency, current mode control. It is capable of Burst Mode operation or constant-frequency switching. Unlike the LTC1877/LTC1878, it uses bipolar power transistors instead of MOS switches. One of the main design challenges was providing the ability to operate with inputs as low as 2V.

To achieve this low voltage operation in a buck switching regulator, a bipolar NPN topside power switch is needed, rather than a MOS device. Because the NPN power transistor requires significant base drive current, efficiency is not as high as with its MOS counterpart. Thus, a small sacrifice in efficiency is made for this low voltage operation. The alternative to using the LT1612 to step down from low voltages is to use a linear regulator, which, of course, has its own disadvantages. Linear regulators are inherently inefficient because the power device is operated in the linear region. They must be physically larger to allow for dissipation of the extra heat generated and heat sinks are often needed, even at modest output power.

Applications

Figure 6 shows the LT1612 converting a 2V input down to 0.9V. The internal reference is set at 0.62V, which allows outputs below 1V. The graph in Figure 7 compares efficiency for the LT1612 to that of a theoretical linear regulator. At an input voltage of 2V and a load current of 200mA, the efficiency is 70% for the circuit in Figure 6 vs 45% for the linear regulator. At an input voltage of 3V, the linear regulator's efficiency is just 30%, while that of the circuit using the LT1612 drops to 65%. This clearly illustrates the power savings of the LT1612 as compared to a linear regulator.

The LT1612 is also well suited for more general purpose applications, such as the circuit shown in Figure 8. Here, the LT1612 is shown stepping down 5V to 3.3V. Efficiency, graphed in Figure 9, reaches 83% at a load current of 300mA. Maximum output power for this configuration is nearly 2W. Figure 10 shows transient response to a 300mA load step with Burst Mode enabled. If low noise operation is desired, the $\overline{\text{MODE}}$ pin can be pulled high, giving the response seen in Figure 11. The low frequency output voltage ripple is now eliminated.

Conclusion

The LTC1877/LTC1878 and LT1612 are well suited for medium to low power step-down applications with tight board space requirements. These synchronous buck regulators can deliver 500mA of output current and cover the input voltage range of 2V to 10V. The LTC1877/LTC1878 switch at 550kHz and offer the highest performance possible with efficiency exceeding 90%. An internal phase-locked loop allows frequency synchronization from 400kHz to 700kHz. The LT1612 operates at 800kHz and exhibits less than one fourth the power loss of a linear regulator at an input of 3V. All three parts come in the MS8 package and require minimal external components, which allows them to meet the tightest space requirements. **⫶LT**

New Rail-to-Rail Output Op Amps Bring Precision Performance to Low Voltage Systems

by Alexander Strong and Gary Maulding

Introduction

Linear Technology has recently released several new high precision op amps for use in low voltage systems. The LT1677, LT1881, LT1882, LT1884 and LT1885 all operate on power supplies from 3V or lower up to 36V and have rail-to-rail output voltage swing. These amplifiers allow high precision circuits to be implemented on low voltage power supplies, including single positive supplies. Rail-to-rail output stages maintain the output signal dynamic range by eliminating the base-emitter voltage drops of conventional emitter-follower output stages. Offset voltages are trimmed to less than 80µV, with the low temperature drift and low noise to be expected from bipolar transistor designs. High open-loop voltage gains maintain this accuracy over the output swing range.

The LT1677 is a rail-to-rail input, rail-to-rail output, single-supply version of the industry-standard LT1007. It features the lowest noise available for a rail-to-rail op amp: $3.2nV/\sqrt{Hz}$ and 70nV peak-to-peak 0.1Hz to 10Hz noise. An important feature in low voltage, single-supply applications (as low as 3V) is the ability to maximize the dynamic range. The LT1677's input common mode range can swing 100mV beyond either rail and the output is guaranteed to swing to within 170mV of either rail when loaded with 100µA. Low noise is combined with outstanding precision: the CMRR and PSRR are 130dB, the offset voltage is only 20µV and the open-loop gain is twenty-five million (typical). The LT1677 is unity-gain stable and has a gain bandwidth product of 7.2MHz. Figure 1 shows the input and output of an LT1677 in follower mode (gain = 1) using a single 3V supply. The output clips cleanly at the rails with no phase reversal, even when the input exceeds the rail by 0.5V. This has the advantage of eliminating lockup in servo systems.

The LT1881 dual and LT1882 quad op amps feature 150pA input bias currents, whereas the similar LT1884 and LT1885 dual and quad op amps trade slightly higher input bias currents of 500pA for three times higher speed. This series of amplifiers brings the performance of the LT1112 to low voltage applications that need the wide rail-to-rail output dynamic range. The graph of Figure 2 shows the input bias currents of the LT1884 over the common mode range of –14V to 14V. This low stable bias current behavior, when coupled with 50µV offset voltage, open-loop gains of over one million and high common mode rejection, allows precision accuracy to be maintained in systems with difficult source impedances.

Table 1 highlights key performance specifications for these amplifiers. Each of these amplifiers provides higher precision operation than was previously available in a rail-to-rail output swing amplifier.

Selecting the Right Amplifier

When choosing one of these amplifiers for an application, it is necessary to consider the signal levels and source impedance of the signal source. Low impedance, low level sources will usually operate best with the LT1677 amplifier. The ultralow $3.2nV/\sqrt{Hz}$ noise of the LT1677 will not obscure low amplitude signals. High gain can be used without introducing DC errors, an important feature in low supply voltage applications. Other natural applications for the LT1677 occur when the input signal range extends to either power supply rail. The LT1677 maintains good DC accuracy and noise performance with the inputs at either power supply rail. As source impedance increases the LT1881 dual or LT1882 quad ampli-
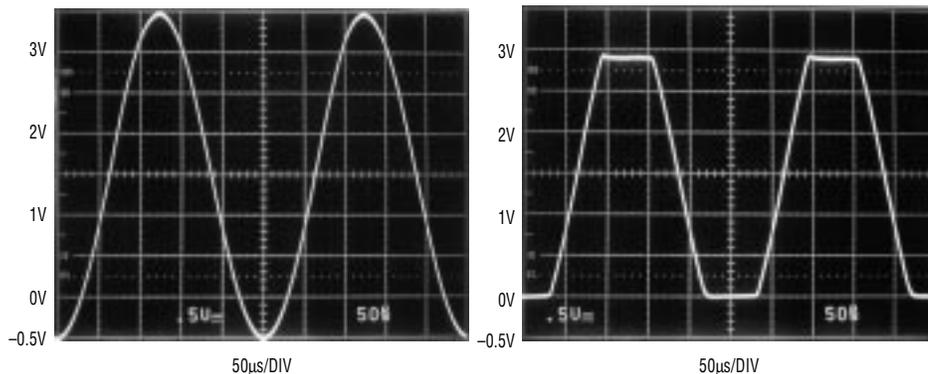
Figure 1. Input (left) and output (right) of an LT1677 configured as a voltage follower with input exceeding the supply voltage (V_S = 3V, input = –0.5V to 3.5V)
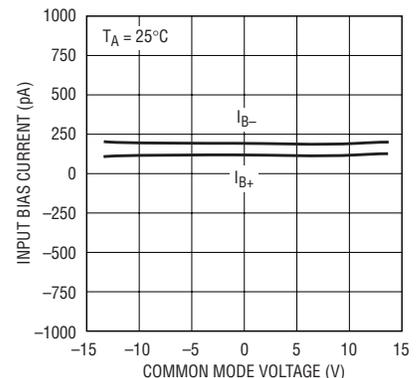
Figure 2. LT1884 input bias current vs common mode voltage

Table 1. Key performance specifications

Parameter	LT1677	LT1881	LT1882	LT1884	LT1885
Configuration	Single	Dual	Quad	Dual	Quad
Offset Voltage (Max)	60µV	80µV 50µV (A grade)	80µV	80µV 50µV (A grade)	80µV
Input Bias Current (Max)	20nA	500pA 200pA (A grade)	500pA	900pA 400pA (A grade)	900pA
Input Offset Current (Max)	15nA	500pA 200pA (A grade)	500pA	900pA 300pA (A grade)	900pA
Input Common Mode Range	V_{EE} + 1.7V to V_{CC} − 1V	V_{EE} + 1V to V_{CC} − 1V	V_{EE} + 1V to V_{CC} − 1V	V_{EE} + 1V to V_{CC} − 1V	V_{EE} + 1V to V_{CC} − 1V
(Reduced Precision)	V_{EE} − 0.1V to V_{CC} + 0.1V				
Output Swing I_L = 100µA	V_{EE} + 0.170V V_{CC} − 0.170V	V_{EE} + 0.06V V_{CC} − 0.230V	V_{EE} + 0.06V V_{CC} − 0.230V	V_{EE} + 0.06V V_{CC} − 0.230V	V_{EE} + 0.06V V_{CC} − 0.230V
Input Voltage Noise (Typ)	3.2nV/√Hz	14nV/√Hz	14nV/√Hz	9.5nV/√Hz	9.5nV/√Hz
Input Current Noise (Typ)	0.3pA/√Hz	0.03pA/√Hz	0.03pA/√Hz	0.05pA/√Hz	0.05pA/√Hz
Supply Voltage Range	2.7V to 40V	2.7V to 36V	2.7V to 36V	2.7V to 36V	2.7V to 36V
Supply Current per Amplifier (Max)	3.5mA	0.9mA	0.9mA	0.9mA	0.9mA
Gain Bandwidth Product (Typ)	7.2MHz	1MHz	1MHz	2MHz	2MHz
Slew Rate (Typ)	1.7V/µs	0.15V/µs, −0.11V/µs	0.15V/µs, −0.11V/µs	0.5V/µs, −0.4V/µs	0.5V/µs, −0.4V/µs
Open Loop Gain, R_L = 10k (Typ)	25V/µV	1V/µV	1V/µV	1V/µV	1V/µV
C_{LOAD}, A_V = + 1 (Max)	1000pF	1000pF	1000pF	300pF	300pF

fiers become the better choice. These amplifiers have an input noise current that is less than one tenth of the LT1677's. The input bias currents are as low as those of most FET input devices and they maintain their low I_B at high temperatures where FET leakage currents increase exponentially. The input offset voltage and temperature drift are far superior to those of JFET input amplifiers. The LT1881 and LT1882 also operate at only 1mA supply current per amplifier.

The LT1884 dual and LT1885 quad amplifiers have input bias and offset currents almost as low as the LT1881 and LT1882, but have approximately three times faster AC response. These amplifiers can be employed in the same types of applications as the LT1881/LT1882, where AC response has greater value and the cost in DC accuracy is minimal. Supply current is the same 1mA per amplifier.

Low Noise Remote Geophone Amplifier

Small signal applications require high gain and low noise, a natural for the LT1677. Its 1kHz noise is 100% tested and is guaranteed to be less than 4.5nV/√Hz. Figure 3 is a 2-wire remote geophone preamp that operates on a current-loop principle and, as such, has good noise immunity. A low noise amplifier is desired in this application because the seismic signals that must be resolved are extremely small and require high gain. The LT1677 amplifies the geophone signal by one hundred and transmits it back to the operator by modulating the current through R12. U2 is an LT1635 micropower rail-to-rail op amp and reference configured as a stable current source of 5mA, which powers the LT1677 and another LT1635, this time configured as a 3V shunt regulator. The idling current through R10 is set up from the voltage at the emitter of Q2 (3V) and the voltage at the emitter of Q3 (1.85V from the ratio of R6 and R7). This places about 1.15V (zero TC, since Q1 temperature compensates Q2) across R10, thereby pulling an additional 7mA from the main supply through Q2. Of the total 12mA across the receiver resistor R12, 7mA is being modulated by allowing a peak signal of ±1.5V about the 3V bias point across R12.
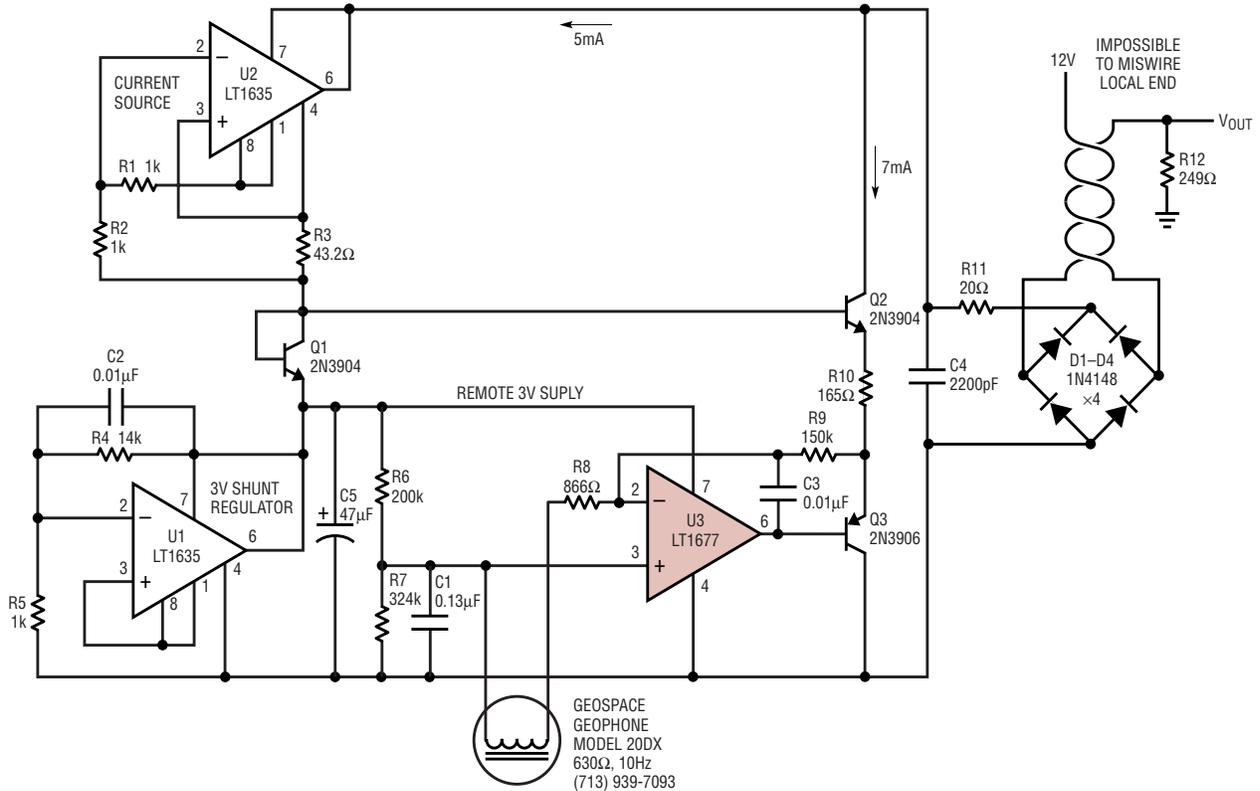
Figure 3. Geophone amplifier

Buffered Precision Voltage Reference

Figures 4a and 4b, respectively, show the gain (V_{OUT}/V_{IN}) and gain linearity for the LT1677 sinking or sourcing current into a 600Ω load with a single 5V supply. A horizontal trace indicates high gain; a straight trace indicates constant gain vs output voltage—this is excellent gain linearity. The trace for the ground-referenced load is more horizontal; this indicates higher loop gain, due to the additional gain of the PNP output stage. Gain and gain linearity are improved by increasing the load resistor. Figure 4c shows the gain for a higher load resistance at a ±15V supply (note the change of vertical scale).

When teamed up with a precision shunt voltage reference such as the LT1634 (Figure 5), the LT1677, used as a precision buffer, can enhance the reference voltage without significantly increasing the error budget. The LT1677 is used to make a 2.5V voltage source from a single 5V supply. The tolerance of the LT1634BCS8-2.5 is ±1.25mV (0.05%); the LT1677 adds only a ±60μV offset voltage. The output impedance of the voltage source for a wide range of sourcing or
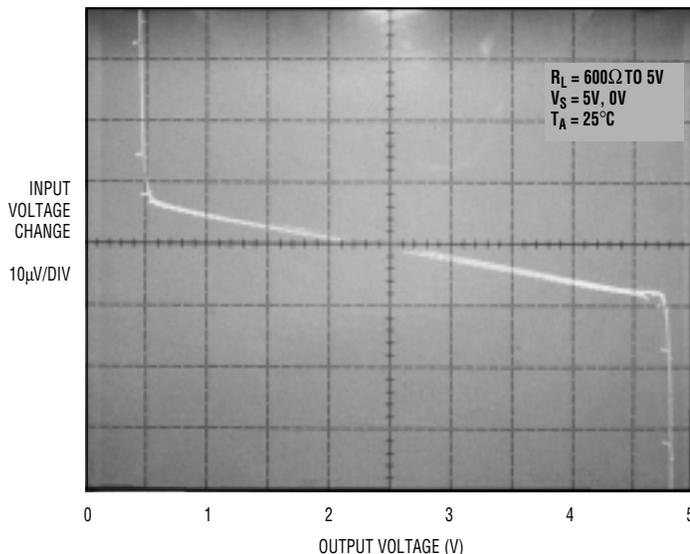
Figure 4a. Gain linearity of the LT1677 sinking current
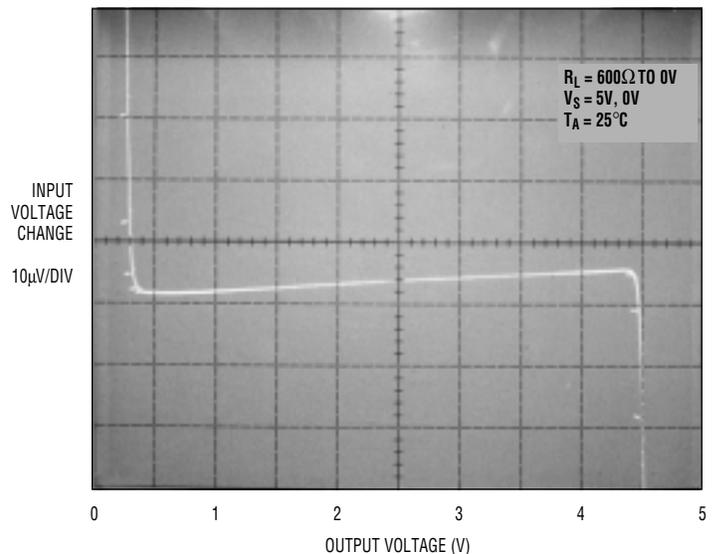
Figure 4b. Gain linearity of the LT1677 sourcing current
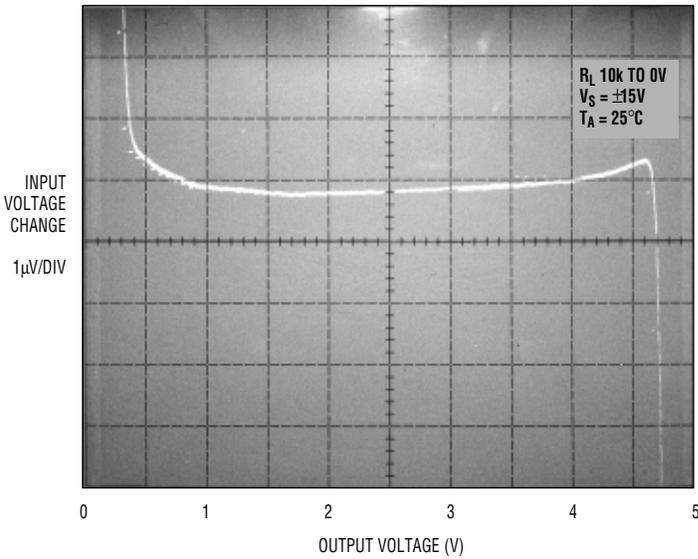
Figure 4c. LT1677 gain linearity with a higher load resistance and supply voltage

Figure 5. 2.5V reference from a 5V supply

sinking currents can be calculated by dividing the LT1677's 80Ω open-loop resistance by its loop gain. This results in an output impedance of less than 1mΩ. The dynamic impedance at 10kHz drops from 20Ω (LT1634) to less than 0.01Ω (LT1677). The change in output voltage due to die temperature is reduced thirty times by shifting the load current to the LT1677. The temperature coefficient of the LT1677, 2µV/°C max, is negligible compared to the 62.5µV/°C TC (25ppm/°C • 2.5V) of the LT1634.

High-Side Current Sensing

Figure 6 is a precision high-side current sense amplifier that can operate on a single supply from 3V to 40V. The current flowing into the load produces a voltage drop across the line resistor R_{LINE}. The LT1677 forces a current through R_{IN}, which dupli-

cates the voltage drop across R_{LINE}. This current is then converted back to a voltage across R_{OUT}. By selecting appropriate values for these three resistors, the transfer function can be tailored to fit any application. Since the LT1677 can operate from either rail, a low-side current sense circuit can also be realized.

Low Input Bias Currents Fit Other Applications

The applications described above benefit from the LT1677's low input noise and rail-to-rail inputs, but other applications require high DC accuracy with low input bias currents. The LT1881/LT1882/LT1884/LT1885 provide the appropriate answer in these applications. Circuits that have high source impedances make the input bias current and input offset current characteristics of the ampli-

fier important considerations. The amplifiers' input currents, acting on the source impedance, generate a DC offset error, limiting precision sensing of the source signal. The input voltage noise of the amplifier becomes a less important parameter because the noise generated by the high source impedance will typically be larger than the op amp's input noise. Input current noise is now the more important amplifier noise characteristic. The LT1881/LT1882/LT1884/LT1885 have very low input noise current, as shown in Table 1. Figure 7 graphs the total system noise due to amplifier input noise voltage, input noise current and the source resistance Johnson noise. The graph shows that the LT1677 is the correct amplifier when source resistance is below 20k. Above 200k an LT1881, LT1882, LT1884 or LT1885 are the best choices for minimizing system noise. In the

$$V_N = \sqrt{(V_{OP\ AMP})^2 + 4KT \cdot R_S + 2_q \cdot I_S \cdot R_S{}^2}$$

LT1677	3.2nV/√Hz	0.30pA/√Hz
LT1884	9.5nV/√Hz	0.05pA/√Hz
LT1881	14.0nV/√Hz	0.03pA/√Hz
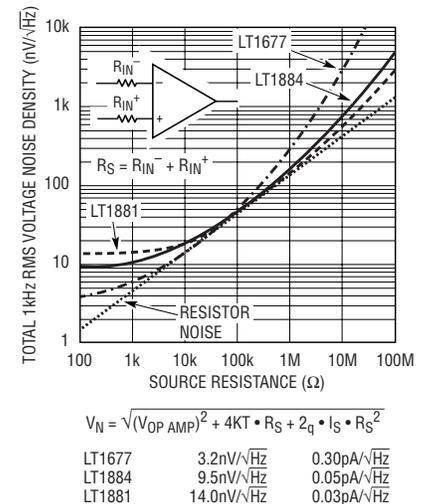
Figure 7. 1kHz noise voltage vs source resistance

$$\frac{V_{OUT}}{I_{LOAD}} = R_{LINE}\frac{R_{OUT}}{R_{IN}}$$
$$= 2V/AMP$$

*ZETEX   (516) 543-7100

Figure 6. Precision high-side current sense amplifier
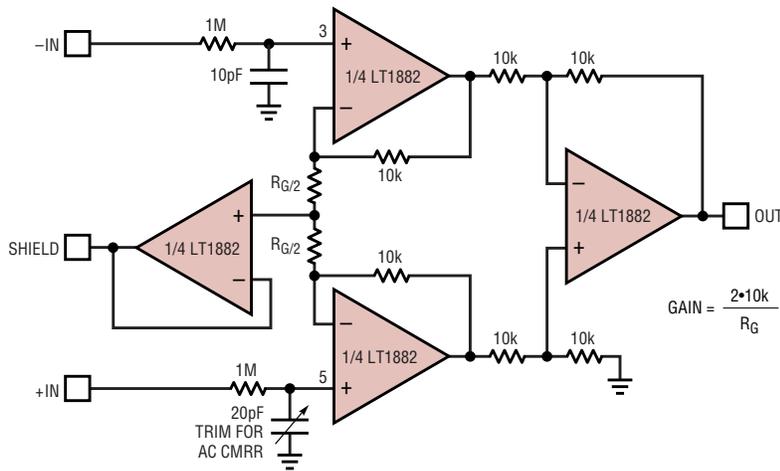
Figure 8. Input-fault-protected instrumentation amplifier

$$\text{GAIN} = \frac{2 \cdot 10k}{R_G}$$

intermediate range of 20k to 200k, the source resistor's noise dominates and all of the amplifiers will give nearly equal system noise performance.

Input-Fault-Protected Instrumentation Amplifier

Figure 8 is a fault-protected instrumentation amplifier with shield drive. The 1M input resistors allow high voltage faults to be tolerated without damaging the amplifiers. An AC line fault will result in only 180µA of peak current flowing into the LT1882's input pins. Normally, such a high input resistance would result in huge DC offsets due to the input bias currents from the amplifiers. The LT1882's I_B is a low 500pA max. In addition, by using the guaranteed matching of I_B between amplifiers A and B or C and D, a worst-case I_B mismatch of 700pA is guaranteed. This results in a worst-case offset error of 700µV; typically this error would be less than 200µV. A pair of LT1881 "A" grade devices may be used to ensure a worst-case error less than 300µV.

The LT1882's input noise current working against the 1M source resistance generates a noise voltage of 42nV/√Hz. This compares to the protection resistors' Johnson noise of 182nV/√Hz and the amplifier's input noise voltage of 14nV/√Hz. Hence, the 1M protection resistors dominate the system's input noise. It is interesting to note that the LT1677 would contribute 420nV/√Hz of input noise

due to its input noise current, dominating the system noise level. In high source impedance applications, the LT1677 low noise amplifier will generate more system noise than an LT1882, which has a higher input voltage noise level. This underscores the need for proper amplifier selection based upon the application. In high source impedance applications, input current noise is a more important parameter than input voltage noise.

Low Voltage –50°C to 600°C Digital Thermometer

The circuit of Figure 9 is a digital thermometer which uses a 1k RTD sense element in a linear-output, single-leg bridge configuration. An LT1881 dual amplifier is used to provide the negative bridge excitation as well as output amplification and buffering. An LTC1287 A/D converter

digitizes the output. No reference is needed; the bridge excitation and A/D reference are the power supply. The fixed bridge elements and output gain resistor are made with series and parallel combinations of an $8 \times 2k$ resistor pack to get the best precision at a reasonable price.

The LT1884's low offset voltage and rail-to-rail output swing enable the circuit to function properly. The first amplifier, A1, is used to drive the negative side of the bridge to force a constant current excitation of the variable resistance element. The constant current drive results in the output voltage being perfectly linear with respect to the variable resistance. Since the LT1884 is able to swing to within to 50mV of the negative supply, the full dynamic range of the transducer is available even when operating on low voltage supplies. The second amplifier provides voltage gain to the bridge output to use the full-scale range of the A/D converter. The LT1884's low offset voltage is an important attribute of the gain amplifier.

±4.096V Swing 16-Bit Voltage Output DAC on a ±5V Supply

The final application, Figure 10, shows an LT1881 dual amplifier used as an I/V converter with the 16-bit LTC1597 DAC. The first amplifier is used to invert and buffer the LT1634 reference. This amplifier has no trouble swinging to –4.096V even with low supply voltages. The LT1881's exceptionally low I_B and offset voltage

$$V = \frac{V_{CC}}{2} \pm 1.588mV/°C$$
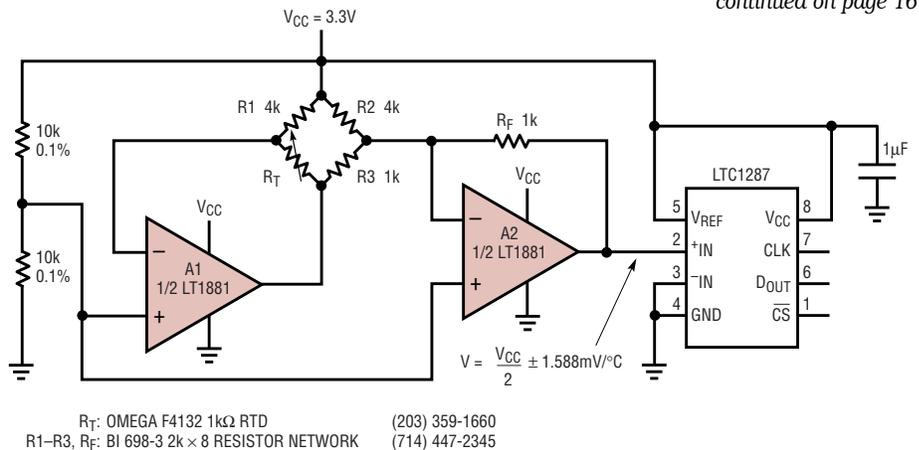
R_T: OMEGA F4132 1kΩ RTD   (203) 359-1660
R1–R3, R_F: BI 698-3 2k × 8 RESISTOR NETWORK   (714) 447-2345

Figure 9. –50°C to 600°C digital thermometer runs on 3.3V

DC Accurate, Rail-to-Rail Active RC Lowpass Filter Replaces Discrete Designs—One Resistor Value Sets the Cutoff Frequency

by Doug La Porte

No More Complex Equations, No More Precision Capacitors, No More Frustration

The LTC1563-2 and LTC1563-3 form a family of extremely easy to use, 4th order active RC lowpass filters (no signal sampling or clock requirements). They cover cutoff frequencies ranging from 256Hz to 256kHz while operating at supplies from as low as a single 3V (2.7V minimum) up to ±5V. The LTC1563 also features rail-to-rail input and output operation with, typically, 1mV of DC offset. The design of the most popular filter responses is trivial, requiring only six resistors of identical value and no external capacitors. The cutoff frequency of unity-gain Butterworth or Bessel filters is set with a single resistor value calculated using the following simple formula:

$$R = 10k\Omega \cdot (256kHz/f_C)$$

where f_C is the cutoff frequency in Hertz.

The LTC1563-2 is used for a Butterworth response, whereas the LTC1563-3 is used for a Bessel response.

Beyond design simplicity, *the LTC1563 facilitates manufacturability.* For a discrete design to achieve the ±2% cutoff frequency accuracy of the LTC1563, precision capacitors (2% or better) are required. These capacitors are not readily available and can present a difficult and costly purchasing problem. A typical discrete design also requires four resistor values and four capacitor values—eight reels of components. This leads to eight times the purchasing, stocking and assembly costs and eight reels of components on the automated assembly machine. Many large circuit boards require more component reels than the assembly machine can accommodate leading to costly secondary operations. The LTC1563 decreases purchasing, stocking and assembly costs while removing seven component reels from the assembler.

The LTC1563 is also very versatile. The proprietary architecture yields effortless design of the unity gain Butterworth and Bessel filter responses while still allowing complex, arbitrary filter responses with any gain desired. A Chebyshev, Gaussian or any other all-pole response, with or without gain, can be obtained using unequal valued resistors calculated with a more complex set of equations (for the best results use FilterCAD version 3.0). Designs ranging from a dual 2nd order filter up to an 8th order filter (two cascaded devices) are also easily obtained. With the addition of two capacitors, a single LTC1563 can be used to implement a 6th order lowpass filter. In another application, the two additional capacitors render a simple wideband, low Q bandpass filter.

Salient performance features of the LTC1563 family include the following:

❏ $256Hz \leq f_C \leq 256kHz$
❏ f_C accuracy < ±2% (typ)
❏ Continuous time filter—no clock, no sampling
❏ SINAD ≥ 85dB at $3V_{P-P}$, 50kHz—compatible with 16-bit systems
❏ Rail-to-rail input and output operation
❏ Output DC offset voltage ≤ ±1mV (typ)
❏ DC offset drift ≤ ±5µV/°C (typ)
❏ Operates from a single 3V (2.7V min) to ±5V supplies
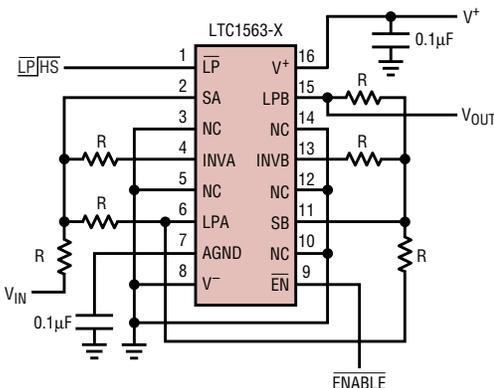
Figure 1. Typical LTC1563-X single-supply application
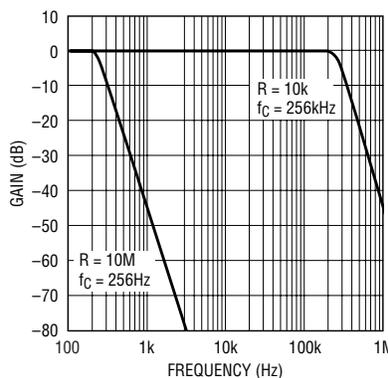
Figure 2. LTC1563-2 Butterworth response of Figure 1's circuit for R = 10M and R = 10k
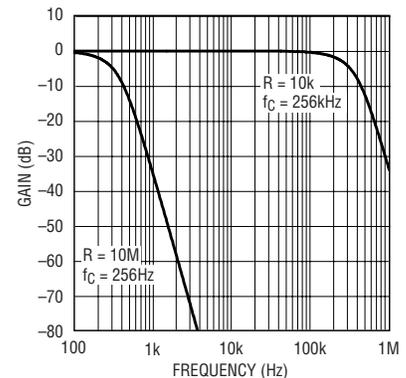
Figure 3. LTC1563-3 Bessel response of Figure 1's circuit for R = 10M and R = 10k
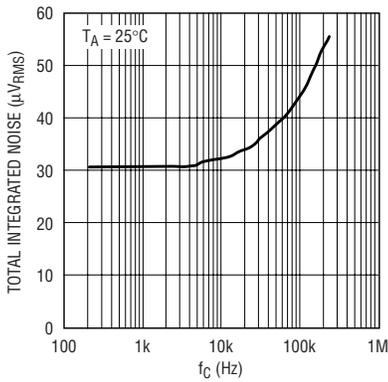
Figure 4. LTC1563-X total integrated noise vs cutoff frequency
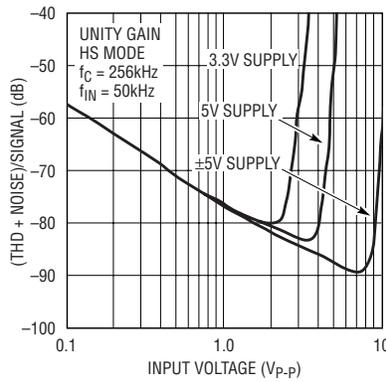
Figure 5. LTC1563-X THD plus noise performance vs input signal amplitude
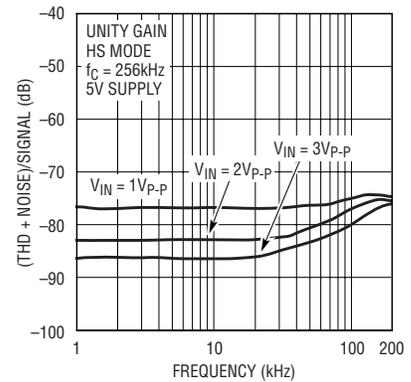
Figure 6. LTC1563-X THD plus noise vs input signal frequency

❏ Low power mode, I_{SUPPLY} = 1mA (typ), $f_C \leq$ 25.6kHz

❏ High speed mode, I_{SUPPLY} = 10mA (typ), $f_C \leq$ 256kHz

❏ Shutdown mode, I_{SUPPLY} = 1µA (typ)

❏ Narrow SSOP-16 package, SO-8 footprint

Typical 4th Order Butterworth and Bessel Applications

Figure 1 illustrates a typical LTC1563 single-supply application, with Figure 2 showing the Butterworth frequency response of the LTC1563-2 and Figure 3 showing the Bessel frequency response of the LTC1563-3. As the R value is decreased from 10M to 10k, the cutoff frequency increases from 256Hz to 256kHz. For cutoff frequencies below 25.6kHz, significant power can be saved by placing the LTC1563 into the low power mode. Connect the $\overline{LP}$ pin to the V⁻ potential to enable the low power mode. All other applications should place the part in the high speed mode by leaving the $\overline{LP}$ pin open or connecting it to the V⁺ potential. The high speed mode, in addition to supporting higher cutoff frequencies, has a lower DC offset voltage and better output drive capability than the low power mode. The minimum supply voltage in the high speed mode is 3V, whereas the low power mode supports 2.7V operation. The shutdown mode is available at all times. The $\overline{EN}$ pin is internally pulled up to the V⁺ potential, causing the LTC1563 to default to the shutdown mode. To enable normal operation, the $\overline{EN}$ pin must be pulled to ground. In the shutdown mode, the supply current is typically 1µA and 20µA maximum over temperature.

Performance Specifications

The LTC1563 family has outstanding DC specifications. The DC offset of the filter in the high speed mode is typically ±1mV, with a maximum offset over temperature of ±3mV. The DC offset is slightly greater in the low power mode at ±5mV maximum over temperature on the lower supply voltages and ±6mV maximum over temperature on a ±5V supply. The DC offset drift is only 10µV/°C.

The LTC1563's SINAD performance with lower signals is dominated by the noise of the part. Figure 4 is a plot of the noise vs the cutoff frequency.

The total integrated noise (over a bandwidth of twice the cutoff frequency) is 32µV_RMS at the lowest cutoff frequency and increases to 56µV_RMS at the highest cutoff frequency. Figure 5 shows the SINAD performance as function of the input signal amplitude for a 50kHz signal. The plot demonstrates that distortion is not a significant factor at smaller signal amplitudes. Distortion is only noticeable when the signal amplitude is very large, within about 1V of the supply rails. The distortion performance also holds up well at higher frequencies, as Figure 6 illustrates. The SINAD is nearly flat over all frequencies, indicating again that noise is the determining function. The SINAD is about 85dB for the 3V_P-P input, indicating that this part is suitable for 16-bit systems.

Table 1. LTC1563 family configurations		
Design	**LTC1563 Support**	**FCAD 3.0 Support**
2nd order LPF	Yes	Yes
Dual 2nd order LPF	Yes	Yes
3rd order LPF (one capacitor)	Yes	Yes
Dual 3rd order LPF (two capacitors)	Yes	Yes
4th order LPF	Yes	Yes
5th order LPF (one capacitor)	Yes	Yes
Pseudo–6th order LPF (one part, two capacitors)	Yes	Yes
Standard 6th order LPF (two parts, no capacitors)	Yes	Yes
7th order LPF (one capacitor)	Yes	Yes
8th order LPF	Yes	Yes
9th order LPF (one capacitor)	Yes	Yes
Wideband bandpass (two capacitors)	Yes	No
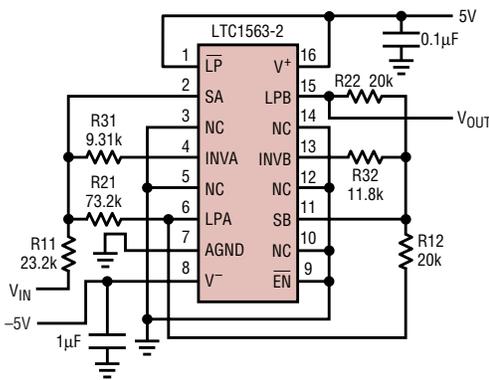
Figure 7. 0.5dB, 150kHz, Chebyshev lowpass filter with a DC gain of 10dB
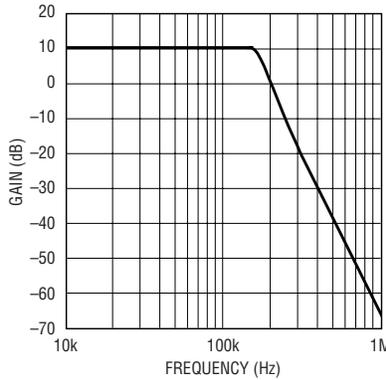
Figure 8. Frequency response of Figure 7's circuit

Transfer Function Capabilities

The LTC1563 was designed to make implementing standard unity-gain, 4th order Butterworth and Bessel filters as simple as possible. Although this goal was accomplished, *the part also maintains tremendous flexibility.* Virtually any all-pole transfer function can be realized with the LTC1563-2. Table 1 lists the many filter configurations attainable with the LTC1563 family. The actual transfer function (pole locations) of the filter is nearly arbitrary.

4th Order Lowpass Filters with Gain

Filters responses other than Butterworth and Bessel, filters with gain and higher order filters are easily obtained with the LTC1563. The design equations are more complex than the simple unity-gain Butterworth and Bessel equation. Refer to the LTC1563 data sheet for the actual equations. For the best design result, use FilterCAD version 3.0 (or later). FilterCAD uses a very complex and accurate algorithm to account for most parasitics and op amp limitations. Using FilterCAD will yield the best possible design.

Figure 7 shows an LTC1563-2 employed to make a 4th order, 150kHz, 0.5dB ripple Chebyshev lowpass filter with a DC gain of 10dB. The frequency response is shown in Figure 8. All of the gain is realized in the first section to achieve the lowest output voltage noise. Note that the schematic, and thus the PC board layout, is the same as a unity gain Butterworth lowpass filter except that the resistor values are different. The same PC board layout could be used to build an infinite number of lowpass filters, each with a different gain, transfer function and cutoff frequency.

8th Order Lowpass Filter

Designing an 8th order filter is just as easy as a 4th order filter. Of course, the final solution uses twice as many components but the design is essentially the same procedure. Using FilterCAD makes the design procedure simple and straightforward. Figure 9 shows the schematic for a 180kHz 8th order, Butterworth lowpass filter with a gain of 6dB along with a plot of its frequency response. The solution is quite compact, simple to layout on the PC board and uses only standard 1% resistors. A discrete solution would involve several precision capacitors and a much more complicated layout accompanied by numerous layout-related parasitics. With the discrete solution, you may not get the response that you expect, due to these parasitic elements.
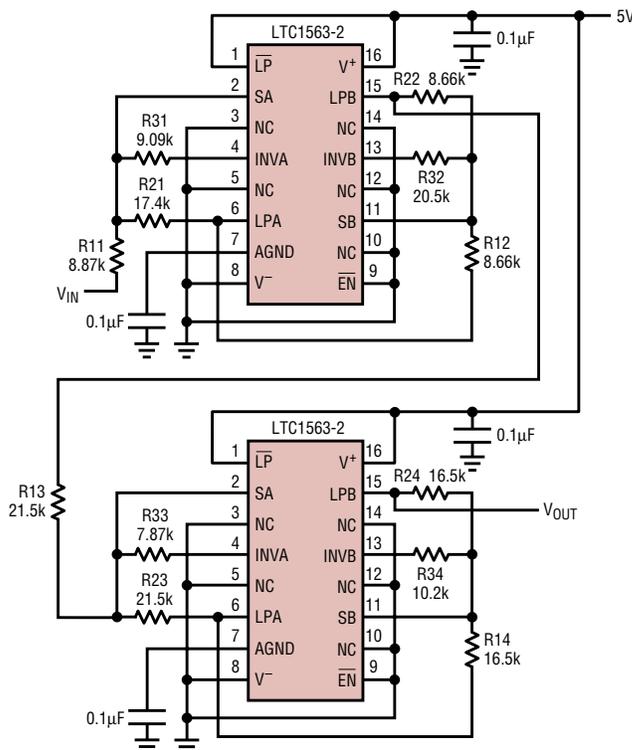
Figure 9a. 180kHz 8th order, Butterworth lowpass filter with a DC gain of 6dB
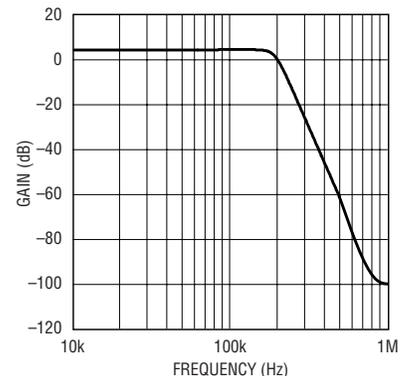
Figure 9b. Frequency response of Figure 9a's circuit
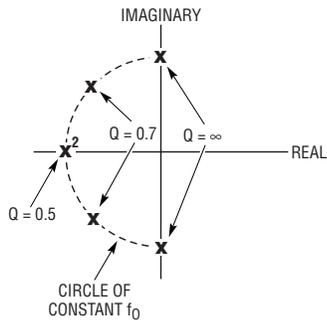
Figure 10. Locations of complex pole pairs of fixed f_O and different Qs

Figure 11. Pole locations for the classic Butterworth and pseudo-Butterworth lowpass filters

CLASICAL BUTTERWORTH

$f_C = 100kHz$

f_O	Q
100kHz	0.5176
100kHz	0.7071
100kHz	1.9319

PSEUDO-BUTTERWORTH

$f_C = 100kHz$

f_O	Q
100kHz	——
100kHz	——
100kHz	0.7358
100kHz	1.9319

Pseudo–6th Order Lowpass Filter

A textbook, theoretical 6th order lowpass filter is composed of three 2nd order sections, each realizing a complex pole pair. The LTC1563 has two 2nd order sections to yield two complex pole pairs. A 6th order lowpass filter can be made using two LTC1563 parts (with half of the second part unused) or, by using an old filter trick, it can be implemented with a single part.

First a little background material (a bit of filter theory, but not too bad). Each 2nd order, complex pole pair can be defined by the parameters f_O and Q. Figure 10 illustrates that each complex pole pair has the same real component and the complementary imaginary components. The f_O parameter is the magnitude of the poles and the Q is a measure of how close the poles are to the real or imaginary axis. The closer the poles are to the imaginary axis, the higher the Q becomes, until Q reaches infinity when the poles are directly on the imaginary axis. As the pole pair moves close to the real axis, the Q decreases in value until the Q is at 0.5 when they are both on the real axis. A pole pair with a Q of 0.5 is mathematically identical to two 1st order, real poles.

Armed with a little filter knowledge, we are now ready for the trick. All 6th order filters have three f_O and Q pole pairs. The pair with the lowest Q usually has a Q somewhere between 0.5 and 0.6. The trick is to substitute two 1st order, real poles (the equivalent of a 2nd order section with a Q of 0.5) for the pole pair with the lowest Q value. To compensate for this bending of the ideal mathematics, it is necessary to go back and tweak some or all of the f_O and Q values in the design. The resulting filter is no longer the exact, ideal, theoretical mathematical implementation, but with care you can get a frequency response and a step response that differ imperceptibly from the textbook plots. The name "pseudo–6th order filter" is somewhat misleading, because the filter is clearly of the 6th order (six poles with a final attenuation slope of –36dB/octave). It is only "pseudo" in the sense that the filter does not conform to the classical, standard mathematical models. If your company is shipping mathematics, stick with the textbook 6th order response. However, realize that once you consider the component tolerances, you still end up with an approximation. Most products really require filters that meet a specific set of performance criteria (for example, cutoff frequency, passband flatness, stopband attenuation, step response overshoot and step response settling) in a simple, reproducible and cost effective manner. The textbook responses are just a convenient way to synthesize a filter (or a good starting point in the filter design).

The classical response is tweaked manually using the FilterCAD Custom Design feature. Start with the textbook 6th order lowpass filter. Open the Step Response and Frequency Response windows by clicking on the appropriate buttons. In each response window, save the trace to compare the responses with the tweaked design. Next, click on the Custom Response button, remove the low Q
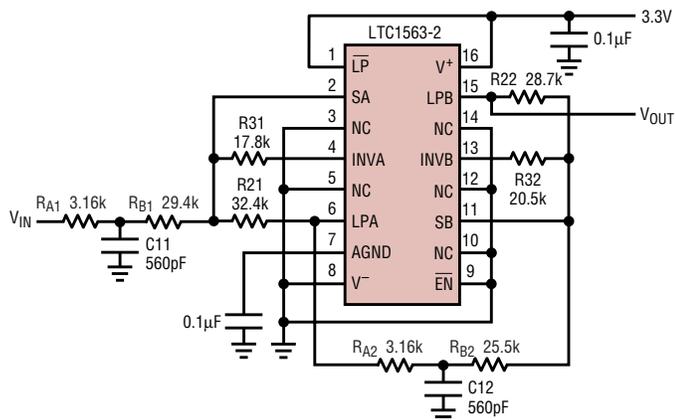
Figure 12. 100kHz, 6th order pseudo-Butterworth lowpass filter
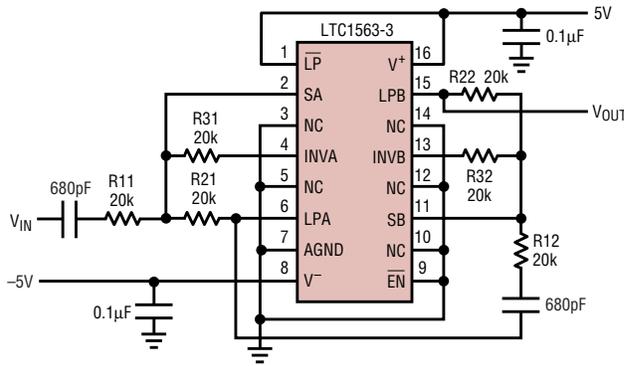
Figure 13. 50kHz wideband bandpass filter
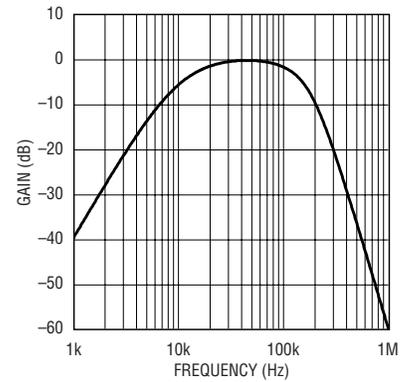
Figure 14. Frequency response of Figure 13's circuit

section and add two 1st order lowpass sections at the same f_O. Finally, alter the new design's f_O and Q parameters as required, while monitoring the frequency and step response windows, until the desired responses are achieved. With some practice, an intuitive sense of which parameters need adjustment is developed.

The procedure is clearly illustrated with the following 6th order 100kHz Butterworth lowpass filter example. Figure 11 shows the pole locations and f_O and Q values for a textbook 6th order Butterworth lowpass filter and the pseudo–6th order equivalent values. The circuit implementation, Figure 12, of this transfer function uses a standard 4th order type of circuit where the input resistor is split into two resistors with an additional capacitor to ground in between the resistors. This "TEE" network forms a single real pole. By making

this modification to both sections, a pair of real poles is added to the 4th order network forming the desired pseudo–6th order filter. The TEE network technique is also used to give the single real pole required in all odd-order responses.

Wideband Bandpass Filters

Although the LTC1563 family does not directly support classical bandpass filters, you can successfully implement a wideband bandpass filter using the standard 4th order lowpass circuit and a couple of additional capacitors. The resulting filter is more of a highpass-lowpass type of filter than a true bandpass. You can design outstanding, highly selective bandpass filters using the LTC1562 family of universal filter products (see *Linear Technology* VIII:1 [February 1998] and IX:1 [February 1999])—the best continuous time filters in the

industry for bandpass and elliptic highpass or lowpass filters. Although the LTC1562 is the best part for narrowband bandpass filters, if your requirements are less stringent, the LTC1563 family can provide a simple, cost-effective wideband bandpass filter.

Figure 13 shows the schematic of an LTC1563-3 used to make a simple, wideband bandpass filter centered at 50kHz. The frequency response is shown in Figure 14. The design procedure for this type of filter does not conform to any standard procedure. It is best to start with a standard lowpass filter and add two 1st order highpass sections to the transfer function. Adjust the highpass corner and the lowpass f_C up and down until the desired transfer function is achieved. The design in Figure 13 starts with a standard, unity gain, 4th order Bes-
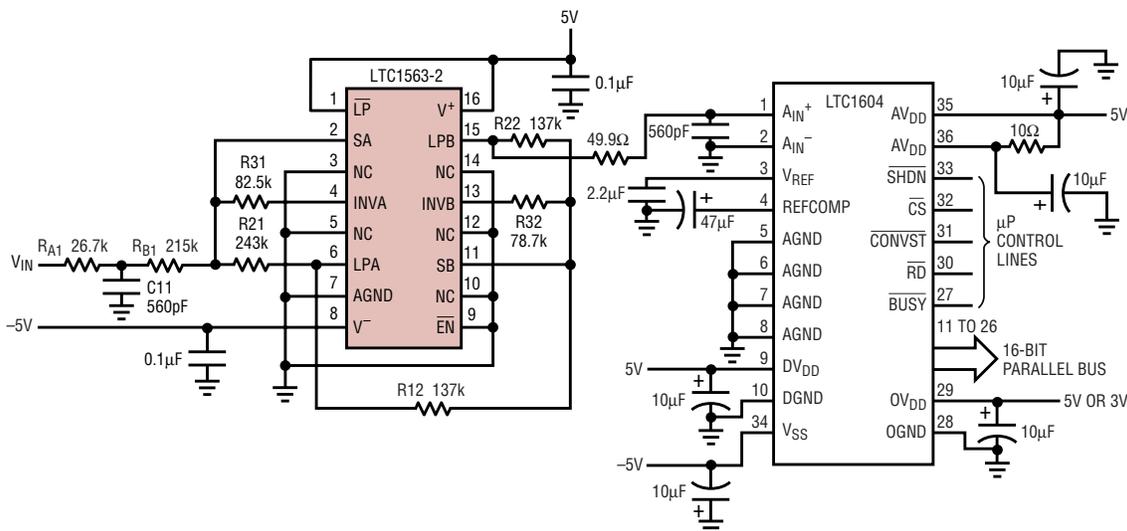
Figure 15. 0.1dB, 5th order, 22kHz Chebyshev lowpass filter driving an LTC1604 16-bit ADC

sel lowpass filter with a cutoff frequency of 128kHz. Each section is then AC coupled through the 680pF capacitors. Each capacitor, working against its input resistor, realizes a 1st order highpass function with the cutoff frequency (11.7kHz in this design) defined by the following equation:

$$f_C = 1/(2 \cdot \pi \cdot R \cdot C) \quad (R = R11 \text{ or } R12)$$

The resulting circuit yields a wideband bandpass filter that uses only one resistor value and one capacitor value. Note that although FilterCAD does not provide complete support for this type of filter with the LTC1563, you can still use the program's Custom Design mode to set the required transfer function. After the transfer function has been chosen, use FilterCAD to design the lowpass part of the filter and then use the simple highpass formula above to complete the circuit.

Driving 16-Bit ADCs

The LTC1563 is suitable for 16-bit systems. Figures 3 through 5 show that the LTC1563's noise and SINAD is commensurate with 16-bit data acquisition systems. These measurements were taken using laboratory equipment and well-behaved loading circuitry. Many circuits will perform
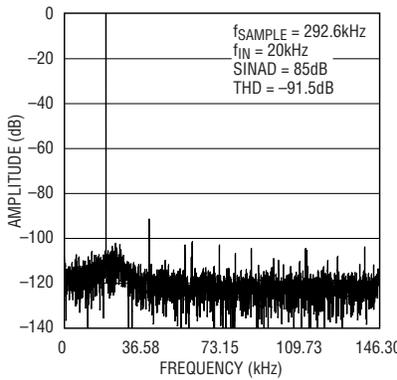
Figure 16. FFT of the ADC output data from Figure 15's circuit

well in this environment only to fall apart when driving the actual A/D converter. Many modern ADCs have a switched capacitor input stage that often proves to be difficult to drive while still maintaining the converter's 16-bit performance. The LTC1563 succeeds with only a little help from a resistor and a capacitor.

Figure 15 shows the LTC1563-2 configured as a 5th order, 22kHz, 0.1dB ripple Chebyshev lowpass filter driving an LTC1604 16-bit ADC. The converter operates with a 292.6kHz sample clock. The 22kHz Chebyshev filter has attenuation of about 96dB at the Nyquist frequency. This is a very conservative antialiasing filter that guarantees aliasing will not occur even with strong input signals beyond the Nyquist frequency.

Figure 16 shows a 4096 point FFT of the converter's output while being driven by the LTC1563 at 20kHz. The FFT plot shows the fundamental 20kHz signal and the presence of some harmonics. The THD is –91.5dB and is dominated by the second harmonic at –92dB. The remaining harmonics are all well below the –100dB level. There are also some nonharmonically related spurs that are artifacts of the ADC. In the filter's passband, the noise level is slightly higher than the converter's. The peaking of the noise level at the cutoff frequency, mostly due to the high Q section, is a typical active filter characteristic. In the stopband, the noise level is essentially that of the converter. The end result is a SINAD Figure of 85dB, about 4dB less than the converter alone.

Conclusion

The LTC1563 continuous time, active RC lowpass filter is an economical, simple to use, yet versatile part that meets the high performance standards required in today's high resolution systems. Beyond ease of use, the part's design simplicity leads to ease of manufacture. This combination of features makes discrete lowpass filters and expensive, bulky filter modules obsolete. ◢T
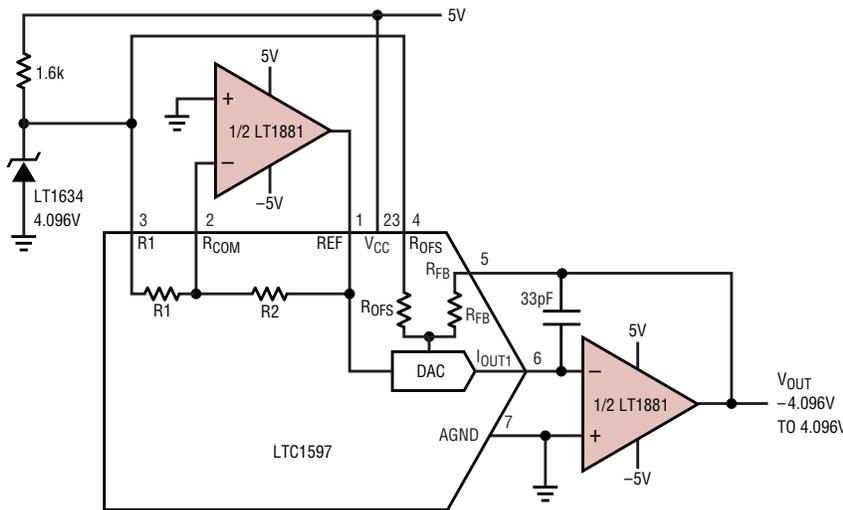
Figure 10. 16-bit voltage-output DAC on a ±5V supply

minimize the introduction of errors due to the amplifiers. This is especially important when operating the DAC at low supply voltages. An LSB of DAC output current is only 3nA. The low I_B of the LT1881 keeps this error to less than 0.2LSB of zero-scale offset.

Conclusion

Linear Technology's new rail-to-rail output precision operational amplifiers provide the proper amplifier for any low voltage, high precision application. The user must understand the requirements of the application, particularly the source impedance, to make the proper choice as to whether the LT1677, LT1881/LT1882 or LT1884/LT1885 is the best amplifier for a given application. ◢T

SOT-23 Switching Regulator with Integrated 1 Amp Switch Delivers High Current Outputs

by Albert Wu

The LT1930 is the only SOT-23 switching regulator in the industry that includes an integrated 1A switch. The LT1930 utilizes a constant frequency, internally compensated, current mode PWM architecture. Its 1.2MHz switching frequency allows the use of tiny, low cost capacitors and low profile inductors. With an input voltage range of 2.6V to 16V, the LT1930 is a good fit for a variety of applications. The onboard switch features a low V_{CESAT} voltage of 400mV at 1A, resulting in very good efficiency even at high load currents.

Figure 1 shows a typical 3.3V to 5V boost converter using the LT1930.

The circuit can provide an impressive output current of 480mA. The efficiency remains above 83% over a wide load current range of 60mA to 450mA, reaching 86% at 200mA. The maximum output voltage ripple of this circuit is $40mV_{P-P}$, which corresponds to less than 1% of the nominal 5V output. Figure 2 is an oscilloscope photograph of the transient response. The lower waveform represents a load step from 200mA to 300mA, the middle waveform shows the inductor current and the upper waveform shows the output voltage. The output voltage remains within 1% of the nominal value during the transient steps

and displays a well damped response with little ringing.

Another typical application is a 5V to 12V boost converter, as shown in Figure 3. This circuit can provide 300mA of output current with efficiencies as high as 87%. The maximum output voltage ripple of this circuit is $60mV_{P-P}$, which corresponds to 0.05% of the nominal 12V output. Figure 4 is an oscilloscope photograph of the transient response. The lower waveform shows a load current step from 200mA to 250mA. The middle waveform displays the inductor current and the upper waveform shows the output voltage. The
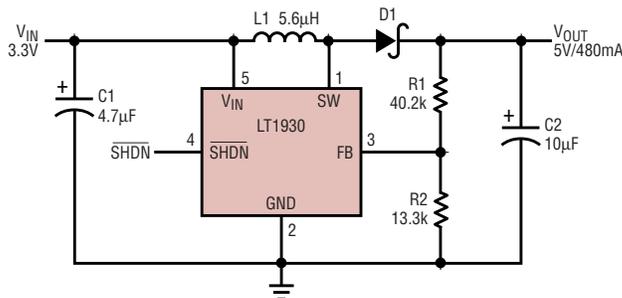
C1: TAIYO-YUDEN X5R JMK212BJ475MG (408) 573-4150
C2: TAIYO-YUDEN X5R JMK316BJ106ML
D1: ON SEMICONDUCTOR MBR0520 (800) 282-9855
L1: SUMIDA CR43-5R6 (847) 956-0666

Figure 1a. 3.3V to 5V/450mA step-up DC/DC converter
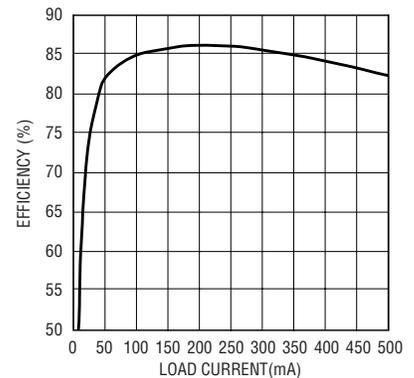
Figure 1b. Efficiency of Figure 1a's circuit

20µs/DIV
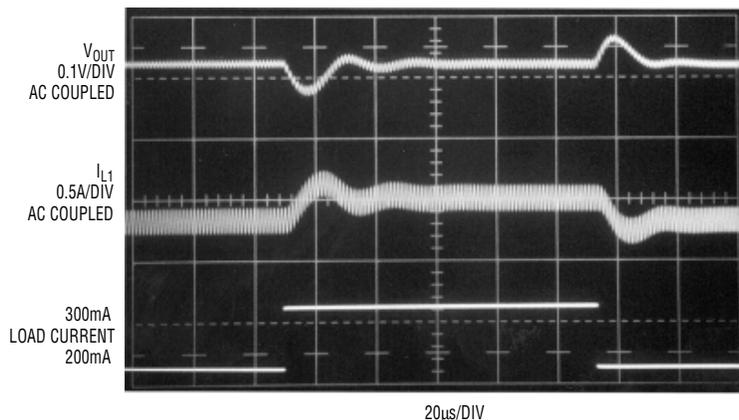
Figure 2. Transient response of Figure 1a's circuit

Dual Operational Amplifier Combines 16-Bit Precision with High Speed

by Kris Lokere

Introduction

The LT1469 is a dual operational amplifier that has been optimized for accuracy and speed in 16-bit systems. The amplifier settles in just 900ns to 150µV for a 10V step. The LT1469 also features the excellent DC specifications required for 16-bit designs. Input offset voltage is 125µV maximum, input bias current is 10nA maximum for the inverting input and minimum DC gain is 300V/mV. The LT1469 specifications are summarized in Table 1.

This article presents two applications of the LT1469 in 16-bit data-conversion systems. The first application is with a fast current-output digital-to-analog converter (DAC), such as the LTC1597. The dual LT1469 amplifier allows this DAC to operate in bipolar, 4-quadrant multiplying mode. The second application illustrates the use of this dual amplifier as a buffer for a differential analog-to-digital converter (ADC), such as the 333ksps LTC1604.

16-Bit 4-Quadrant DAC with 2.4µs Settling Time

The fastest, most precise way to achieve 16-bit digital-to-analog conversion is using a current-output DAC followed by a precision amplifier for current-to-voltage conversion. Figure 1 shows the LT1469 used in conjunction with the LTC1597 16-bit current-output DAC. The first amplifier is used as the current-to-voltage (I/V) converter at the output of the DAC. The second amplifier is used to invert the reference input voltage. All the resistors are internal to the DAC and precisely trimmed. With a fixed 10V reference input (such as could be provided by the LT1021-10), the reference inversion allows a bipolar output swing, that is, from –10V to 10V. In addition, because of the high bandwidth and low distortion of the LT1469, this configuration allows the reference input to be a variable signal, such as a sine wave, for full 4-quadrant multiplication operation. Figure 2 shows signal-to-(noise plus distortion) measurement results of this circuit.

The key AC specification of the circuit in Figure 1 is settling time, since this limits the DAC update rate. In an optimum configuration, the settling time of the LT1469 alone is a blistering 900ns. In Figure 1, settling time is limited by the need to compensate for the DAC output capacitance, which, for the LTC1597, varies from 70pF to 115pF, depending on the input code. This capacitance at the amplifier's inverting input combines with the internal feedback resistor to form a zero in the closed-loop frequency response in the vicinity of 100kHz–200kHz. Without a feedback capacitor, the circuit will oscillate. A 15pF feedback capacitor stabilizes the circuit by adding a pole at 880kHz. This 12kΩ||15pF feedback network increases the settling time. The theoretical minimum for the settling time to 16-bit accuracy for a 1st order linear system is $-\ln(2^{-16})$ = 11.1 time constants set by the 12kΩ and 15pF, which equals 2.0µs. Figure 1's circuit settles in 2.4µs to 150µV for a 20V step.

The important DC specifications of this bipolar DAC circuit are integral and differential nonlinearity (INL and DNL), zero error and gain error. The amplifiers contribute to these errors through their input offset voltage (V_{OS}), finite DC gain (A_{VOL}) and inverting input bias current (I_{B-}). Since both amplifiers have their positive inputs tied to ground, the noninverting input bias current does not add to any errors. With this key application in mind, the design of the LT1469 is optimized for a low I_{B-}.

Table 1. LT1469 specifications summary	
Parameter	**Value**
Input Offset Voltage	125µV (Max)
Inverting Input Bias Current	10nA (Max)
Noninverting Input Bias Current	40nA (Max)
DC Gain	300V/mV (Min)
CMRR	96dB (Min)
PSRR	100dB (Min)
Channel Separation	100dB (Min)
Input Noise Voltage	5nV/√Hz
Input Noise Current	0.6pA/√Hz
Gain Bandwidth	90MHz
Slew Rate	22V/µs
Settling Time (A_V = –1, 150µV, 10V Step)	900ns
Settling Time (with LTC1597, C_F = 15pF, 20V Step)	2.4µs
THD for $10V_{P-P}$, 100kHz	–96.5dB
Supply Current, V_S = ±15V (Per Amplifier)	5.2mA (Max)
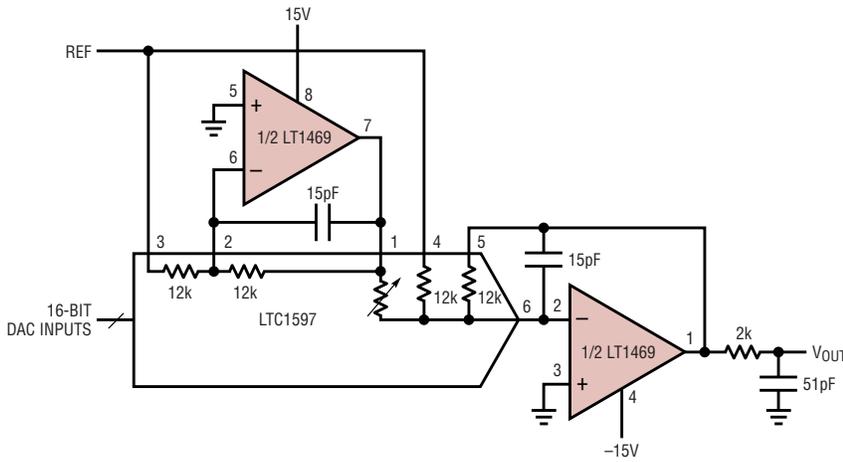
Figure 1. 16-bit DAC I/V converter and reference inverter

Figure 2. Signal to (noise plus distortion) for Figure 1's circuit (code = all zeros)

The INL and DNL of the LTC1597 are hardly affected by the surrounding amplifiers. Figure 3 shows measured results of INL better than 0.25LSB and DNL better than 0.1LSB, which is outstanding for 16-bit performance.

The effect of the amplifier's V_{OS}, I_{B-} and A_{VOL} on the system's zero error and gain error is a function of the noise gain and DAC resistance. The exact design equations have been presented in Linear Technology Design Note 214. For a –10V to 10V output swing, the LSB of this 16-bit system is $20V/2^{16} = 305\mu V$. Relative to this LSB, the LT1469 worst-case specifications lead to a zero error of 3.6LSB and a full-scale gain error of 4.9LSB. These numbers are insignificant compared to the inherent DAC specifications.

With its low $5nV/\sqrt{Hz}$ input voltage noise and $0.6pA/\sqrt{Hz}$ input current noise, the LT1469 contributes only an additional 23% to the DAC output noise voltage. The optional lowpass filter at the output allows the designer to trade off resolution for settling time. A lower cutoff frequency eliminates wideband noise, as shown in Figure 2, whereas a higher cutoff frequency, such as the 1.6MHz shown in Figure 1, contributes only 0.1µs to the settling time.

Single-Ended-to-Differential 16-Bit ADC Buffer

Figure 4 illustrates the use of the LT1469 as a buffer for the LTC1604 differential 16-bit ADC. The impor-

tant amplifier specifications for this application are low noise and low distortion. The LTC1604 16-bit ADC signal-to-noise ratio (SNR) of 90dB implies $56\mu V_{RMS}$ noise at the input. The noise of the two amplifiers and $100\Omega/3000pF$ lowpass filter is only $6.4\mu V_{RMS}$. The total noise includes a contribution from the source resistance. For a high value R_S of $10k\Omega$, this amounts to $11.8\mu V_{RMS}$. Clearly, both noise sources taken together are still well within the requirement for 16-bit precision.

An advantage of driving the LTC1604 differentially is that the signal swing at each input can be reduced, which reduces the distortion of both the ADC and the amplifier. For the ADC, a full-scale input means that $A_{IN}^{+} - A_{IN}^{-} = \pm2.5V$. In single-ended mode, with A_{IN}^{-} grounded, this means that A_{IN}^{+} must swing $\pm2.5V$. When driving both inputs differentially, each input must swing only half that amount, that is, $\pm1.25V$. The LTC1604 total harmonic distortion (THD) is a low –94dB at 100kHz. The buffer/filter combination alone has 2nd and 3rd harmonic distortion bet-
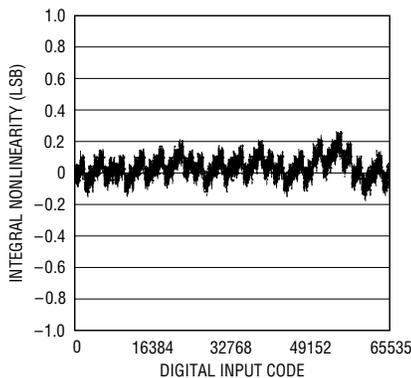
Figure 3a. INL for Figure 1's circuit
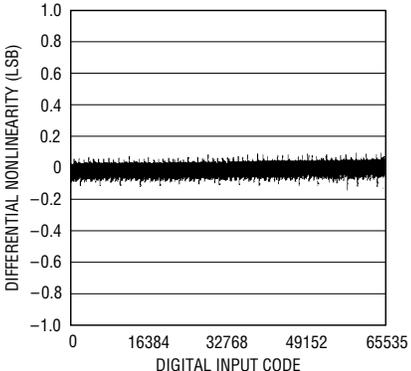
Figure 3b. DNL for Figure 1's circuit
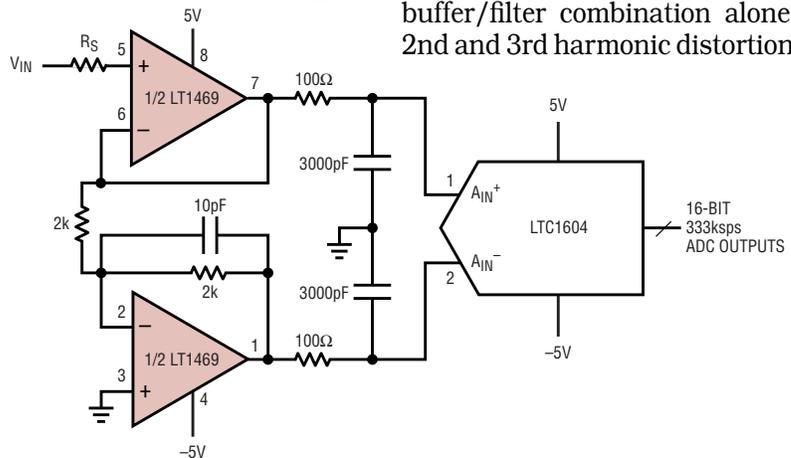
Figure 4. Differential ADC buffer

ter than –100dB for a ±1.25V, 100kHz input, so it does not degrade the AC performance of the ADC. Typical performance is shown in Figure 5.

Another advantage of operating in differential mode is that common mode errors of the ADC can be reduced. In single-ended mode, the ADC sees a common mode signal at its inputs that is one-half of the input signal. With the LTC1604's minimum CMRR of 68dB, this can result in significant gain and offset errors at the ADC output. In differential mode, only the LT1469 amplifiers see a common mode at their inputs, which results in negligible errors thanks to the 96dB CMRR of these amplifiers. The common mode signal at the ADC input is now always 0V.

The buffer also drives the ADC from a low source impedance. Without a buffer, the LTC1604 acquisition time increases with increasing source resistance above 100Ω and therefore the maximum sampling rate must be

Figure 5. 4096 point FFT of ADC output for Figure 4's circuit

reduced. With the low noise, low distortion LT1469 buffer, the ADC can be driven at the maximum speed from higher source impedances without sacrificing AC performance.

The DC requirements for the ADC buffer are relatively modest. The input offset voltage, CMRR and noninverting input bias current through the source resistance, R_S, affect the DC accuracy, but these errors are an

insignificant fraction of the ADC offset and full-scale errors.

Conclusion

The LT1469 provides two fast and accurate amplifiers in a single 8-lead SO or PDIP package. The unrivaled combination of speed and accuracy make it the component of choice for many 16-bit systems. *LT*

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C2: TAIYO-YUDEN X5R EMK316BJ475ML
D1: ON SEMICONDUCTOR MBR0520   (800) 282-9855
L1: SUMIDA CR43-100   (847) 956-0667

Figure 3a. 5V to 12V/300mA step-up DC/DC converter
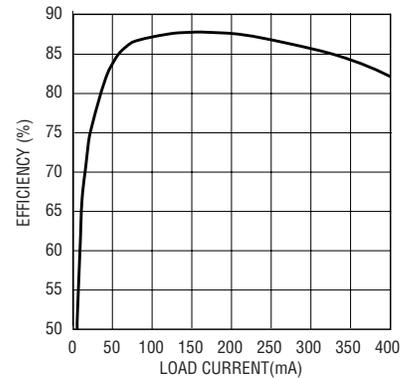
Figure 3b. Efficiency of Figure 3a's circuit

output voltage remains within 1% of the nominal value during both transient steps.

These applications demonstrate that the LT1930 is the industry's highest power SOT-23 switching regulator. In addition to step-up or boost converters, the LT1930 can be used in single-ended primary inductance converters (SEPIC) and flyback designs. The LT1930 is pin compatible with both the low power LT1613 and the micropower LT1615, providing a simple upgrade path for users of the older parts who need more power. *LT*

Figure 4. Transient response of Figure 3a's circuit

New Instrumentation Amplifier: Single-Resistor Gain Set and Precision Front End Make Accuracy Easy

by Glen Brisebois

The LT1168 is a low power, single-resistor gain-programmable instrumentation amplifier that is easy to apply. It is a pin-compatible upgrade for the AD620 (and the INA118 with a resistor-value change) and is available in C and I grades. With negligible 60µV (Max) offset voltage and ultra-high 1TΩ input impedance, it can sense bridges with source impedances from 10Ω to 100k without degrading the signal. Its 120dB CMRR at 60Hz ($A_V = 100V$) is achieved even with a 1k source impedance imbalance. Matching the LT1168's CMRR using discrete op amps would require the use of 0.001% resistors. The LT1168's robust inputs meet IEC1000-4-2 Level 4 ESD tests with the addition of two external 5k series resistors. These 5k resistors will contribute only a negligible 6µV of DC error.

Typical Application: Absolute Pressure Meter (Barometer)

Figure 1 shows just how easy it is to apply the LT1167. The LT1097, in conjunction with the LT1634-1.25 reference and R1, provides a precision current drive for the bridge. D1 ensures that the common mode input

range of the LT1097 is not exceeded over temperature. With the current drive and the sensor bridge in place, the rest of the circuit is composed entirely of the LT1167 and its gain-set resistor, R2. The sensor gives a full-scale output of 50mV (±1%) at 30psi (just over two atmospheres) with a 1.235V reference. With a 1.25V reference, the full-scale output value scales to 50.61mV. In order to get a convenient and easily read output of 100mV per 1psi, R2 should be chosen to set the gain to 3V/.05061V = 59.28. Or, with 2.036 inches of mercury equal to 1psi (referred to 39°F), change R2 to set a gain of 120.7 for a convenient output of 100mV per 1inHg. Or, again, with 6.8947kPascals equal to 1psi, set the gain to 408.7 for an output of 100mV per kiloPascal. The single-resistor gain adjustment makes

it easy to accommodate the desired units effortlessly.

Setting the Gain

The relation between the LT1168 gain and the gain-set resistor is given by the following equations: $R_G = 49.4k\Omega/(Gain - 1)$, and equivalently, Gain = $(49.4k\Omega/R_G) + 1$. In order to take advantage of the high CMRR without taking gain, simply do not connect an R_G. This configures the LT1168 as a precision, buffered, unity-gain difference amplifier. If precision gain is desired, use a 0.1% precision resistor in order not to degrade the 0.1% gain error specification of the LT1168. To target the desired gain exactly, pick a standard 0.1% value that is slightly smaller than required. Then, in order to "top up" the total R_G to the required value, use a small value standard 1% resistor in series, as shown in Figure 2. As long as the 1% resistor is a relatively small value, say 1/20 of the 0.1% value, the overall precision will not be degraded. Table 1 shows prac-

Table 1. Examples of series resistors for precision gain

Desired Gain	R_G (Theoretical)	R_{G1} 0.1%	R_{G2} 1% "Top-Up"	Resultant Gain
59.28	847.63Ω	845Ω	2.61Ω	59.28
102.69	412.72Ω	412Ω	1Ω	120.61
408.72	121.62Ω	121Ω	0Ω	409.62
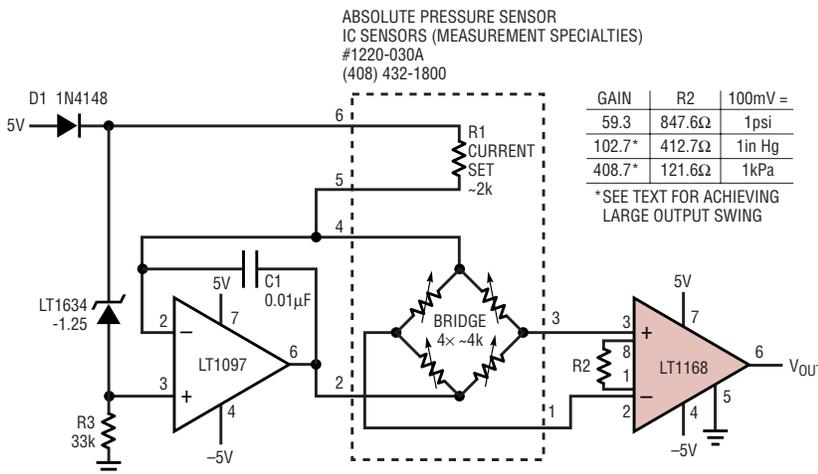
Figure 1. Simple barometer

R_{G1} = LARGER VALUE PRECISION RESISTOR
R_{G2} = SMALLER VALUE (A FEW OHMS) "TOP-UP" RESISTOR
$R_G = R_{G1} + R_{G2}$

$$GAIN = \frac{49,400\Omega}{R_G} + 1$$
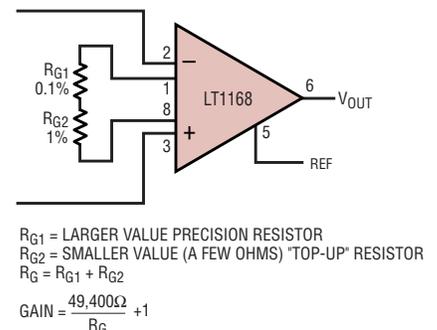
Figure 2. Targeting gain precisely
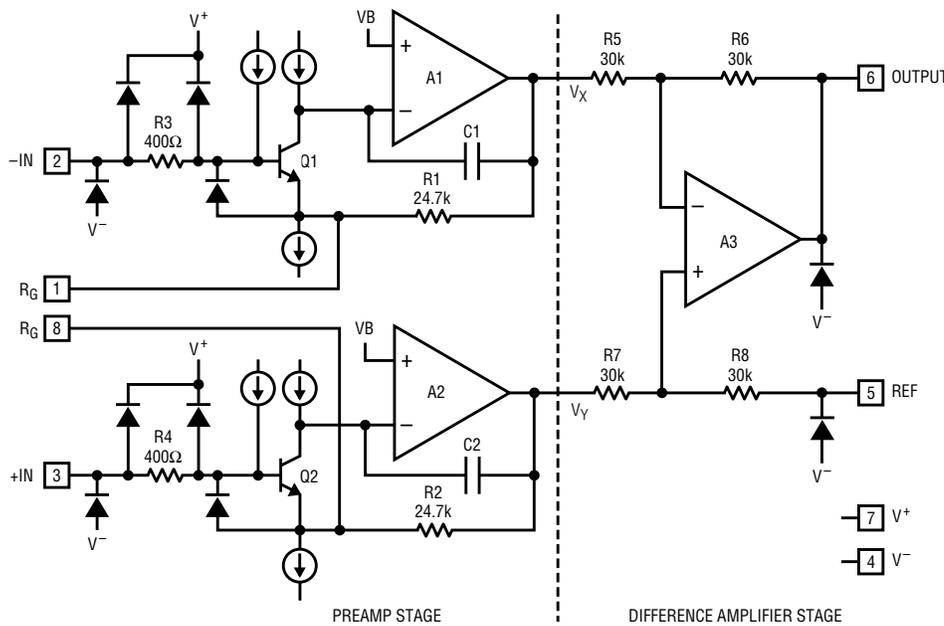
Figure 3. LT1168 block diagram

Figure 4. LT1168 gain vs frequency

AC Performance at Low Power

The LT1168 is not limited to DC and low frequency applications. Figures 4 and 5 show the frequency response and common mode rejection ratio of the LT1168 for various gains. The high frequency performance renders the LT1168 applicable in accelerometer and balanced audio line receiver applications, for example, in addition to the usual slower applications. This AC performance is achieved with a low supply-current budget of only 0.5mA.

Conclusion

The LT1168's precision front end and simple gain programmability make accuracy easy to achieve. The AC performance of the internal amplifier results in both extended differential mode bandwidth and excellent common mode rejection. Good common mode rejection is essential for extracting signals from a hostile world of interference. *LT*

tical resistor values for the gains specified above. Note that most transducers do not have 0.1% accurate sensitivity anyway, so most applications would use a 1% resistor and then perform a two-point calibration on the overall system.

Achieving Large Output Swings

Figure 3 shows the block diagram of the LT1168. Note that the last stage is a unity-gain difference amplifier. This means that the output voltage (across the Output and the Ref pins) will appear internal to the LT1168 across nodes Vx and Vy, centered around the common mode input voltage (minus one V_{BE}). In order to support full output swings, whether due to high applied gains or large differential inputs, the common mode input voltage should not be too close to either rail. For example, if the inputs are centered around ground and the Ref pin is grounded, then under excitation Vx and Vy will swing around ground (minus one V_{BE}) and the output swing will be limited by the normal output stage limitation of about 1.2V from either rail. However, if the common mode input voltage is at 10V on ±15V supplies, Vx and Vy will swing around 9.3V. In this case, the output swing will be limited by the outputs of

the intermediate amplifiers, A1 and A2, as they reach their upper limits about 1V from the rail. Thus, the final output swing in this case will be limited to ±4.6V even though the supplies are ±15V. With regard to the lower rail, if the common mode input voltage is at –10V on ±15V supplies, then V_X and V_Y will swing around –10.7V. The final output swing in this case will be limited to ±3.3V even though the supplies are ±15V.

As a rule of thumb, in order to achieve the full output swing, keep the common mode input voltage within the middle one-third of the supplies. For example, in the case of Figure 1, with gain = 408.7, the full-scale output voltage at 30psi (204.4kPa) would be 20.44V. Providing the LT1168 with +24V/–5V supplies and, given that the bridge section of the sensor typically has about 3V of excitation across it, replacing D1 with a 12V Zener diode will approximately center the common mode input voltage. This allows the LT1168 to achieve full 0V (vacuum) to 20.44V (204.4kPa, or about 2.2 atmospheres) output swing. For information on using the LT1168 on a single 5V supply, see "Designing the LT1167 Instrumentation Amplifier into a Single 5V Supply Application," in *Linear Technology* IX:2 (June 1999).

Figure 5. Common mode rejection ratio vs frequency (1k source imbalance)

SOT-23 SMBus Fan Speed Controller Extends Battery Life and Reduces Noise

by David Canny

Introduction

Battery run times for notebook computers and other portable devices can be improved and acoustic noise reduced by using Linear Technology's LTC1695 to optimize the operation of these products' internal cooling fans. The LTC1695 comes in a SOT-23 package and provides all the functions necessary for a system controller or microcontroller to regulate the speed of a typical 5V/≤1watt fan via a

Figure 2. Fan start-up voltage profile

2-wire SMBus interface. By varying the fan speed according to the system's instantaneous cooling requirements, the power consumption of the cooling fan is reduced and battery run times are improved. Acoustic noise is practically eliminated by operating the fan below maximum speed when the thermal environment permits. Designers also have the option of controlling the temperature in portable devices by using feedback from a temperature sensor to control the fan speed.

Figure 1 shows a typical application. Fan speed is easily programmed by sending a 6-bit digital code to the LTC1695 via the SMBus. This code is converted into an analog reference voltage that is used to regulate the output voltage of the LTC1695's internal linear regulator. The system controller can enable an optional boost feature that eliminates fan start-up problems by outputting 5V to the fan for 250ms before lowering the output voltage to its programmed value. Another important feature is that the system controller can read overcurrent and overtemperature fault conditions from information stored in the LTC1695. The part's SMBus Address is hard-wired internally as 1110 100 (MSB to LSB, A6 to A0) and the data code bits D0 to D6 are latched at the falling edge of the SMBus Data Acknowledge signal (D6 is a Boost-Start Enable bit and D5 to D0 translate to a linearly proportional output voltage, 00–3F hex = 0V–5V). The

Figure 1. SMBus fan-speed controller

LTC1709 Low Cost, High Efficiency 42A Converters with VID Control Reduce Input and Output Capacitors

by Wei Chen

Introduction

The LTC1709-8/LTC1709-9 are dual, current mode, PolyPhase™ controllers that drive two synchronous buck stages out of phase. This architecture reduces the number of input and output capacitors without increasing the switching frequency. The relatively low switching frequency and integrated high current MOSFET drivers help provide high power-conversion efficiency for low voltage, high current applications. Because of the output ripple current cancellation, lower value inductors can be used, resulting in a faster load transient response. This, plus the 5-bit VID table, makes these devices particularly attractive for CPU power supply applications. Two VID tables are available to comply with the VRM 8.4 (LTC1709-8) and VRM9.0 (LTC1709-9) specifications.

Design Example

Figure 1 shows the schematic diagram of a 42A power supply for the AMD Athlon microprocessor. With only one IC, eight tiny SO-8 MOS-FETs and two 1μH low profile, surface mount inductors, an efficiency of 86% is achieved for a 5V input and a 1.6V/42A output. Greater than 85% efficiency can be maintained throughout the load range of 3A–42A, as shown in Figure 2. Because of the low input voltage, the reverse recovery losses in the body diodes of the bottom MOSFETs are not significant. No Schottky diodes are required in parallel with the bottom MOSFETs in this application.
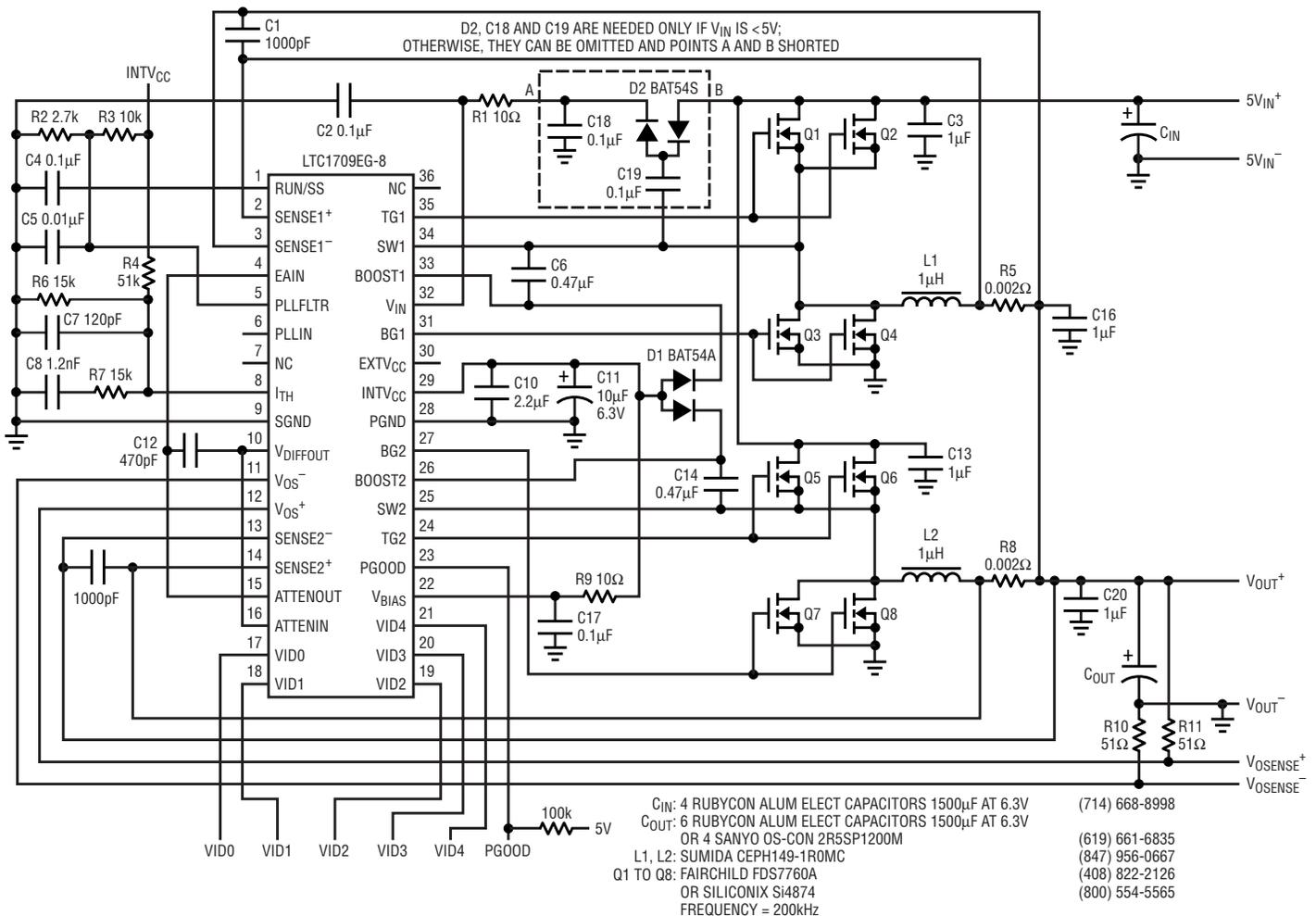
Figure 1. Schematic diagram of a 42A power supply using the LTC1709

Table 1. Comparison of input and output ripple current for single-phase and dual-phase configurations (L = 1μH, f_S = 200kHz)

Phases	Input Ripple Current (A$_{RMS}$)	Output Ripple Current (A$_{P-P}$)
1	19.7	10.9[1]
2	10.1	2.9

[1]Assumes that the single-phase circuit uses two 1.0μH/21A inductors in parallel to provide 42A output.

Table 1 compares the input and output ripple currents for single-phase and 2-phase configurations. A 2-phase converter reduces the input ripple current by 50% and the output ripple current by 75% compared to a single-phase design. The reduction in the cost and size of the input and output capacitors is significant.

Figure 3 shows the measured load transient waveform. The load current changes between 2A and 42A with a slew rate of about 30A/μs. Output capacitor type and size requirements are dominated by the total ESR of the output capacitor network. Six low cost aluminum electrolytic caps (Rubycon, 1500μF/6.3V) are needed on the
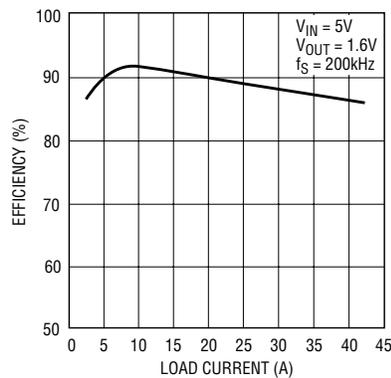
Figure 2. Efficiency vs load current for Figure 1's circuit

output to meet this requirement. The maximum output voltage variations during the load transients are less than 200mV$_{P-P}$. Active voltage positioning was employed in this design to keep the number of output capacitors at six (refer to Linear Technology Design Solutions 10 for more details on active voltage positioning). R4 and R6 provide the output voltage positioning with no loss of efficiency. If OSCON caps are used, four 1200μF/2.5V (2R51200M) capacitors will be sufficient.
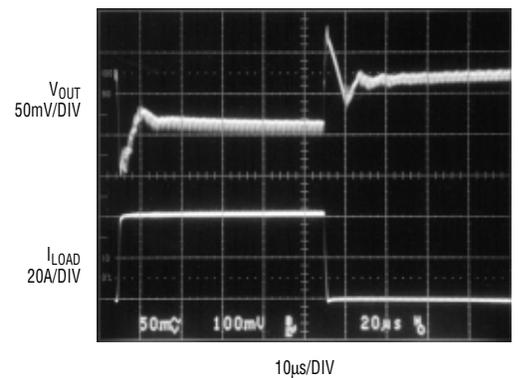
Figure 3. Load transient waveforms at 40A step and 30A/μs slew rate

Conclusion

The LTC1709 based, low voltage, high current power supply described above achieves high efficiency and small size simultaneously. The savings in the input and output capacitors, inductors and heat sinks help minimize the cost of the overall power supply. This LTC1709 circuit, with a few modifications, is also suitable for VRM9.0 applications. Refer to Linear Technology Application Note 77 for more information on the PolyPhase technique. *LT*

LTC1694, which also appears in Figure 1, is a dual SMBus accelerator/pull-up device that may be used in conjunction with the LTC1695.

Boost-Start Timer, Thermal Shutdown and Overcurrent Clamp Features

A DC fan typically requires a starting voltage higher than its minimum stall voltage. For example, a Micronel 5V fan requires a 3.5V starting voltage, but once started, it will run until its terminal voltage drops below 2.1V (its stall voltage). Thus, the user needs to ensure that the fan starts up properly before programming the fan voltage to a value lower than the starting voltage. Monitoring the fan's DC current for stall conditions does not help because some fans consume almost the same amount of current at the same terminal voltage in both stalled and operating conditions. Another approach is to detect the absence of

fan commutation ripple current. This, however, is complex and requires customization for the characteristics of specific brands of fans. The LTC1695 offers a simple and effective solution through the use of a boost-start timer. By setting the Boost-Start Enable bit high via the system controller, the LTC1695 outputs 5V for 250ms to the fan before lowering the voltage to its programmed value (see Figure 2 for the start-up voltage profile).

During a system controller Read command, bits 6 and 7 in the data byte code are defined as the Thermal Shutdown Status (THE) and the Overcurrent Fault (OCF), respectively. The rest of the data byte's register (bits 0 to 5) are set low during host read back. The LTC1695 shuts down its PMOS pass transistor and sets the THE bit high if die junction temperature exceeds 155°C. During an overcurrent fault, the LTC1695's overcurrent detector sets the OCF bit high and actively clamps the output cur-

rent to 330mA. This protects the LTC1695's PMOS pass transistor. Under dead short conditions (V$_{OUT}$ = 0), although the LTC1695 clamps the output current, the large amount of power dissipated on the chip will force the LTC1695 into thermal shutdown. These LTC1695 dual protection features protect the IC and the fan and, more importantly, alerts the host to system thermal management faults. During a fault condition, the SMBus logic continues to operate so that the host can poll the fault status data.

Conclusion

The LTC1695 improves battery run times and reduces acoustic noise in portable equipment. In addition, it provides important performance and protection features by controlling the operation of the equipment's cooling fan. It comes in a SOT-23 package and is easily programmed via the SMBus interface. *LT*

ADSL Line Driver Design Guide, Part 2

by Tim Regan

Part one of this article appeared in *Linear Technology* X:1 (February 2000) and is also available on the Linear Technology web site at www.lineartech.com/ezone/dsl.html. It discusses the different DSL standards, characteristics of the DSL signals, the design of differential drivers for DSL and the requirements for amplifiers used in this application.

Design Calculations, Volts, Amps and Power Dissipation

It is very important to consider the power requirements of the line driver in DSL applications. Although a nominal power level of 100mW$_{RMS}$ or less into a 100Ω load does not seem to be a lot of power, the driver must handle large peak signals and therefore requires a larger than nominal power supply voltage. This increases both the power dissipation in the driver package and the peak current capability needed from the power supply. This issue becomes most critical in central office designs, where many DSL ports are included on a single card powered from one supply. Additionally, the heat generated by the drivers must be handled properly to ensure reliable operation.

This section will provide the calculations necessary to determine the voltages, currents and power dissipation for an ADSL driver of either standard. It can be quite useful to place these equations in a spreadsheet to allow quick observation of the effect of different design variables on the overall system. Assuming that a wide band, low distortion driver has been selected (the LT1795 and LT1886 are excellent choices), the three most important system issues to consider are the total supply voltage, the peak output current and the driver power dissipation required.

For these calculations, the RMS voltages required are treated as DC levels for the purpose of estimating the power dissipation. In an actual DSL design this approach overestimates the typical power dissipation with a DMT signal by 10% to 20% because a data transmission is not always at the maximum output power level. The DSP intelligence built into the system automatically adjusts the transmitted power level and frequency spectrum for each connection made. With shorter phone-line loops, the transmitted power is reduced; with longer loops, not all of the channels are used and the number of data bits per channel is reduced. The maximum transmitted power is provided when the connection loop length is in the range of 4000 feet to 10,000 feet and there happens to be a significant level of noise interference and/or low line impedance conditions. Designing to handle the conservative estimate provides a margin of safety for reliable operation.

The Input Variables

Before a design can begin, the following information must be known: which DSL standard is to be used, Full Rate or G.Lite, whether upstream (CPE) or downstream (CO). These same equations apply for any DSL standard (HDSL and HDSL2 for example) with some changes to the input parameters (see Table 1).

	Table 1. Input variables		

Symbol	Parameter	Description	Typical Values for ADSL
P$_{LINE}$ (dBm)	Line Power	RMS power to be put on the line	20dBm (Full Rate, CO)
			16.3dBm (G.Lite, CO)
			13dBm (Full Rate and G.Lite, CPE)
PAR	Crest Factor	Peak-to-average ratio for the DMT signal	5.3
Z$_{LINE}$	Line Impedance	Characteristic impedance of the line	100Ω
n	Turns Ratio	The turns ratio of the line coupling transformer	1:1 or higher
P$_{LOSS}$ (dBm)	Insertion loss	The power loss of the transformer being used	0.2dBm to 2dBm
V$_{HR}$	Headroom Voltage	A function of the output saturation voltages (positive and negative swing) of the driver used. Headroom is twice the larger of the two saturation voltages.	2V to 5V
I$_Q$	Quiescent Current	Total quiescent (no input signal) supply current of the driver that is not diverted to the load.	10mA to 30mA
e$_{IN}$	Input Voltage	Maximum peak-to-peak differential input voltage from the AFE (analog front end)	1.5V to 4.5V$_{P-P}$

Basic System Requirements

The following equations determine the essential operating requirements independent of the driver amplifier used in the design:

Line Power in Watts:

$$P_{LINE(W)} = 10^{\frac{P_{LINE(dBm)}}{10}} \bullet 1mW \qquad (1)$$

example: 20dBm = 100mW.

RMS Line voltage:

$$e_{LINE(RMS)} = \sqrt{P_{LINE(W)} \bullet Z_{LINE}} \qquad (2)$$

Power to the primary of the transformer:

$$P_{PRI(dBm)} = P_{LINE(dBm)} + P_{LOSS(dBm)} \qquad (3)$$

$$P_{PRI(W)} = 10^{\frac{P_{PRI(dBm)}}{10}} \bullet 1mW$$

Impedance of primary of the transformer:

$$Z_{PRI} = \frac{Z_{LINE}}{n^2} \qquad (4)$$

Transformer termination resistors:

$$R_{BT1}, R_{BT2} = \frac{Z_{PRI}}{2} \qquad (5)$$

Primary RMS voltage:

$$e_{PRI(RMS)} = \sqrt{P_{PRI(W)} \bullet Z_{PRI}} \qquad (6)$$

Transformer primary RMS current:

$$I_{PRI(RMS)} = \frac{e_{PRI(RMS)}}{Z_{PRI}} \qquad (7)$$

Driver amplifier RMS output voltage:

$$e_{AMPLIFIER(RMS)} = \qquad (8)$$
$$\left(\frac{Z_{PRI} + (2 \bullet R_{BT})}{Z_{PRI}} \right) \bullet e_{PRI(RMS)}$$

This is the RMS voltage between the two amplifier outputs. If the R_{BT} resistors are properly sized this voltage is twice the RMS voltage of the transformer primary.

Peak driver amplifier output current:

$$I_{PEAK} = \frac{E_{PRI(RMS)} \bullet PAR}{Z_{PRI}} \qquad (9)$$
$$= I_{PRI(RMS)} \bullet PAR$$

The peak current handling capability is key to selecting the driver amplifiers.
Power supplied by the driver amplifiers:

$$P_{OUT} = e_{AMPLIFIERS(RMS)} \bullet I_{PRI(RMS)} \qquad (10)$$

Overall line driver voltage gain:

$$A_{V(TOTAL)} = \frac{e_{LINE(RMS)} \bullet 2 \bullet PAR}{e_{IN}} \qquad (11)$$

Differential amplifier voltage gain:

$$A_{VDIFF(AMPLIFIERS)} = \qquad (12)$$
$$\frac{e_{AMPLIFIERS(RMS)} \bullet 2 \bullet PAR}{e_{IN}}$$

The turns ratio of the transformer used is critical to the overall design. Figure 1 illustrates the minimum total supply voltage across the driver and the peak driver output current required as a function of the turns ratio. These are the absolute minimum requirements based on an ideal amplifier that has 0V headroom and is therefore able to swing fully to either supply voltage rail, and an ideal transformer, with zero insertion power loss. A practical implementation will require a larger supply voltage, as

determined from the next section. Trying to design a system with less supply voltage or current capability using conventional transformer termination resistors will result in clipping and transmission data errors.

Figure 1 also compares the different ADSL standards with the central office, downstream, Full Rate ADSL, which requires the most current and voltage. The reduced line power requirements for the downstream G.Lite and the upstream Full Rate and G.Lite modems produce designs with lower voltage and current requirements.

Important Driver Characteristics: Headroom Voltage and Quiescent Current

To determine the required supply voltage, power consumption and power dissipation of the driver, the headroom voltage and required quiescent current of the driver amplifier must be considered.

Minimum total supply voltage for the amplifiers:

$$V_{SUPPLY(MIN)} = E_{AMPLIFIER(RMS)} \qquad (13)$$
$$\bullet PAR + V_{HR}$$

The actual supply voltage for the driver amplifier must be set above the minimum peak-to-peak amplifier output swing to provide for the headroom voltage to prevent peak signal clipping. Using a supply voltage greater than this minimum value will increase the power dissipation in the driver amplifiers.
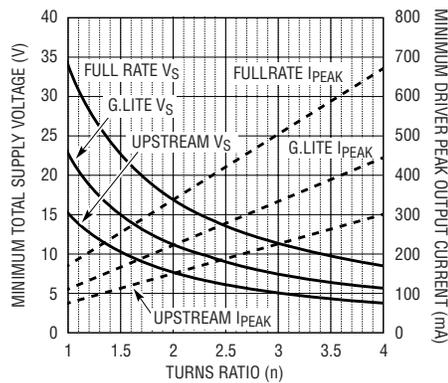
Figure 1. Minimum peak-to-peak driver output voltage and peak output current required, ideal amplifier and transformer
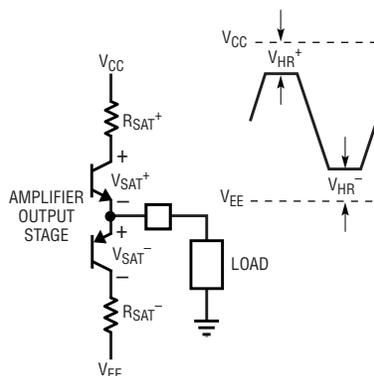
Figure 2. Typical output stage model and common data sheet curves are used to determine amplifier headroom voltage

$I_Q = I_{SUPPLY}^+ - I_{LOAD}$
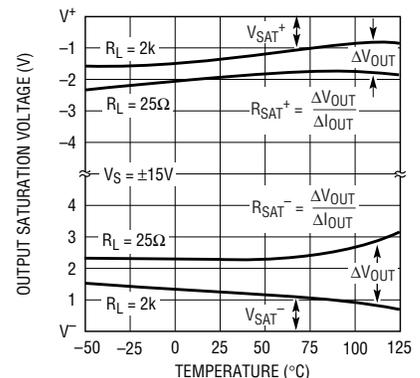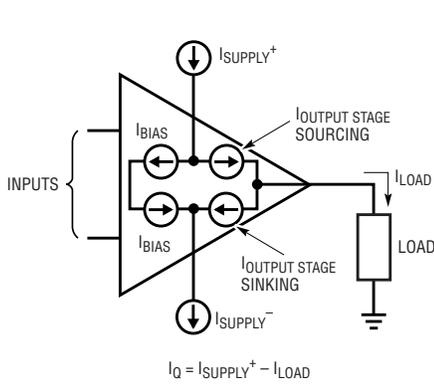
Figure 3. Much of an amplifier's quiescent current is transferred to the load current

The headroom voltage of an amplifier is determined from either the guaranteed specification for output voltage swing or from characteristic curves showing output saturation voltage vs output current or vs temperature with different load currents. The headroom voltage is the difference between the supply voltage rail and the maximum output voltage swing, both positive and negative, for a given load current. Figure 2 shows a simple model for determining an amplifier's output saturation voltages and an example of a useful data sheet curve.

During large signal transients, the transistors in the output stage of the amplifier will fully turn on to pull the output as close as possible to the supply voltage rails. The limitation on how close the signal can swing can be modeled as a fixed voltage drop across the transistor being driven with a resistance in series. This resistance increases the voltage swing limitation in proportion to the amount of load current the transistor must source or sink. The combined total of the fixed voltage drop and the voltage across the resistor is called the output saturation voltage. The values to use to model this characteristic can be determined from a data sheet curve. Figure 2 shows the curve that appears on the LT1795 data sheet.

This curve shows the positive and negative amplifier saturation voltages vs junction temperature with two different values of load resistance. DSL line drivers typically run warm, so the area of interest on the curve will be in the range of junction temperature
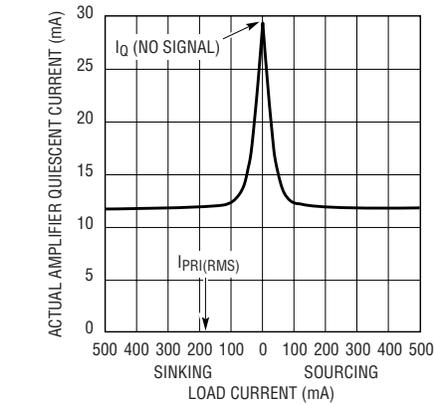
around 50°C. To determine the fixed voltage part of the model for the positive output swing, V_{SAT}^+, evaluate the top curve with R_L = 2k. From the curve it can be seen that the output will swing to within 1.2V of the positive supply. Because the curve was generated using supplies of ±15V, the load current at 50°C is only 13.8V/2kΩ or 7mA. To determine the value for the series resistance in the model, determine the change in output saturation voltage with a change in load current. At the same 50°C junction temperature point, evaluate the upper curve with R_L = 25Ω. With this load the output swings to within 1.8V of the positive rail and the load current is 13.2V/25Ω or 528mA. The series resistance is then $\Delta V_{SAT}/\Delta I_{OUT}$ (0.6V/521mA), which is 1.15Ω. From these values, the positive amplifier saturation voltage will be 1.2V + 1.15Ω • I_{PEAK} where the value of I_{PEAK} depends on the particular modem design. Applying the same approach for the amplifier swing towards the negative rail results in saturation voltage model parameters of 1.2V in series with a resistance of 2.2Ω.

With these values modeling the output saturation characteristics of the LT1795, at any level of peak output current the output stage will saturate or clip when swinging towards the negative supply before it will clip on the positive swing, due to the higher effective series resistance voltage drop. Transmission errors can occur if either output swing excursion clips, so when sizing the total supply voltage requirement for the driver the total headroom voltage of

the amplifier, V_{HR}, should be twice the larger of the two output saturation voltages. This will ensure that the output will not clip at all during maximum peak signal conditions.

With V_{SUPPLY} set large enough to prevent signal clipping the total power consumption from the supplies can be determined with Equation 14:

Power consumption of the complete line driver:

$$P_{IN} = V_{SUPPLY} \bullet (I_Q + I_{PRI(RMS)}) \qquad (14)$$
$$= (V_{EXTRA} + V_{HR} + V_{AMPLIFIER(RMS)} \bullet PAR)$$
$$\bullet (I_Q + I_{PRI(RMS)})$$

This equation introduces two new terms, V_{EXTRA} and I_Q. V_{EXTRA} is the total additional power supply voltage above $V_{SUPPLY(MIN)}$ that is actually used to power the driver amplifiers. For example, if the minimum total supply voltage for a design is determined to be 20V (or ±10V) but the actual supplies available are ±12V, then the V_{EXTRA} term will be 24V – 20V or 4V. The total power consumption of each line driver is very important when sizing the power supply for both voltage and current capability to be used in the system. This becomes most significant when multiple DSL ports are to be powered from a predesigned power supply. The power supply could become the limiting factor to the number of ports allowable.

The quiescent current, I_Q, is basically the operating supply current of the driver amplifiers. This is the cur-

ASSUMPTIONS

	FULL RATE	G.LITE	CPE
I_Q	28mA	18mA	14mA
V_{HR}	3V	2.5V	2V
P_{LOSS}	0.5dBm	0.5dBm	0.5dBm
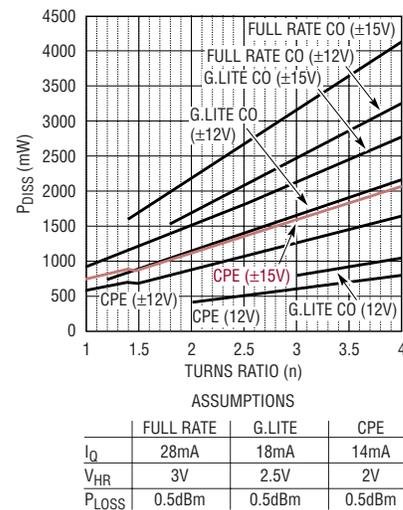
Figure 4. Driver power dissipation vs turns ratio: a practical implementation

rent required to bias the internal circuitry of the amplifiers. In general, high speed, high output current amplifiers that process signals with very low distortion require significantly more operating current than general-purpose amplifiers. This current adds to the power consumption and power dissipation of the driver package, because it must always be supplied whether there is signal applied or not. However, the power dissipation in the driver for the quiescent current is not just a fixed DC power of $I_Q \cdot V_{SUPPLY}$. As seen in Figure 3, much of the quiescent current is diverted to the amplifier output stage and becomes part of the load current while processing a signal. The curve shown is again for the LT1795 driver. With no load, all of the 30mA quiescent current flows from the positive supply through the amplifier to the negative supply. However, when the load is sourcing or sinking 500mA, only 12mA flows through the amplifier, the remaining 18mA is taken by the output stage and diverted to become part of the load current. To obtain an accurate estimate of the average power dissipation of the drivers, this sharing of the quiescent current should be taken into account. This will prevent overdesign of the thermal management area of concern. The I_Q term in Equation 14 should be the only current that continues to flow through the amplifier at the load current level of $I_{PRI(RMS)}$. The diverted quiescent current is included in the $I_{PRI(RMS)}$ term.

Unfortunately, this curve of quiescent operating current vs load current is not found on typical data sheets. Some characterization of the chosen amplifier should be done. The design of amplifier power output stages is varied and has a direct effect on the diversion of the total supplied operating quiescent current.

Power dissipated in the line driver amplifiers:

$$P_{AMPLIFIERS} = P_{IN} - P_{OUT} \qquad (15)$$
$$= e_{AMPLIFIERS(RMS)} \cdot [PAR \cdot I_Q + I_{PRI(RMS)}$$
$$\cdot (PAR - 1)] + (V_{HR} + V_{EXTRA}) \cdot$$
$$(I_Q + I_{PRI(RMS)})$$

The power dissipated in the driver package is important to consider when addressing heat management issues.

To minimize power dissipation, the driver should be powered from a power supply with voltages set to the minimum required. Most implementations, however, use existing power supply voltages, typically ±15V, ±12V or just the 12V rail for the line driver/receiver. Figure 4 provides an indication of the actual power dissipation in the line-driver amplifier package with commonly available supply voltages and a range of transformer turns ratios. This is a practical example where values have been assumed for the amplifier headroom and quiescent current and some transformer power loss. The lower power upstream modems require less operating current, which helps to minimize the package power dissipation. If the turns ratio is too low for the given supply voltage, the lines on the graph terminate because the supply voltage is not large enough to prevent clipping of the DMT signal peaks.

As previously stated, the power dissipation in the driver is an important concern as it generates heat in the system. For each of the ADSL standards, a certain minimum amount of power dissipation is required. Three factors that add to this power dissipation are the amplifier headroom voltage, the amplifier quiescent operating current and the power loss of the line-coupling transformer. Attention to these three factors when selecting an amplifier and transformer can optimize the overall power dissipation. Analysis of the sensitivities of the amplifier power dissipation (see Equation 15) for each of these three terms is summarized in Table 2. This shows the effect on total package dissipation for each factor taken individually with the other two factors set to zero. The term *n* is the transformer turns ratio.

The factors in Table 2 provide a rough indication of the additional power dissipation from these three system variables. The combined effect on power dissipation from I_Q, V_{HR} and P_{LOSS} must still be determined from Equation 15.

Optimizing Power Dissipation, Adjustable Quiescent Current and Shutdown

Several high speed power amplifiers from Linear Technology provide the ability to externally set the operating quiescent current. For the design of any of the DSL standards, this allows for fine tuning the amplifier's

Table 2. Additional power dissipation factors

Standard	ADSL Full Rate Downstream	G.Lite Downstream	Full Rate and G.Lite Upstream	Additional Power Dissipation
Minimum Power Dissipation, P_{MIN}	860mW	367mW	172mW	
Amplifier Quiescent Current, I_Q	33.5mW/n	22.14mW/n	15mW/n	Per 1mA of I_Q, P_{DISS} = (FACTOR) $\cdot$ (I_Q/1mA)
Total Amplifier Headroom Voltage, V_{HR}	n $\cdot$ 31.6mW	n $\cdot$ 20.9mW	n $\cdot$ 14.1mW	Per 1V of V_{HR}, P_{DISS} = (FACTOR) $\cdot$ (V_{HR}/1V)
Transformer Insertion Loss, P_{LOSS} in dBm	2.3%	2.3%	2.3%	Per 0.1dBm of P_{LOSS}, P_{DISS} = $P_{MIN} \cdot 1.023 \cdot \left(\frac{P_{LOSS(dBm)}}{0.1dBm} - 1 \right)$

operating point for minimum power dissipation and adequate distortion performance. There is a direct trade-off between the two, however. Designing for very low quiescent current significantly reduces the power dissipation, but obtaining the lowest distortion performance requires additional biasing current for the internal amplifier circuitry. Figure 5 illustrates the adjustability of the operating current for the LT1795. An internal current source is programmed via a single external resistor. The current through this source is mirrored and scaled up to become the biasing current for the two amplifiers. Also shown in Figure 5 is the effect of adjusting the operating current on distortion. The spectrum analyzer plots show the intermodulation components from twenty carrier tones (from 200kHz to 500kHz). With too low of an operating current, the signal on the line is far too distorted and interference with other channels is inevitable. However turning up the current drops all of the distortion products into the noise floor. This adjustment should be made during the evaluation of the driver under actual transmission conditions and optimized for the highest data rates obtainable.

The best power and thermal management technique in multiple-port systems or energy efficient stand-alone modem designs is to shut off the driver when the line is inactive. The digital circuitry always knows
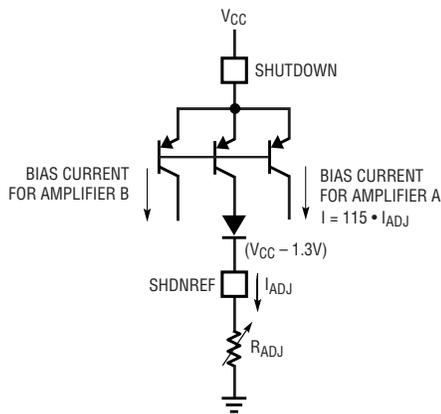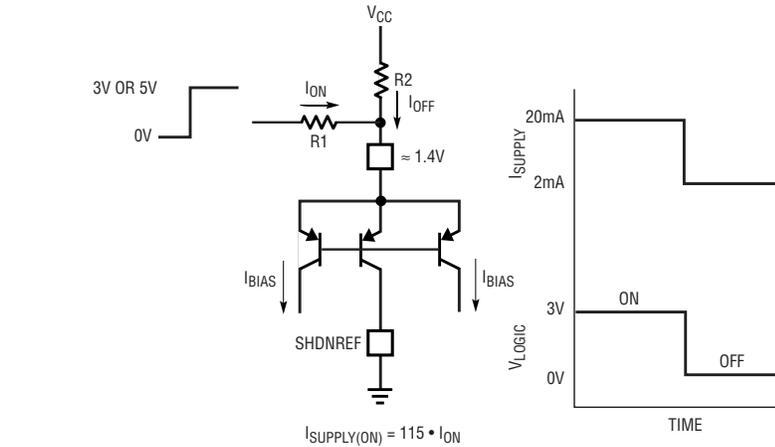
Figure 6. How to reduce driver supply current in an idle channel while maintaining the receiver function

when there is no data transmission activity and can issue a signal to the driver to shut down operation. Many drivers accept this control signal and completely power down the internal circuitry. The LT1795, for example, can be shut down to consume less than 200µA of current when not required to transmit data. When commanded to power up, the driver requires only a few microseconds to reestablish full performance, an insignificant time when compared to a typical communication training-up interval. When powered down, however, the output stage of the amplifier loses all bias and enters a high impedance state. This essentially opens the connection to the transformer back-termination resistors. As these resistors are often used to sense the received signal from the line, no signal can be developed across them if they are left floating.

Figure 6 illustrates a power saving function, called partial shutdown, that

keeps the amplifier slightly biased and thus allows the modem to continue to monitor the line for transmission signals to be received. Here, two resistors are carefully chosen to control the amount of operating quiescent current as well as to retain a small amount of "keep-alive" current when shut down. Resistor scaling can accommodate a direct connection to an I/O pin from the DSP processor with any logic voltage level. Shutting down to a quiescent current level of 2mA keeps the output stage active and terminates the received signal sensing resistors, resulting in a better than 10-to-1 reduction in idle-channel power consumption and dissipation.

Thermal Management

Depending on the ADSL standard being applied, the power supplies and the transformer turns ratio used, the driver amplifier package will dissipate somewhere between 500mW and 2W. The average power dissipation

Figure 5a. Proper adjustment of the operating current minimizes spectral components, adjusting the sujpply current
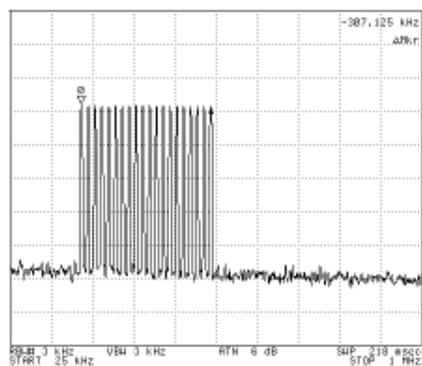
Figure 5b. Spectrum of 20 carrier tones with I_9 of 12mA/amplifier
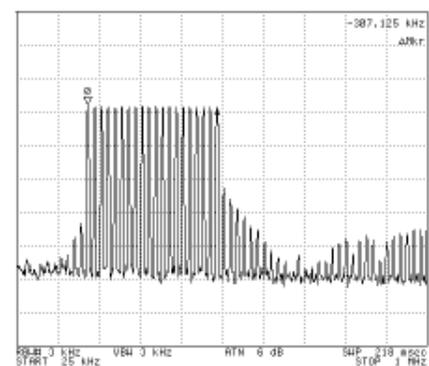
Figure 5c. Spectrum of 20 carrier tones with I_9 of 2.2mA/amplifier
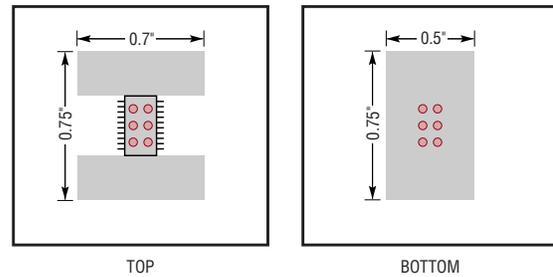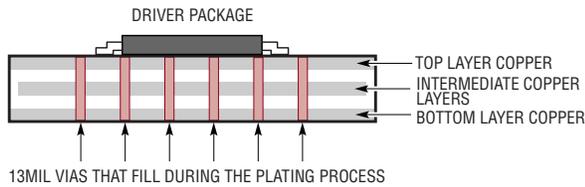
Figure 7a. Using PCB copper foil for heat sinking
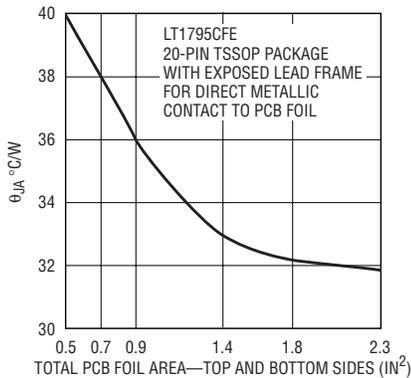
Figure 7b. Improving Heat dissipation with increased copper foil area

times the overall thermal resistance from the junction of the driver to the ambient air will determine the rise in operating junction temperature above the maximum ambient temperature. Most power amplifiers have a built in thermal protection mechanism that will disable the output stage when the junction temperature exceeds typically 160°C. Should this temperature ever be reached, the amplifier will protect itself, but data transmission errors will abound and most likely result in a data transmission disconnect. Designing a heat-spreading system to limit the driver junction temperature to less than 125°C at the highest expected ambient temperature will ensure continuous operation.

Fortunately, the power dissipation levels are not so high that external heat sinks are necessarily required, so heat spreading can usually be managed through planes of PCB copper foil. In addition, the packaging of most power amplifiers uses thermal conduction enhancements, such as fused or exposed lead frames. Fused lead frames have several package pins connected directly to the metal pad where the IC is attached. This pro-

vides a continuous path for heat transfer from the junction of the IC, out of the plastic encapsulation, to pins that are directly connected to PCB copper planes. An exposed lead frame does not plastic encapsulate the underside metal where the IC is attached. This provides a metal pad that can be connected directly to PCB copper for direct transfer of heat from the IC mounting junction heat source to the ambient air. An exposed lead frame allows for very small packages, such as that used for the LT1795CFE, a 20-pin TSSOP, to have thermal conductivity characteristics similar to much larger sized packages. Very small packages with good thermal conductivity can result in very dense multiport ADSL systems for central office applications.

The best way to spread the heat generated by the driver is to use as many planes of copper as are available and to "stitch" them together through small vias from the topside of the board to the bottom, as shown in Figure 7. These vias should be small enough in diameter (15 mils or less) that they are completely filled with solder during the plating process. This provides a continuous thermal conductivity path from the top of the board to the bottom for the most exposure to the ambient environment. There are no fixed rules for determining the lateral area of the copper planes on the PCB, other than "bigger is better," and 2oz copper is a thicker and therefore better thermal conductor than 1oz copper. Figure 7 also provides an indication of the improvement in the heat spreading thermal resistance from junction to case with various amounts of copper foil area on the top and bottom sides of a PCB.

As most of the heat is dissipated in the area immediately surrounding the driver amplifier package, there comes a point of diminishing returns where more copper area does not provide much additional benefit. This can be seen in the plot of thermal resistance in Figure 7 where, beyond a total PCB area of 1in^2, further reduction in thermal resistance is minimal. One word of caution regarding PCB planes for heat spreading is that the fiberglass material (typically FR-4) is a fairly good thermal insulator. Any component interconnect traces that cut through the plane of copper significantly reduce the effectiveness of the lateral area. Interconnect traces should be made on the inner layers of multilayer boards to minimize the distance between components. The complex interconnect of the logic circuits used in DSL modems usually requires a multilayer PC board that can be put to good use in the line driver area.

Another measure that can be taken is to provide some forced airflow cooling. A linear flow of air across the driver package can significantly reduce the effective thermal resistance from junction to ambient (θ_{JA}) of the heat-spreading system. A reduction of 2°C/W to 3°C/W for each 100lfpm (linear feet per minute) can
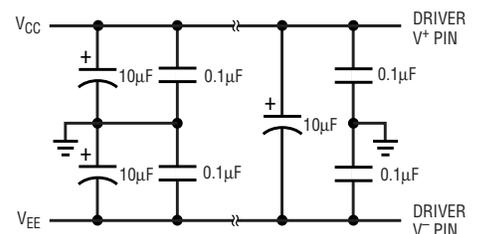
Figure 8. Recommended power supply bypassing for any design

be achieved. This is particularly important in a multiport system housed in an enclosed case.

A Gallery of Design Recommendations

This section will provide examples of driver and receiver circuits for each of the ADSL standards. These circuits provide a good starting point for implementing the line interface functions for a DSL modem. The circuits were designed with all of the considerations mentioned so far, but other system variables, such as available supply voltages or AFE output and input dynamic range, could mandate some modifications. The total voltage gain of each line-driver design, from the differential input voltage to the actual voltage output to the phone line, has been scaled to a value that requires less than $3V_{P-P}$ from the AFE providing the transmitted signal. The gain of the amplifier stage is adjusted to take into account the signal boost of the transformer used as well as the signal loss through the back-termination resistors.

Common to all of the designs is a good power supply bypassing approach. This is shown in Figure 8. A large- and a small-valued bypass capacitor at the points where the supplies connect to the board provide decoupling of noise and ripple over a wide frequency range. Additional high frequency decoupling at the driver and receiver supply pins is recommended. Another large-valued bypass capacitor connected directly between the supply pins of the driver helps to reduce the 2nd harmonic component of ripple on the supply lines. This component comes from the peak current demands from each supply, which occur twice for each input signal cycle due to the differential amplifier topology (each amplifier sources and sinks the peak current once each signal cycle).

The Differential Receiver

Not all DSL modems will require a receiver circuit. Some analog front end ICs have sophisticated circuitry for a very wide dynamic input range
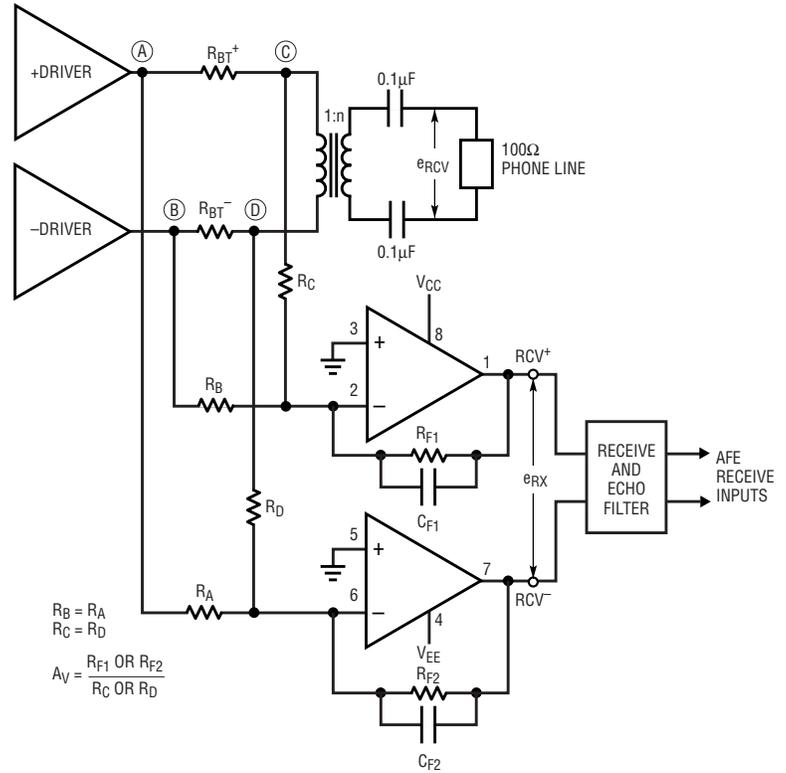
Figure 9. Basic differential receiver (4-wire to 2-wire)

to directly pick the small received signals out of the noise floor after passing through the receive/echo filter. Other designs may use a second transformer to process the differential received signal directly to the filter/AFE. Many designs still prefer to sense the differential signal across the termination resistors and provide gain to the received signal before passing it through the filter to the AFE. This basic differential receiver circuit
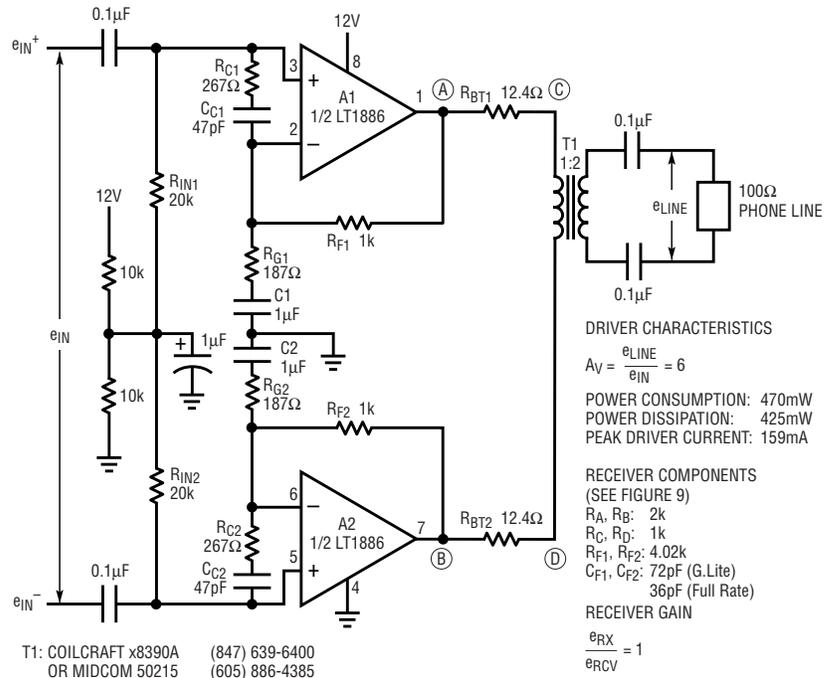
Figure 10. Full Rate or G.Lite upstream (CPE) driver
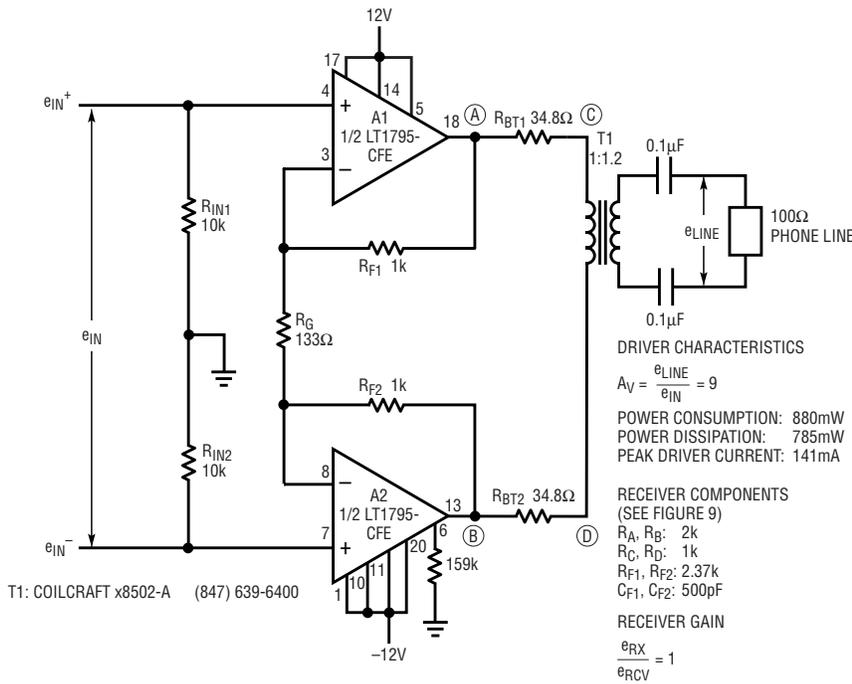
Figure 11. ADSL G.Lite downstream (CO) line driver

be set to exactly twice the value of resistors R_C and R_D.

The gain of the receiver is simply the inverting gain of the received signal path, R_{F1}/R_C and R_{F2}/R_D. In the driver design examples to follow, the receiver input resistors connect to the driver at nodes A through D. The recommended component values for the receiver provide for unity gain from the received signal appearing at the line to the differential receiver output. This takes into account the attenuation of the line-coupling transformer. A small feedback capacitor is also shown that reduces the gain at a frequency just above the received signal bandwidth, which varies depending on the application.

ADSL Full Rate or G.Lite Upstream (CPE) Line Driver

This driver (Figure 10) is the lowest powered of the ADSL standards, consuming less than 500mW. The lower line power, 13dBm, and resulting lower peak current requirement allows the use of the LT1886, which is a high speed 200mA dual amplifier. The use of a 2:1 transformer turns ratio allows this driver to be powered from a single 12V power supply.

In order to obtain the highest open-loop gain and bandwidth to minimize distortion, the LT1886 is decompensated and is only stable with closed-loop gains of ten or greater. In this design the signal gain of each amplifier is only 6.35. To remain stable with this low value of gain requires the addition of gain-compensation components R_{C1}, C_{C1}, R_{C2} and C_{C2}. These components, which come into play only at frequencies greater than 15MHz, parallel the gain-setting resistances, R_{G1} and R_{G2}, to make the feedback factor of each amplifier a value of 0.9, which is the same as having a closed-loop gain of ten; thus, stability is ensured.

The LT1886 is a 700MHz gain bandwidth amplifier. The combination of gain at such high frequencies and not being unity gain stable requires that the gain-setting resistors be returned to a low impedance at all frequencies. For this reason, the two gain setting

is shown in Figure 9. Each receiver amplifier is a summing stage that sums the received signal and the attenuated transmitted signal seen at the primary of the transformer with a weighted, opposite-phase transmitted signal. This weighted summing of the transmitted signal ideally cancels the 180° out-of-phase signals, leaving only the received signal at the differential amplifier outputs. This is called local echo cancellation. In a standard line-driver design, the transmit signals at nodes A and B in Figure 9 are twice the magnitude of the signals at nodes C and D. To cancel these signals in the receiver requires resistors R_A and R_B
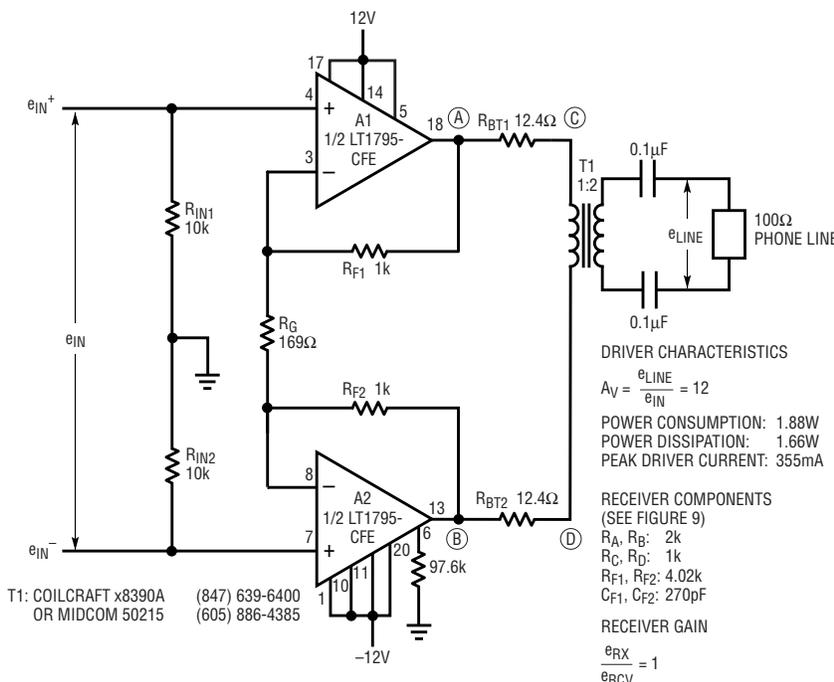
Figure 12 ADSL Full Rate downstream (CO) line driver
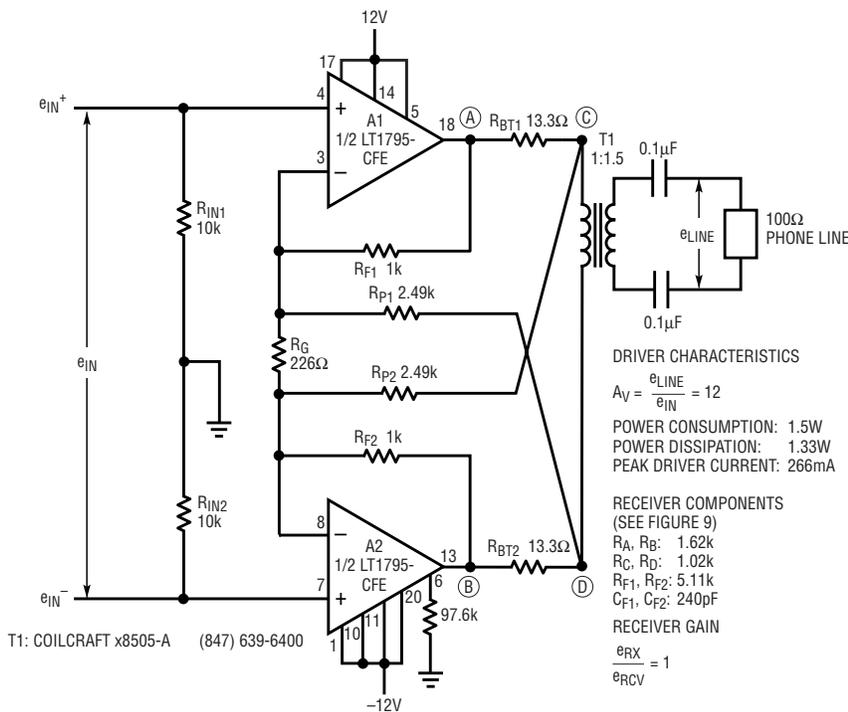
Figure 13. Reduced power dissipation ADSL Full Rate downstream (C) line driver

resistors are connected to ground rather than using a single resistor connected to the other amplifier's inverting input. Capacitors C1 and C2 are included to prevent applying gain to the DC offset voltages of the amplifiers. The different values of feedback capacitors for the receiver amplifier account for the frequency spectrum of the downstream information from the CO modem in either the Full Rate (1104kHz) or G.Lite (552kHz) implementation.

ADSL G.Lite Downstream (CO) Line Driver

This moderate power (16.4dBm) driver requires less than 1W and is shown in Figure 11. This design is biased from ±12V supplies and uses a transformer with a turns ratio of only 1:1.2. Although the peak current is only 140mA, the LT1886 cannot be used due to its limited operating supply voltage of 13.2V total. Instead the LT1795CFE, which is in a very small TSSOP power package, is used. This small package is ideal for central office, multiple DSL port designs for compacting a high number of drivers on a single PC card.

ADSL Full Rate Downstream (CO) Line Driver

Figure 12 is the highest powered DSL line driver application, used in central office applications to obtain up to 8Mbps data rates throughout the Internet. This design uses standard back termination and can be powered from ±12V supplies by using a 2:1 turns ratio transformer. This results in a fairly high, 355mA peak output current demand from the amplifiers. The LT1795, with a 500mA output current rating, once again is capable of the task.

Reduced Power Dissipation ADSL Full Rate Downstream (CO) Line Driver

To address the power consumption and dissipation issues for Full Rate ADSL drivers, a slightly modified topology can be used, as shown in Figure 13. Recognizing that one-half of the power provided by the amplifiers is lost in the transformer back-termination resistors, an obvious approach to reduce power is to simply reduce the value of these resistors. Doing so, however, modifies the output impedance of the modem as seen from the phone line and also

reduces the amount of received signal developed across these sensing resistors. Although it is powered by ±12V supplies, the circuit of Figure 13 achieves 300mW of power savings. The driver current is substantially reduced by using a transformer turns ratio of only 1.5:1. Normally, this would require a higher supply voltage of ±14V and R_{BT} resistors of 22.2Ω. However, although the R_{BT} resistors are reduced to 13.3Ω, the circuit still maintain the proper line-impedance termination of 100Ω and operates from ±12V supplies. It is not suitable for every application, however, because it still reduces the amount of received signal. It is most applicable for systems that use a sensitive receiver AFE that can still detect the reduced received signal.

The approach is termed active termination. A small amount of positive feedback in each amplifier is obtained from the opposite amplifier output. This feedback makes the effective output impedance seen looking into the circuit at nodes C and D the proper value even though the R_{BT} resistor has been reduced by 40% from what is should be. The design equations for this topology are as follows.

Instead of using the standard value of R_{BT} resistance, it can be reduced to any value desired, with attendant received-signal loss. A factor called K can be used to define the new R_{BT} resistance:

$$R_{BT} = \frac{K \cdot Z_{LINE}}{2 \cdot n^2} \qquad (16)$$

With standard termination and a 1:1.5 turns ratio transformer, the value of R_{BT} should be 22.2Ω. In the design of Figure 13, this resistor is reduced by 40% to 13.3Ω, therefore the factor K = 0.6.

The normal forward path circuit gain from the noninverting input of each amplifier to the output nodes A and B is a term called G where G = 1+ R_F/R_G.

The gain of the positive feedback signal path for each side (from node D to A and from node C to B, is called P where P = R_F/R_P.

<div align="center">**Table 3. Driver and receiver amplifier characteristics**</div>

Line Drivers						
Part	**LT1795**	**LT1207**	**LT1886**	**LT1497**	**LT1206**	**LT1210**
Single/Dual	Dual	Dual	Dual	Dual	Single	Single
Output Current	500mA	250mA	200mA	125mA	250mA	1.1A
Supply Voltage	10V to 30V	10V to 30V	5V to 13V	5V to 30V	10V to 30V	10V to 30V
Gain Bandwidth Product	50MHz	60MHz	75MHz	50MHz	60MHz	35MHz
Slew Rate	900V/μs	900V/μs	200V/μs	900V/μs	900V/μs	900V/μs
I_Q/Amplifier	1mA to 30mA	1mA to 30mA	7mA	10mA	1mA to 30mA	1mA to 50mA
V_{SAT}^+	1.2V	1.2V	0.75V	1.2V	1.2V	1.2V
V_{SAT}^-	1.2V	1.2V	0.9V	1.15V	1.2V	1.25V
R_{SAT}^+	1.2Ω	3.2Ω	3.1Ω	14Ω	3.2Ω	0.9Ω
R_{SAT}^-	2Ω	5.3Ω	2.3Ω	10Ω	5.3Ω	1.7Ω
Dual-Amplifier Receivers						
Part	**LT1355**	**LT1358**	**LT1361**	**LT1364**	**LT1813**	**LT1253**
Supply Voltage	5V to 30V	5V to 30V	5V to 30V	5V to 30V	5V to 12V	10V to 24V
Gain Bandwidth	12MHz	25MHz	50MHz	70MHz	100MHz	90MHz
Slew Rate	400V/μs	600V/μs	800V/μs	1000V/μs	750V/μs	250V/μs
Noise Voltage	10nV/√Hz	8nV/√Hz	9nV/√Hz	9nV/√Hz	8nV/√Hz	3nV/√Hz
I_Q/Amplifier	1.25mA	2.5mA	5mA	7.5mA	3mA	6mA

Using these abbreviations:
For proper impedance matching: P = 1 – K.

To obtain a desired voltage gain from the AFE output to the line, A_V, the term G is set to:

$$G = \frac{A_V \bullet e_{PRI}}{e_{LINE}} \bullet (1 + K - P) - P \qquad (17)$$

where e_{PRI} and e_{LINE} are the voltages at the transformer primary and on the line, determined by taking into account the turns ratio and transformer insertion loss.

The use of a high performance amplifier such as the LT1795 does not result in any degradation of distortion performance when modifying the closed-loop gain by positive feedback. Significant power savings can be obtained but the design may not be suitable for all applications as previously mentioned.

Conclusion

Following the design procedures described in this article should make the design and implementation easy and accurate. At the very least, it will ensure that power and heat issues receive proper consideration.

Linear Technology offers a variety of high speed, low distortion power amplifiers and low noise dual amplifiers that can be used to implement the driver/receiver functions of the DSL modem (see Table 3). ⌐⌐

Measure Resistances Easily, without Reference Resistor or Current Source

by Glen Brisebois

Measuring the resistance of a device, for example a thermistor, usually requires biasing it with a precision current source or combining it with several other precision resistors in a bridge. The circuit of Figure 1 shows how to use the new LT1168 instrumentation amplifier to achieve a precision resistance-to-voltage conversion as simply as possible. Normally, the resistor across pins 1 and 8 is the gain-set resistor and the voltage across pins 3 and 2 is the variable to be measured. In this case,

however, the 1.25V reference establishes a fixed input voltage so that the variable to be measured is now the resistance. The equation for V_{OUT} vs R_T is $V_{OUT} = 1.25V \cdot 49.4k\Omega / R_T$. Given the limitation on output swing (with the supply voltages shown), the smallest measurable resistance is about 4.5k. The highest resolvable resistance is limited to about 200M by the 300μV output offset voltage of the LT1168. The 0.05% accuracy of the LT1634 is not an issue here, because it is subtracted at the Ref pin of the

LT1168 and only contributes to gain error. Figure 2 shows output voltage vs temperature for 10k and 100k (at 25°C) thermistors from two manufacturers. Thermistors are difficult to linearize, so although the output is still not linear with temperature, it can, at least, be read directly by an ADC and compared against a lookup table. The circuit has good noise immunity but does not tolerate capacitance at pin 1 or 8 and so is not ideal for resistive devices placed remotely from the LT1168. ![LT]
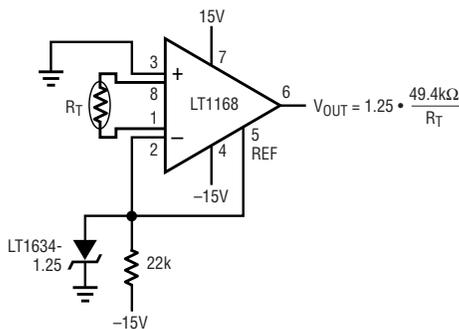
Figure 1. Simple resistance-to-voltage converter
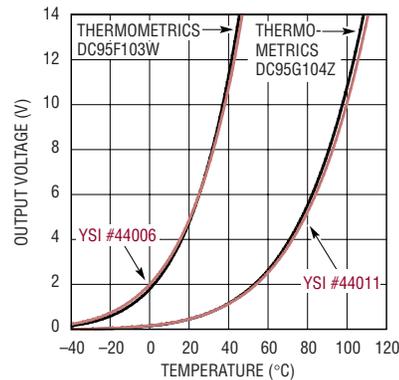
Figure 2. Output voltage vs temperature for thermistors from two manufacturers. Curves are approximations to aid design— contact manufacturers for exact lookup tables: YSI (800) 765-4974; Thermometrics (732) 287-2870.

New Device Cameos

LTC1726: A Micropower, Precision Triple Supply Monitor Adds Adjustable Reset and Watchdog Timer Functions

In multiple-processor systems, such as network servers and routers, 5V, 3.3V and 2.5V supplies are very common and are typically designed to ±5% tolerances. The LTC1726 solves the system-level problem of providing early warning of supply voltage failure to system control logic. Also, it incorporates additional features so that system designers can implement a variable reset time-out and/or variable watchdog time-out. In the LTC1726, both the reset and the watchdog time-out periods are fully adjustable using external capacitors.

In the systems mentioned above, PC board area is at a premium. To address this system constraint, the LTC1726 is available in either SO-8 or MSOP-8 packaging. For monitoring three supplies, two resistors and two capacitors are the only external components required by the LTC1726; Like the LTC1727 and the LTC1728 (see "New Device Cameos" in *Linear Technology* IX:2, June 1999), the LTC1726 is available in two versions: the LTC1726-5 is designed to monitor 5V, 3.3V and one user-defined supply voltage. The LTC1726-2.5 is designed to monitor 3.3V, 2.5V and one user-defined supply voltage. The adjustable supply voltage monitor is a high impedance input with a 1V threshold that allows the system designer to program the monitored voltage using two external resistors. Both versions operate at a supply current of 16µA and offer tight ±1.5% threshold accuracy over temperature and glitch immunity that ensures reliable reset operation without false triggering.

The LTC1726 is powered from either of the two preset supply voltage monitor inputs, allowing the reset output to be active low, independent of supply voltage sequencing. In addition, the reset output is guaranteed to be active low for supply voltages down to 1V.

LTC1751-5 Regulated Charge Pump Delivers 5V at 100mA without Inductors

Charge pump–based power supplies offer the advantages of low solution cost, simplicity and small size. Until now, however, their output current capability has been very limited. While retaining the best features of its predecessors, the LTC1751-5 delivers 100mA (500mW) to the load from an MS8 package while stepping up 3V to a regulated 5V. Additionally, it provides shutdown capability, a power-good feature and programmable soft-start timing. The LTC1751-5 also has built-in thermal shutdown circuitry that allows it to survive a continuous short circuit to ground at its output.

The quiescent supply current of the LTC1751-5 is only 20µA. This low supply current ensures very low power consumption in light load applications, resulting in extended battery life. Furthermore, because it uses Burst Mode operation, its efficiency with a 3V input is 82.4%, which is very close to the theoretical maximum charge pump efficiency of 83.3%. In shutdown the supply current is less than 1µA.

The PGOOD pin can be used to alert a microcontroller when the output voltage of the LTC1751-5 has reached its final value. This is useful, for example, if the LTC1751-5 is providing power to a peripheral device that will communicate with the microcontroller. Furthermore, in the event of an undervoltage fault at the V_{OUT} pin, the PGOOD pin reports the fault. Once the fault is removed, PGOOD returns to the "all-clear" state.

An optional soft-start circuit allows the LTC1751-5's output voltage to be increased as slowly as necessary. A slow rise time on V_{OUT} will prevent unnecessary start-up and loading problems by limiting the current into the output capacitor. A small external capacitor on the SS pin programs the rise time to an appropriate rate. If start-up current isn't an issue, the SS capacitor can be omitted.

With no inductors and only three to four small capacitors, the LTC1751-5 regulated charge pump delivers significant power and functionality from a very small footprint.

LT1962 300mA Low Noise, Micropower Low Dropout Regulator Saves Current in Battery-Powered Applications and Operates with Small Ceramic Capacitors

The LT1962 is a low noise, low dropout linear regulator that is rated for 300mA of output current at a dropout voltage of 300mV and comes in an 8-lead MSOP package. The regulator is designed for use in battery-powered systems with 30µA quiescent current and less than 0.1µA supply current in shutdown. The LT1962 can operate with as little as 3.3µF of output capacitance. Any capacitor, including small ceramic capacitors, can be used on the output without the need for additional series resistance, as is commonly required with other regulators. Quiescent current is well controlled; it does not rise in dropout, as is the case with many competing devices.

The LT1962 features low noise operation. With the addition of an external 0.01µF bypass capacitor, output voltage noise over the 10Hz-to-100kHz bandwidth is reduced to $20\mu V_{RMS}$. This is the lowest output voltage noise of any linear regulator currently available. The LT1962 is capable of operating over a wide 1.8V to 20V supply range. Internal protection circuitry includes reverse-battery protection, current limiting, thermal limiting and reverse-current protection.

The LT1962 is available in fixed output voltages of 2.5V, 3V, 3.3V and 5V, or as an adjustable device with an output voltage range of 1.22V to 20V. The LT1962 is packaged in the space-saving 8-lead MSOP package with a

fused leadframe for improved thermal resistance.

LT1963 1.5A Low Noise, Low Dropout Regulator Provides Fast Transient Response

The LT1963 is a low noise, low dropout linear regulator rated for 1.5A of output current at a dropout voltage of 350mV. The regulator is designed for use in applications where fast transient response is necessary, such as powering ASICs or FPGAs. The LT1963 can operate with as little as 10µF of output capacitance. Small ceramic capacitors can be used without the need for additional series resistance, as is commonly required with other regulators. The 1mA quiescent current drops to less than 1µA in shutdown. Quiescent current is well controlled; it does not rise in dropout.

The LT1963 features low noise operation. Output voltage noise over the 10Hz-to-100kHz bandwidth is under 40µV$_{RMS}$. The LT1963 is also capable of operating over a wide 1.9V to 20V supply range. Internal protection circuitry includes reverse-battery protection, current limiting, thermal limiting and reverse-current protection.

The LT1963 is available in fixed output voltages of 1.8V, 2.5V and 3.3V or as an adjustable device with an output voltage range of 1.21V to 20V. The LT1963 is available in an 8-lead SO package, with full features and a fused leadframe for lower thermal resistance; it is also available in a 3-lead SOT-223 without shutdown and remote sensing, for a small size/ low thermal resistance combination. Surface mount 5-lead DD and through hole 5-lead TO-220 packages are available for applications requiring higher power dissipation.

LTC1706-82 Programs Power for Next Generation Pentium Processors Down to 1.1V with ±0.25% Accuracy

The LTC1706-82 is a 5-bit desktop VID voltage programmer that programs the output of a whole family of LTC controller-based DC/DC converters to supply a precise input supply voltage to the next generation of Pentium® microprocessors. The Pentium processor's supply voltage requirements change with the various clock speed options. To meet this need, the LTC1706-82 uses its five programmable VID inputs to program a ±0.25% accurate output voltage from 1.10V to 1.85V in 25mV steps. This is fully compliant with the Intel Pentium Processor VID Specification (VRM 9.0).

The LTC1706-82 comes in the small 10-lead MSOP package. It consumes practically zero current (only device leakage) when all five inputs are high; each grounded VID input adds only 68µA of input current in a 3.3V system. For extremely high current applications (up to 200A), such as high-end servers and workstations, just one LTC1706-82 can program up to six LTC1629 PolyPhase, high efficiency, step-down DC/DC controllers to complete an extremely compact, powerful, programmable power supply that uses only surface mount components.

In addition to the LTC1629, the LTC1706-82 also works equally well with the LTC1735, LTC1702, LTC1628 and other LTC DC/DC converters with onboard 0.8V references.

LTC1779 Step-Down DC/DC Converter Delivers 250mA from Tiny 6-Lead SOT-23

The LTC1779 is a constant frequency, current mode, step-down DC/DC converter capable of 250mA output current operation without an external power switch or sense resistor. Its constant 550kHz operating frequency allows the use of a small external inductor. This feature, coupled with the part's tiny SOT-23 package, results in a very small footprint solution.

The LTC1779 operates over a wide V$_{IN}$ range of 2.5V to 9.8V and is capable of efficiencies up to 90% while maintaining excellent AC and DC load and line regulation. The device, which boasts ±2.5% output voltage accuracy, consumes only 130µA of quiescent current in normal operation and a mere 8µA in shutdown. Under light load conditions, the device optimizes efficiency using Burst Mode operation. To maximize the life of the battery source, the internal power switch is turned on continuously in dropout (100% duty cycle). ![LT]

DESIGN TOOLS

Technical Books

1990 Linear Databook, Vol I —This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

1992 Linear Databook, Vol II — This 1248 page supplement to the 1990 Linear Databook is a collection of all products introduced in 1991 and 1992. The catalog contains full data sheets for over 140 devices. The 1992 Linear Databook, Vol II is a companion to the 1990 Linear Databook, which should not be discarded. $10.00

1994 Linear Databook, Vol III —This 1826 page supplement to the 1990 and 1992 Linear Databooks is a collection of all products introduced since 1992. A total of 152 product data sheets are included with updated selection guides. The 1994 Linear Databook Vol III is a companion to the 1990 and 1992 Linear Databooks, which should not be discarded. $10.00

1995 Linear Databook, Vol IV —This 1152 page supplement to the 1990, 1992 and 1994 Linear Databooks is a collection of all products introduced since 1994. A total of 80 product data sheets are included with updated selection guides. The 1995 Linear Databook Vol IV is a companion to the 1990, 1992 and 1994 Linear Databooks, which should not be discarded. $10.00

1996 Linear Databook, Vol V —This 1152 page supplement to the 1990, 1992, 1994 and 1995 Linear Databooks is a collection of all products introduced since 1995. A total of 65 product data sheets are included with updated selection guides. The 1996 Linear Databook Vol V is a companion to the 1990, 1992, 1994 and 1995 Linear Databooks, which should not be discarded. $10.00

1997 Linear Databook, Vol VI —This 1360 page supplement to the 1990, 1992, 1994, 1995 and 1996 Linear Databooks is a collection of all products introduced since 1996. A total of 79 product data sheets are included with updated selection guides. The 1997 Linear Databook Vol VI is a companion to the 1990, 1992, 1994, 1995 and 1996 Linear Databooks, which should not be discarded. $10.00

1999 Linear Data Book, Vol VII — This 1968 page supplement to the 1990, 1992, 1994, 1995, 1996 and 1997 Linear Databooks is a collection of all product data sheets introduced since 1997. A total of 120 product data sheets are included, with updated selection guides. The 1999 Linear Databook is a companion to the previous Linear Databooks, which should not be discarded. $10.00

1990 Linear Applications Handbook, Volume I — 928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels. $20.00

1993 Linear Applications Handbook, Volume II — Continues the stream of "real world" linear circuitry initiated by the 1990 Handbook. Similar in scope to the 1990 edition, the new book covers Application Notes 40 through 54 and Design Notes 33 through 69. References

and articles from non-LTC publications that we have found useful are also included. $20.00

1997 Linear Applications Handbook, Volume III — This 976 page handbook maintains the practical outlook and tutorial nature of previous efforts, while broadening topic selection. This new book includes Application Notes 55 through 69 and Design Notes 70 through 144. Subjects include switching regulators, measurement and control circuits, filters, video designs, interface, data converters, power products, battery chargers and CCFL inverters. An extensive subject index references circuits in LTC data sheets, design notes, application notes and *Linear Technology* magazines. $20.00

1998 Data Converter Handbook — This impressive 1360 page handbook includes all of the data sheets, application notes and design notes for Linear Technology's family of high performance data converter products. Products include A/D converters (ADCs), D/A converters (DACs) and multiplexers—including the fastest monolithic 16-bit ADC, the 3Msps, 12-bit ADC with the best dynamic performance and the first dual 12-bit DAC in an SO-8 package. Also included are selection guides for references, op amps and filters and a glossary of data converter terms. $10.00

Interface Product Handbook — This 424 page handbook features LTC's complete line of line driver and receiver products for RS232, RS485, RS423, RS422, V.35 and AppleTalk® applications. Linear's particular expertise in this area involves low power consumption, high numbers of drivers and receivers in one package, mixed RS232 and RS485 devices, 10kV ESD protection of RS232 devices and surface mount packages.

Available at no charge

Power Management Solutions Brochure — This 96 page collection of circuits contains real-life solutions for common power supply design problems. There are over 70 circuits, including descriptions, graphs and performance specifications. Topics covered include battery chargers, desktop PC power supplies, notebook PC power supplies, portable electronics power supplies, distributed power supplies, telecommunications and isolated power supplies, off-line power supplies and power management circuits. Selection guides are provided for each section and a variety of helpful design tools are also listed for quick reference.

Available at no charge.

Data Conversion Solutions Brochure — This 64 page collection of data conversion circuits, products and selection guides serves as excellent reference for the data acquisition system designer. Over 60 products are showcased, solving problems in low power, small size and high performance data conversion applications—with performance graphs and specifications. Topics covered include ADCs, DACs, voltage references and analog multiplexers. A complete glossary defines data conversion specifications; a list of selected application and design notes is also included.

Available at no charge

Telecommunications Solutions Brochure —This 76 page collection of application circuits and selection guides covers a wide variety of products targeted for telecommunications. Circuits solve real life problems for central office switching, cellular phones, high speed modems, base station, plus special sections covering –48V and Hot Swap™ applications. Many applications

highlight new products such as Hot Swap controllers, power products, high speed amplifiers, A/D converters, interface transceivers and filters. Includes a telecommunications glossary, serial interface standards, protocol information and a complete list of key application notes and design notes. Available at no charge.

Applications on Disk

FilterCAD™ 2.0 CD-ROM — This CD is a powerful filter design tool that supports all of Linear Technology's high performance switched capacitor filters. Included is FilterView™, a document navigator that allows you to quickly find Linear Technology monolithic filter data sheets, the FilterCAD manual, application notes, design notes and *Linear Technology* magazine articles. It *does not* have to be installed to run FilterCAD. It is not necessary to use FilterView to view the documents, as they are standard .PDF files, readable with any version of Adobe Acrobat™. FilterCAD runs on Windows® 3.1 or Windows 95. FilterView requires Windows 95. The FilterCAD program itself is also available on the web and will be included on the new LinearView™ CD. Available at no charge.

Noise Disk — This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp. Available at no charge

SPICE Macromodel Disk — This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models and a demonstration copy of PSPICE™ by MicroSim. Available at no charge

SwitcherCAD™ — The SwitcherCAD program is a powerful PC software tool that aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. 144 page manual included. $20.00

SwitcherCAD supports the following parts: LT1070 series: LT1070, LT1071, LT1072, LT1074 and LT1076. LT1082. LT1170 series: LT1170, LT1171, LT1172 and LT1176. It also supports: LT1268, LT1269 and LT1507. LT1270 series: LT1270 and LT1271. LT1371 series: LT1371, LT1372, LT1373, LT1375, LT1376 and LT1377.

Micropower SwitcherCAD™ — The MicropowerSCAD program is a powerful tool for designing DC/DC converters based on Linear Technology's micropower switching regulator ICs. Given basic design parameters, MicropowerSCAD selects a circuit topology and offers you a selection of appropriate Linear Technology switching regulator ICs. MicropowerSCAD also performs circuit simulations to select the other components which surround the DC/DC converter. In the case of a battery supply, MicropowerSCAD can perform a battery life simulation. 44 page manual included. $20.00

MicropowerSCAD supports the following LTC micropower DC/DC converters: LT1073, LT1107, LT1108, LT1109, LT1109A, LT1110, LT1111, LT1173, LTC1174, LT1300, LT1301 and LT1303.

CD-ROM Catalog

LinearView — LinearView™ CD-ROM version 4.0 is Linear Technology's latest interactive CD-ROM. It allows you to instantly access thousands of pages of product and applications information, covering Linear Technology's complete line of high performance analog products, with easy-to-use search tools.

The LinearView CD-ROM includes the complete product specifications from Linear Technology's Databook library (Volumes I–VII) and the complete Applications Handbook collection (Volumes I–III). Our extensive collection of Design Notes and the complete collection of *Linear Technology* magazine are also included.

A powerful search engine built into the LinearView CD-ROM enables you to select parts by various criteria, such as device parameters, keywords or part numbers. All product categories are represented: data conversion, references, amplifiers, power products, filters and interface circuits. Up-to-date versions of Linear Technology's

software design tools, SwitcherCAD, Micropower SwitcherCAD, FilterCAD, Noise Disk and Spice Macromodel library, are also included. Everything you need to know about Linear Technology's products and applications is readily accessible via LinearView. LinearView runs under Windows 95 or later.

Available at no charge.

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