LINEAR TECHNOLOGY

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3MHz Synchronous Boost Regulators Save Critical Board Space in Portable Applications

by Mark Jordan

Introduction

The proliferation of portable devices with ever increasing functionality has imposed a higher demand on power conversion circuitry, with a continued emphasis on maximizing battery life while reducing board real estate. Linear Technology's new LTC3401 and LTC3402 synchronous boost converters operate at high frequency, facilitating the use of a small low cost inductor and tiny ceramic capacitors. Both the LTC3401 and LTC3402 come in a thermally enhanced MSOP-10 package, with the lead frame of the IC connected to ground (pin 5).

With the converter housed in a small MSOP-10 package, the area of a complete 300mW converter is less than $0.08in^2$, with a low 1.2mm profile. For a 2W converter, the board area is less than $0.18in^2$. Efficiencies of up to 97% are achieved through internal features such as lossless current sensing, low gate charge, low $R_{DS(ON)}$ synchronous power switches and fast switching transitions to minimize power loss. An external Schottky diode is not required, but may be used to maximize efficiency.

The LTC3401 is optimized for applications requiring less than 1 amp of input current, whereas the LTC3402 is optimized for applications requiring up to 2 amps of input current. The operating frequency is programmable from 100kHz to 3MHz, which allows these products to fit nicely in various applications where size and efficiency considerations can be traded off. The ICs start up with an input voltage below 1V and, once started, operate with an input below 0.5V. Proper operation below 0.5V protects against worst-case voltage droops in the battery during high current load transients. The output voltage is adjustable from 2.6V to 5.5V with a simple resistor voltage divider.

The current mode control architecture, along with OPTI-LOOP™ compensation and adaptive slope compensation, allows the transient response to be optimized over a wide range of loads, input voltages, and output capacitors. At light loads, the user can choose to enter high efficiency Burst Mode™ operation. The IC consumes only 38µA of quiescent current in this mode. The part can also be commanded to shut down, drawing less than 1µA of quiescent current.

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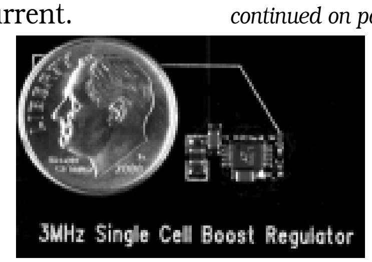


Figure 1. LTC3401, 3MHz single cell to 3V evaluation circuit

Issue Highlights

Our cover article in this issue introduces the new LTC3401 and LTC3402 synchronous boost converters. These devices operate at high frequency, allowing the use of a small low cost inductor and ceramic capacitors. Because they are housed in the small MSOP-10 package, the area of a complete 300mW converter is less than 0.08in^2, with a low 1.2mm profile. Efficiencies of up to 97% are achieved.

Several other new power products are featured in this issue. The LTC1922 is a full featured controller for the phase-shifted full-bridge converter. It combines programmable fixed frequency, current mode control with novel circuitry for zero voltage switching over all operating conditions, optimizing efficiency. Built-in current-doubler synchronous rectification control increases efficiency and reduces output voltage ripple.

The LTC1731/LTC1732 are constant-current/constant-voltage linear charge controllers for single-cell Li-Ion batteries. Output voltage accuracy is 1% (max) over the –40°C to 85°C range, preventing overcharging. The small size of the devices, along with the small number of external parts required, makes them ideal for use in portable and handheld products.

In a related story, we preview SwitcherCAD III, LTC's new switching regulator SPICE tool. Its schematic capture format allows quick iterations and analysis of a design. Part libraries feature comprehensive models of LTC's switching regulators. A steady-state, start-up or load-transient analysis can be completed in minutes. For users unfamiliar with either SPICE tools or switcher design, demonstration circuits are included.

This issue also debuts a variety of new amplifiers. The new LT1797 op amp offers 10MHz gain bandwidth and rail-to-rail inputs and outputs in a tiny SOT-23 package. The usual bandwidth vs supply current tradeoff has been optimized by designing on a 6GHz f_T process and running the transistors at reduced quiescent currents. The result is a fast, tiny, rail-to-rail device that brings to the table all the beauty that is the operational amplifier, while consuming minimal board space and power.

Operating from supplies as low as 2.5V, the 325MHz LT1806 and the 180MHz LT1809 rail-to-rail amplifiers provide the distortion and noise performance required by low voltage signal conditioning and data acquisition systems. Rail-to-rail inputs and outputs allow the entire supply range to be used and their high output current capability is ideal for cable-driver applications. The LT1806 is optimized for noise and DC performance whereas the LT1809 is optimized for slew rate and distortion. Both parts are fully specified for 3V, 5V and ±5V operation.

The LTC2050, LTC2051 and LTC2052 are the smallest zero-drift op amps currently available. They occupy minimal board space while providing the lowest input offset and offset drift. In addition, they operate over a wide supply range, from 2.7V to ±5V. They have rail-to-rail outputs that can drive loads as small as 1k to either supply rail, plus an input range from the negative supply to typically less than 1V from the positive supply.

Our Design Information section presents a new family of differential-input ΔΣ ADCs compatible with the LTC2400. The LTC2410 features 0.1ppm offset error, 2ppm INL, 0.16ppm RMS noise and a common mode reference/input range of GND to V_{CC}; the LTC2411 is packaged in a tiny 10-pin MSOP package with differential input and differential reference; the LTC2413 offers simultaneous 50Hz and 60Hz rejection and is pin compatible with the LTC2410.

Also in the Design Information section is the LTC1661, a dual, serially addressable 10-bit, rail-to-rail voltage output DAC with Sleep mode. Its small size and low power consumption make it most appropriate for use in products with stringent space and/or power constraints.

LTC in the News…

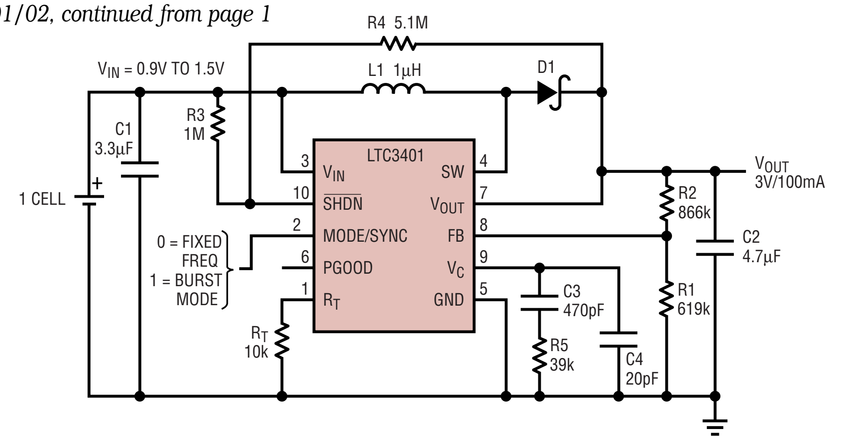
On October 17, Linear Technology Corporation announced its financial results for the first quarter of fiscal year 2001. Robert H. Swanson, Chairman & CEO, stated, "Business continues strong for us in all of our major markets. We increased sales 10% and profits 15% sequentially over the previous quarter, which is particularly strong performance for a summer quarter. We achieved a record level of return on sales of 44%. These continue to be great times for a high performance analog company. Opportunities in Internet infrastructure, wireless communication and mobile computing fuel our growth in communications, computers and industrial applications. We currently see this strength continuing and estimate that we will grow sales and profits sequentially in the 8% to 10% range for the December quarter."

The Company reported sales of $232,141,000 and net income of $102,178,000 for the first quarter. Net sales were up 57% over the same quarter last year. Diluted earnings per share were $0.31, an increase of 75% over the first quarter last year.

In a recent article in *Electronic Buyers' News*, John Day attributes the booming demand for mixed-signal devices to better design techniques and process technologies helping the industry advance toward the "system-on-a-chip." LTC's Todd Nelson offers this perspective. "Our multiprotocol transceivers have gone from three chips to two and our current chips are smaller than the old ones. The 2-chip approach gives customers flexibility in selecting the content of the second chip. Each chip has 28 pins, for a total of 56. A single-chip solution would require 80 pins and customers would have to pay for features they don't need. Customers want lower solution costs and they want to make the best use of board space."

Our Design Ideas section features three power supply circuits and an "infinite" sample-and-hold design. We conclude with a quintet of New Device Cameos.

LTC3401/02, continued from page 1



D1: CENTRAL SEMICONDUCTOR CMDSH-3 (631) 435-1110
L1: TAIYO YUDEN LB2016 (408) 573-4150
C1: TAIYO YUDEN JMK212BJ33MG
C2: TAIYO YUDEN JMK212BJ47MG

Figure 2. 1.2mm high, ultracompact single cell to 3V converter

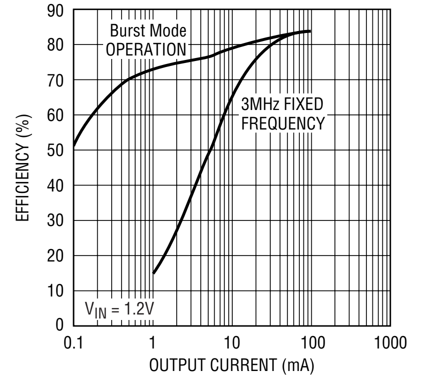


Figure 3. Efficiency of the circuit in Figure 2

1V to 3V, 300mW Converter in less than 0.08 in²

In applications where the physical size is the most critical design factor, the high switching frequency of the LTC3401 allows the use of small ceramic capacitors and a tiny chip inductor, as shown in the evaluation circuit photo in Figure 1. The circuit schematic is shown in Figure 2. This compact, 1.2mm high converter switches at a fixed frequency of 3MHz and can step up a single-cell alkaline battery to 3V with an output load up to 100mA. The efficiency peaks at 83% at 100mA output current, as shown in Figure 3, with the efficiency loss being primarily due to the series resistance of the chip inductor and the ICs switching losses. Using an inductor with lower series resistance, reducing the operating frequency and increasing the size of the filter capacitor result in efficiencies over 90% for this application, although the improved efficiency comes at the expense of added board area.

The Burst Mode efficiency of the converter of Figure 2 is 70% at 500µA load, making it ideal for applications such as pagers, which power down for extended periods of time.

The switching waveform of the SW pin at 3MHz is shown in Figure 4. The fast rise and fall times of less than 5ns along with short break-before-make times between the synchronous switches of 20ns contribute to the high efficiency of the converter.

High Efficiency 1.6W, 2 Cell to 3.3V Converter

Many 2-cell applications require higher output power, but efficiency considerations are as important as board area. The circuit of Figure 5 operates at 1MHz and uses a 0.16in diameter Sumida power inductor along with all ceramic capacitors. The efficiency is 95% at 300mW output power, as shown in Figure 6. Removing the Schottky diode will reduce board area by approximately 5%, but at the cost of 4% less efficiency.

The LTC3402 for Higher Power Applications

The LTC3402 is ideal for applications requiring higher power, such as a 4W Li-Ion to 5V converter shown in Figure 7. To minimize conduction losses at these higher currents, it is imperative to choose low ESR power components. Inductor saturation at high current is also a factor in the selection process. The efficiency of the circuit in Figure 7, with the Li-Ion battery at the nominal 3.6V, peaks at 94%, as shown in Figure 8.

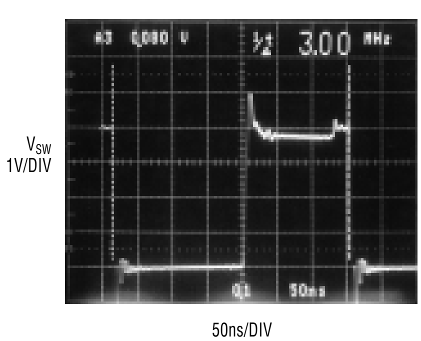
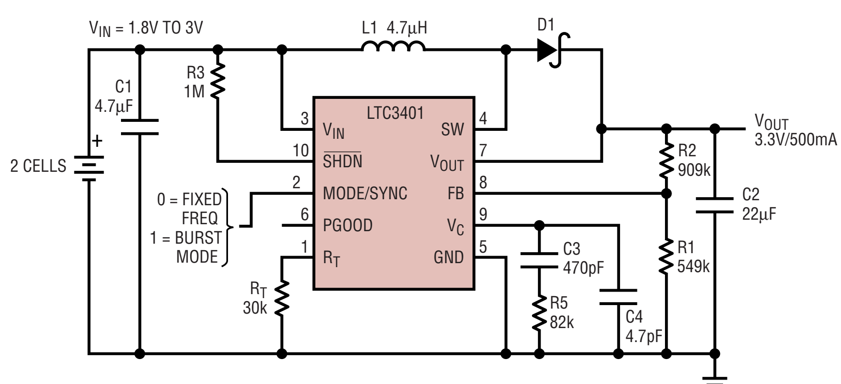


Figure 4. 3MHz switching waveform on the SW pin



L1: SUMIDA CD43-4R7M (847) 956-0667
C1: TAIYO YUDEN JMK212BJ475MG (408) 573-4150
C2: TAIYO YUDEN JMK325BJ226MM
D1: ON SEMICONDUCTOR MBRM120T3 (602) 244-6600

Figure 5. All-ceramic-capacitor 2-cell converter delivers 3.3V at 500mA

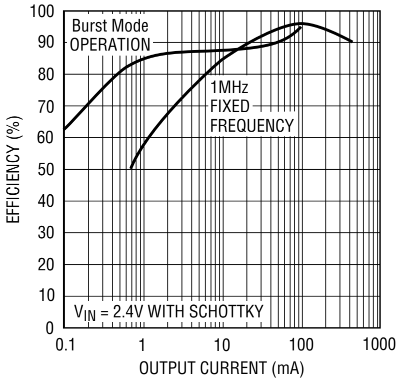
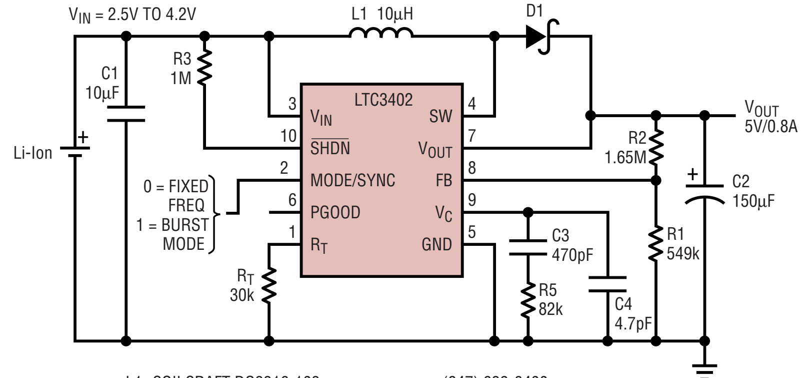


Figure 6. Efficiency of the circuit in Figure 5



L1: COILCRAFT DO3316-103 (847) 639-6400
C1: TAIYO YUDEN JMK212BJ106MM (408) 573-4150
C2: AVX TPSD157M63R (207) 282-5111
D1: ON SEMICONDUCTOR MBR0520L (602) 244-6600

Figure 7. Single Li-Ion cell to 5V application at 800mA

High Efficiency Li-Ion CCFL Backlight Application

Small portable applications with a CCFL backlight, such as a PDA, require a highly efficient backlight converter solution to maximize operating time before recharging. A high efficiency Li-Ion CCFL supply is shown in Figure 9. The LTC3401 provides the tail current to the self-oscillating resonant Royer circuit, which generates the high voltage sinusoidal wave to the lamp. The lamp dimming is provided by means of a control voltage, but alternate dimming techniques can be used.

Flexible Boost Converters

Today's portable electronics environment requires power conversion that is adaptable to varying conditions. The LTC3401 and LTC3402 allow the user to modify output voltage, operating frequency, Burst Mode operation and loop compensation with simple modifications to external components.

The IC remains in fixed frequency mode until the user allows the IC to enter Burst Mode operation. When the MODE/SYNC pin is driven high, full-time power saving Burst Mode operation is enabled. In Burst Mode operation, the converter delivers energy to the output until the regulation voltage is reached. At that point the IC ceases to switch and goes to "sleep" until the output voltage has drooped to typically 1% of the regulated value. The IC then wakes up and delivers energy again and the cycle repeats itself. The efficiency at light loads is improved in Burst Mode operation due to the dramatic reduction in switching and quiescent current losses.

The MODE/SYNC pin serves an additional function of oscillator synchronization. The internal oscillator can be synchronized to an external clock at a higher frequency than the free-running frequency, with

continued on page 8

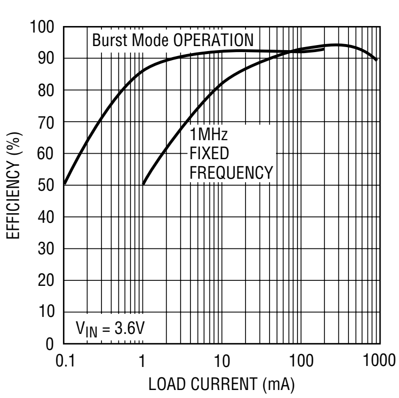
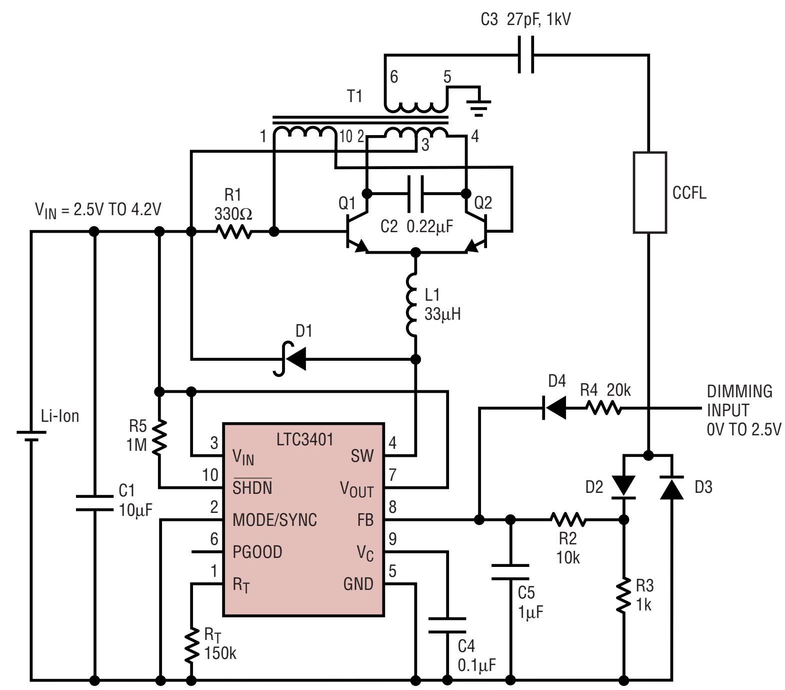


Figure 8. Efficiency of the circuit in Figure 7



T1: SUMIDA C1Q122 (847) 956-0667
L1: SUMIDA CD-54-330MC
Q1, Q2: ZETEX FMMT-617 (631) 543-7100
C1: TAIYO YUDEN JMK212BJ106MM (408) 573-4150
C2: PANASONIC ECH-U (201) 348-7522
D1: ZETEX ZHCS-1000
D2–D4: 1N4148

Figure 9. High efficiency, compact CCFL supply with remote dimming

SOT-23 10MHz Rail-to-Rail Op Amp Saves Board Space and Power

by Glen Brisebois

Introduction

The new LT1797 op amp offers 10MHz gain bandwidth and rail-to-rail inputs and outputs in a tiny SOT-23 package. The usual bandwidth vs supply current trade-off has been optimized by designing on a 6GHz f_T process and running the transistors at reduced quiescent currents. The result is a fast, tiny, rail-to-rail device that brings to the table all the beauty that is the operational amplifier, while consuming minimal board space and power. The LT1797 is available in both I grade and C grade.

When comparing the LT1797 to competing products, don't stop at input offset voltage and input offset current. Be sure to look at open-loop gain, PSRR, CMRR, AC distortion, noise power, supply voltage range and output voltage swing. Table 1 shows some of the LT1797's specifications at a glance.

Table 1. LT1797 specifications

Symbol	Parameter	Typical	Worst Case Over Temperature*
V_{OS}	Input Offset Voltage	1mV	2.5mV (I grade: 3mV)
I_{OS}	Input Offset Current	10nA	25nA
GBW	Gain Bandwidth Product	10MHz	5MHz (I grade: 4.5MHz)
A_{OL}	Open-Loop Gain	1000V/mV	150V/mV
PSRR	Power Supply Rejection Ratio	90dB	80dB
CMRR	Common Mode Rejection Ratio	96dB	88dB
THD	Total Harmonic Distortion, f = 1kHz, A_V = 1	0.001%	——
V_S	Supply Voltage Range	2.5V to 12.6V	2.7V to 12V
I_S	Supply Current, V_S = 3V	1.1mA	2.0mA
P_N	Noise Power, f = 10kHz ($e_N \bullet i_N$)	4.6×10^{-21}W/Hz	——
V_{OH}	Output Voltage Swing High, V_S = 3V, I_{OUT} = 5mA	2.8V	2.7V
V_{OL}	Output Voltage Swing Low, V_S = 3V, I_{SINK} = 5mA	80mV	100mV

*C grade: 0°C to 70°C; I grade: –45°C to 85°C

Applications

Fast Settling, Compact, –48V Current Sense

Figure 1 shows a compact, fast-settling current sense circuit designed for –48V supplies. Fast settling is required in applications that involve circuit-breaking or power rerouting. The circuit operates as follows. Current flowing through the sense resistor creates a voltage across it of $V = I_{SENSE} \times R_{SENSE}$. The LT1797's output rises until an equal voltage appears across R3, with the current flowing from Q1's emitter (= $I_{SENSE} \times R_{SENSE}/R3$). Q1's emitter current comes from its collector and appears as an easily measured voltage across R2. R2 is connected to a 3V supply, so the output voltage equation becomes $V_{OUT} = 3V - I_{SENSE} \times R_{SENSE} \times R2/R3$. With the values shown, the output response is –100mV per amp. R1 is a 5% resistor that reduces Q1's power dissipation at higher currents. The LT1797, the Zener diode and the transistor are both SOT-23 packages. Q1 was chosen for its high breakdown voltage and high β at low currents. Settling time of better than 2µs to 1% was measured on a 1V output step. Total error is shared approximately equally between the 1% resistors, the transistor β and the LT1797 input offset voltage.

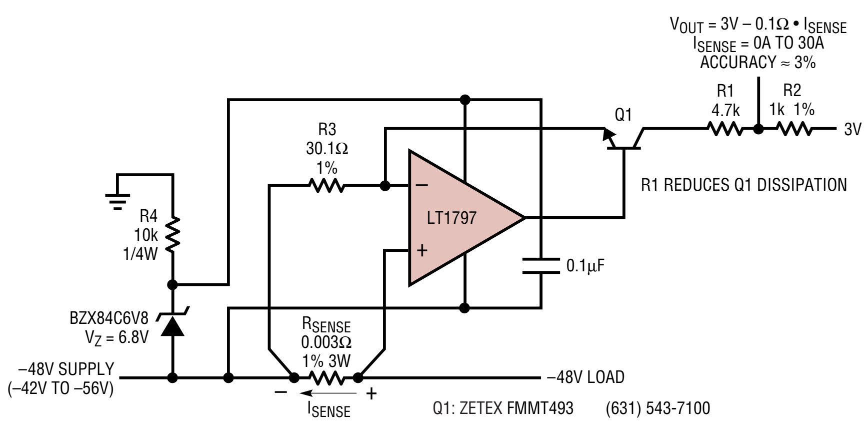
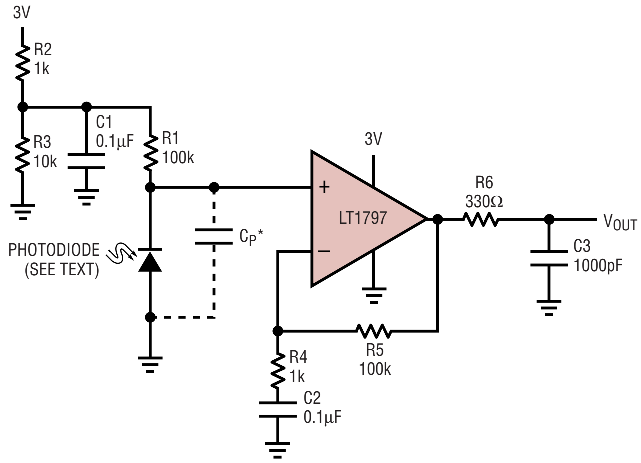


Figure 1. Fast, compact –48V current sense



*C_P = SUM OF PHOTODIODE CAPACITANCE, PARASITIC LAYOUT CAPACITANCE AND LT1797 INPUT CAPACITANCE

Figure 2. Simple, high gain 65kHz photodiode amplifier

Long-Range Photodiode Receiver

Much has been written about photodiode amplifiers, but relatively little has been published showing real circuits with achieved results. The circuit of Figure 2 is a simple photodiode amplifier that was optimized for range (or, if you prefer, sensitivity) with about 65kHz of bandwidth[1]. The keys to achieving range are high gain and low noise. The lowest noise I/V converter is a resistor, so the simplest thing to do is to place a resistor in series with the photodiode (R1 of Figure 2). The problem is that putting a resistor in series with the photodiode reduces the bandwidth, but is infinite bandwidth needed? Maximizing this series resistance improves the inherent signal to noise ratio because the signal is proportional to R1, whereas the resistor noise is proportional to $\sqrt{R1}$. R1 was chosen at 100kΩ to support 100kHz of bandwidth with 16pF[2] of combined photodiode and parasitic capacitance ($f_{-3dB} = 1/2\pi RC_P$). This achieves 100kΩ of transimpedance gain before even getting to the amplifier (pretty good!). R2, R3 and C1 bias the photodiode near the upper rail, reducing its capacitance while decoupling it from power supply noise and keeping the AC operation well ground referenced. Biasing the LT1797 near its upper rail also has the effect of favoring its NPN input stage, which improves the data sheet's $0.23\text{pA}/\sqrt{\text{Hz}}$ current noise specification by a factor of about $\sqrt{3}$. With a large input resistance of 100kΩ, the current noise of the LT1797 would otherwise begin to dominate the circuit's noise performance. (It will be shown later that amplifier noise is not the limiting factor in many applications, anyway.)

R4, R5 and C2 place the LT1797 in an AC gain of 101. This high gain is not a problem for the LT1797 because of its high open-loop gain, and simply has the effect of reducing the bandwidth to 100kHz. R4 and C2 roll off the gain below 1.6kHz. This cancels the effect of 1/f noise and prevents amplification of the total DC offset, which by this point is several millivolts due to the 50nA bias current and the 100kΩ source impedance. R6 and C3 set a reliable upper limit on noise bandwidth at 500kHz, with minimal effect on signal bandwidth. When all is said and done, this single stage gives a total transimpedance gain of 10MΩ, down 3dB at 65kHz.[3]

The total output noise was measured with the circuit battery-powered in a sealed cookie tin with the low capacitance SFH213 photodiode installed. Using a Hewlett Packard 3403C true RMS meter, the output noise was 1.84mV_{RMS}. This result is in approximate agreement with the calculated RMS sum of the total noise sources: voltage noise, current noise $\times R_S$, and R_S Johnson noise.

$$V_{NOISE\_RMS} = \text{gain} \times \text{skirt\_factor} \times \sqrt{BW} \times \sqrt{e_n^2 + (i_n \times R_S)^2 + 1.7e\text{-}20 \times R_S},$$

where gain = 101, skirt factor = 1.3 and BW = 80kHz[4], $e_n = 20\text{nV}/\sqrt{\text{Hz}}$, $i_n = 0.14\text{pA}/\sqrt{\text{Hz}}$, and R_S = 101kΩ.

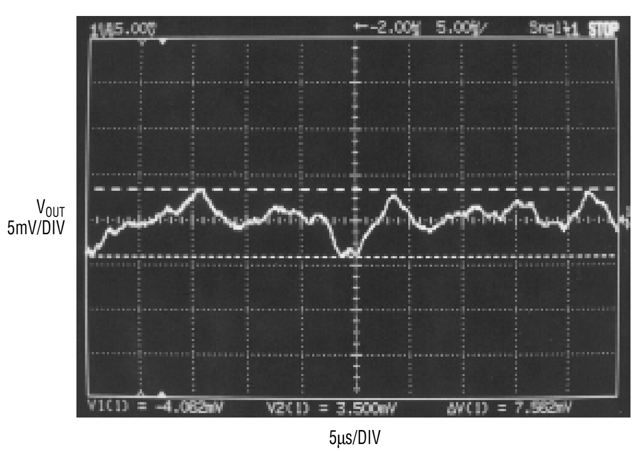


Figure 3. Total amplifier output noise is $7.6\text{mV}_{P\text{-}P}$. The upper limit on measurement bandwidth is dictated by op amp gain bandwidth and R6 × C3. Lower limit is 20kHz, set by the 50µs time window.

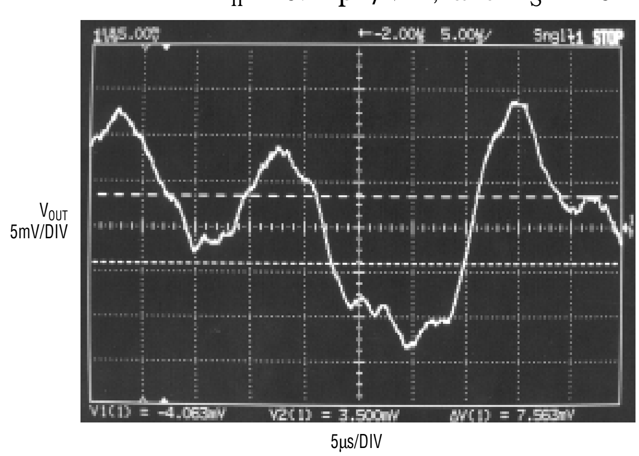


Figure 4. The same circuit exposed indirectly to fluorescent light. Cursors show amplifier noise measurement for comparison. The photodiode used is the least susceptible to this problem.

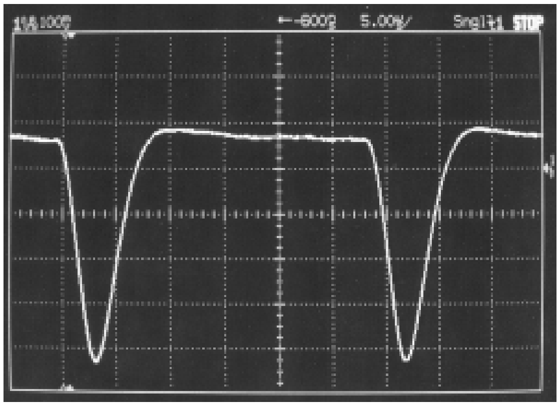


Figure 5. Reception at 16 feet using the SFH213FA. The transmitter is an HSDL-4220 IR LED pulsed with 330mA for 3.5µs.

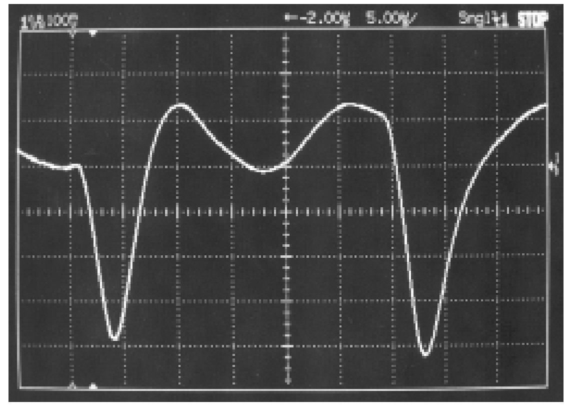


Figure 6. The same conditions as Figure 5, but without an IR filter. The photodiode is an SFH213.

This comes out to $1.8mV_{RMS}$, very close to the $1.84mV_{RMS}$ measured. Figure 3 shows the peak-to-peak output noise at $7.6mV_{P-P}$[5], about four times the RMS value. This output voltage noise represents a total input-referred current noise, and hence resolution, of $0.76nA_{P-P}$. Note that the method of calculating and/or measuring total output noise and then converting to an equivalent input current noise is more realistic than approaches that place undue initial emphasis on low amplifier input current noise. Placing undue emphasis on amplifier input current noise leads one to believe that JFET input amplifiers are the only option.

Although it is possible, and maybe even easy, to improve upon the noise figures achieved, in many through-air transmission applications it would be pointless. This is illustrated in Figure 4, where the circuit has been exposed to light (with the least susceptible photodiode, an SFH213FA). The disgusting results are due to the fluorescent lights in the laboratory; their interference swamps any concerns about amplifier input noise. The problem appears to be a combination of two effects; visible light getting past the imperfect "black plastic" IR filter and the presence of actual IR or near-IR emissions from the lamps. Some lamps are worse than others, with efficient "warmer" lamps being the big culprits. Know your environment.

Overall results with three different photodiodes are shown in Figures 5 through 7. The transmitter is an Agilent HSDL-4220 IR LED placed sixteen feet away, with a drive current of 330mA for 3.5µs using a 10% duty cycle. Figures 5 and 6 show the LT1797 receiver circuit output with the fast, narrow-angle Siemens/Infineon SFH213FA and SFH213 PIN photodiodes. The only difference between these devices is that the FA version has a black plastic filter that eliminates much of the visible fluorescent interference (the 50kHz ripple apparent in Figure 6), while only slightly attenuating the signal. Figure 7 shows results using a wide angle Vishay/Telefunken BPV22NF PIN photodiode. Signal amplitude is reduced not because the BPV22NF takes less optical gain, as this is compensated by its seven times increase in die area over the high optical gain SFH213 types. The reduction in amplitude is primarily due to the bandwidth reduction caused by the factor of seven increase in capacitance. The presence of the fluorescent interference in the case of the BPV22NF is not due to the lack of a visible light filter: it has one. Rather, it is due to its wide angle of acceptance. So, although the wider angle allows reception over a broader angle of transmitter locations, it also opens up its eyes to a lot more background interference through the (always imperfect) filter. At any rate, in none of the three cases is amplifier noise the dominating limit to achieving range.

The circuit works well even at close range because the LT1797 has good output clipping recovery. However, the amplitude of the photodiode current at close range can be fairly

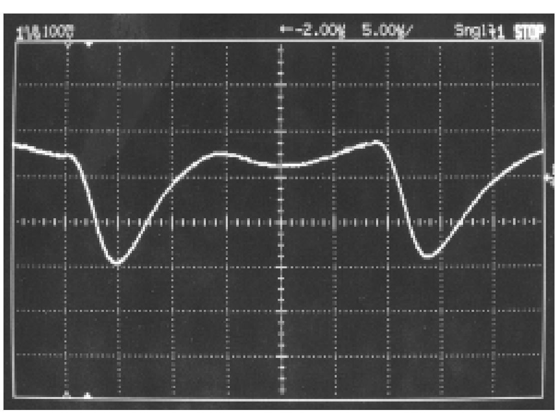


Figure 7. Same conditions as Figures 5 and 6, but using a wider-angle, larger-die device, the BPV22NF. The IR filter attempts to reject some of the fluorescent light; capacitance slows the response.

high, in which case the recovery time will rise and the output pulse width will increase. The higher capacitance BPV22NF shows this effect more than does the SFH213. This circuit is not suited to pulse width modulation schemes unless physical transmitter motion will be below the frequency of interest and the steady-state pulse width is noncritical.

Convert Your Favorite Op Amp to a Rail-to-Rail Output

Many of the world's greatest op amps were not originally intended for operation on reduced supply voltages, the ultralow noise LT1028 being a good example. The LT1797 can help remedy this situation by converting the output stage of one of these amplifiers to a rail-to-rail output stage. Figure 8 shows the method. The LT1028 output drives the noninverting input of the LT1797, which is placed in a gain of three by R1 and R2. The feedback resistors R3 and R4 put the entire loop in a gain of 500, forcing the LT1028 to provide a gain of 167. This combination of the two amplifiers takes advantage of the ultralow noise, precision front end of the LT1028 and the rail-to-rail output of the LT1797. The circuit is stable from a gain-phase point of view without compensation components R5 and C1. However, when the input receives a transient or the output hits a rail, the two op amps begin a usually unrecoverable slew-rate contest. R5 and C1 fix this by slowing down the LT1028.

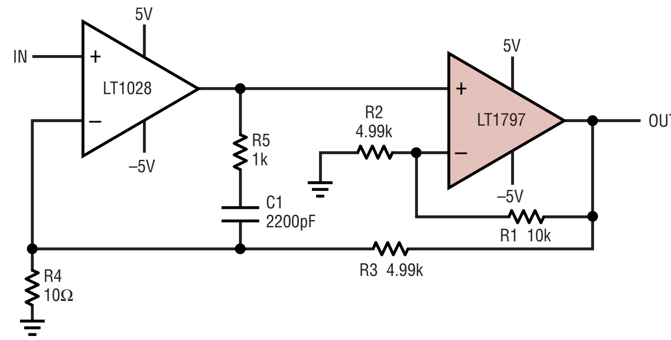


Figure 8. Converting the LT1028 to a ±5V supply with rail-to-rail output; A_V = 500

Conclusion

The LT1797 is a compelling choice where minimal footprint or rail-to-rail 10MHz gain bandwidth are essential. The efficient nature of the LT1797 design also makes it suitable for applications where power is at a premium and wide bandwidth and output drive are also required.

Notes:

[1] To cut to the chase, results will be given with sixteen feet of transmitter-receiver separation.

[2] Some of the photodiodes tested had more capacitance than this, and some had less. Although it is tempting to place a trimpot at R1, the parasitic capacitance of a bulky trimpot would quickly complicate the matter.

[3] Cascading the two 100kHz –3dB bandwidths results in a net bandwidth of 65kHz. However, the –3dB that is due to the photodiode capacitance and R1 will be more or less dependent on the photodiode used, and this will have an effect on the net bandwidth.

[4] The bandwidth is chosen at about 80kHz because the low capacitance photodiode will not reduce the 100kHz bandwidth as much as would the design value of 16pF. For additional complexity, the bandwidth reduction due to input capacitance has effect on current noise and Johnson noise but not voltage noise. Also, the fact that measurements are made over a finite period of time introduces an inherent highpass characteristic. The skirt factor is next to impossible to determine because of the complexity of the various roll-off mechanisms. The value of 1.3 is a compromise.

[5] Taking 100 measurements using a 50µs window, the average peak-to-peak noise was $7.7mV_{P-P}$ with a standard deviation of $1.2mV_{P-P}$. Note that a 50µs window has a highpass effect above about 15kHz.

For more information on parts featured in this issue, see http://www.linear-tech.com/go/ltmag

LTC3401/02, continued from page 4

a pulse width of less than 2µs. The state of the Mode condition remains unchanged because of internal filtering. For applications requiring a flag to indicate the condition of the output voltage, the PGOOD pin provides an open drain output, which pulls low when the output voltage is more than 9% below the regulation voltage.

Conclusion

With Linear Technology's family of high performance synchronous boost converters, the designer of handheld electronics can easily extend operation time while saving critical board real estate. The high frequency operation of the LTC3401 and LTC3402 allows the use of all ceramic capacitors and a small inductor. The low voltage start-up makes these products ideal for single-cell alkaline portable applications, and the ability to program the operating frequency, output voltage, loop compensation and Burst Mode operation allows the designer to make the necessary decisions to optimize the power conversion for the given portable application. Low R_{ON} (0.16Ω NMOS, 0.18Ω PMOS) synchronous switches optimize efficiencies for all applications. All of this functionality is packed into a small MSOP-10 package.

Low Distortion Rail-to-Rail Amplifiers Drive ADCs and Cables

by William Jett, Danh Tran and Glen Brisebois

Introduction

Operating from supplies as low as 2.5V, the 325MHz LT1806 and the 180MHz LT1809 rail-to-rail amplifiers provide the distortion and noise performance required by low voltage signal conditioning and data acquisition systems. Rail-to-rail inputs and outputs allow the entire supply range to be used, and the high output current capability, 60mA typical on a 3V supply, is ideal for cable-driver applications. The LT1806 is optimized for noise and DC performance, featuring a low voltage noise of $3.5nV/\sqrt{Hz}$ and a maximum offset voltage of 550µV. The LT1809 is optimized for slew rate and distortion, featuring a slew rate of 350V/µs and low harmonic distortion –90dBc at f_C = 5MHz (V_S = 5V, V_O = $2V_{P-P}$). Both parts are fully specified for 3V, 5V and ±5V operation and are available in 8-lead SO and 6-lead SOT-23 packages. A shutdown function is included that disables the amplifier and reduces the supply current to less than 1mA.

Performance

Table 1 summarizes the performance of the LT1806 and LT1809. Note that input offset voltage is specified at both the positive and negative supply rails, in contrast to most competitive parts, which are only specified at mid-supply.

Table 1. LT1806/LT1809 key performance specifications

Parameter		LT1806	LT1809
Gain-Bandwidth Product		325MHz	180MHz
Slew Rate		140V/µs	350V/µs
Input Voltage Noise		$3.5nV/\sqrt{Hz}$	$16nV/\sqrt{Hz}$
Harmonic Distortion, R_L = 1k f_C = 5MHz, V_S = 5V, A_V = 1, V_O = $2V_{P-P}$		–80dBc	–90dBc
Settling Time 0.01% V_{STEP} = 2V, V_S = 5V, A_V = 1		60ns	40ns
Operating Supply Range		2.5V to 12V	2.5V to 12V
Output Swing High	I_L = 5mA I_L = 25mA	V_S – 0.18V Max V_S – 0.7V Max	V_S – 0.16V Max V_S – 0.5V Max
Output Swing Low	I_L = 5mA I_L = 25mA	0.13V Max 0.4V Max	0.08V Max 0.3V Max
Short Circuit Current, V_S = 3V		±30mA Min	±40mA Min
Input Offset Voltage V_{CM} = V^+, V^-		0.55mV Max	2.5mV Max
Input Bias Current		13µA Max	28µA Max
CMRR V_S = 5V, V_{CM} = V^+ to V^-		80dB Min	69dB Min
PSRR V_S = 2.5V to 10V, V_{CM} = 0V		91dB Min	73dB Min
Supply Current, V_S = 5V		13mA Max	17mA Max
Supply Current, V_S = 5V Shutdown		0.9mA Max	0.8mA Max

The distortion vs frequency for the two parts is shown in Figures 1–4. The harmonic distortion was measured with two loads: 100Ω, which is representative of a cable-driving application, and 1kΩ, which is typical of signal-conditioning applications. Both devices are quite good but the LT1809 provides the ultimate in distortion performance.

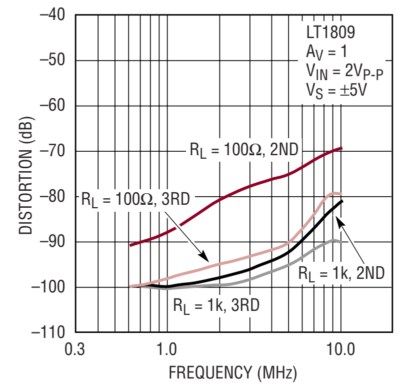


Figure 1. LT1809 distortion vs frequency

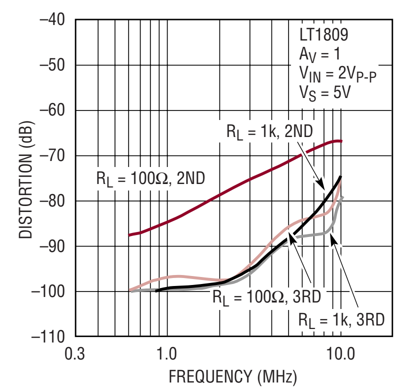


Figure 2. LT1809 distortion vs frequency

Single 3V Supply, 4MHz, 4th Order Butterworth Filter

A low distortion, low voltage filter, suitable for antialiasing applications, is shown in Figure 5. The filter is a cascade of two inverting 2nd order sections, with values selected to give a Butterworth response. In this configuration, signal swing on the inputs of the op amps is small, resulting in

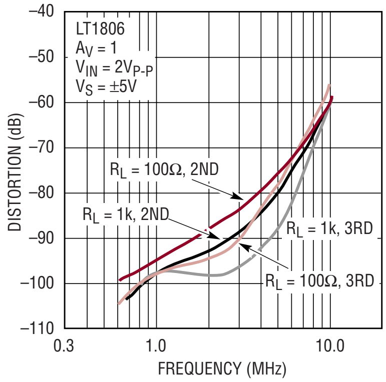


Figure 3. LT1806 distortion vs frequency

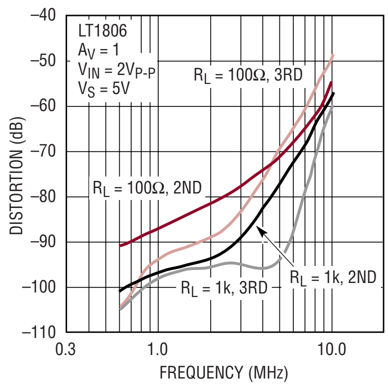


Figure 4. LT1806 distortion vs frequency

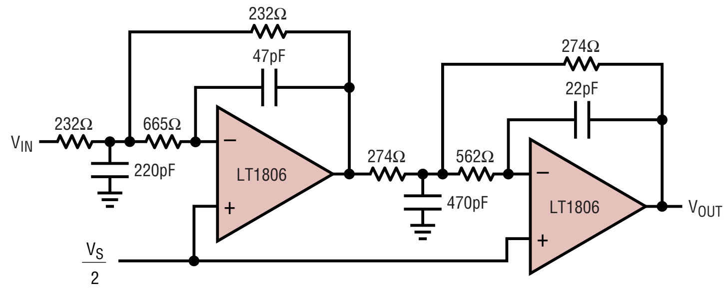


Figure 5. Single 3V supply, 4MHz, 4th order Butterworth filter

good distortion performance. Distortion was measured at –83dBc at 1MHz, V_O = 2.25V_{P-P}. The overall filter response (Figure 6) shows a stopband that has greater than 95dB rejection of frequencies up to 100MHz. Such stopband depth would be difficult to achieve with a dual op amp because of crosstalk and layout issues.

Single 5V Supply Video-Cable Driver

The high output current capability of the LT1809 can be put to use in video-cable-driver applications. Figure 7 shows an AC-coupled video driver using a single 5V supply. The input signal is level shifted to half supply by coupling capacitor C1 and resistor divider R1/R2. An AC gain of two in the amplifier, set by resistors R3 and R4 and capacitor C2, compensates for the loss due to the output termination resistors R5 and R_{LOAD}, resulting in an overall gain of one. Figure 8 shows the frequency response of the driver. The –3dB bandwidth is about 95MHz and peaking is less than 1dB.

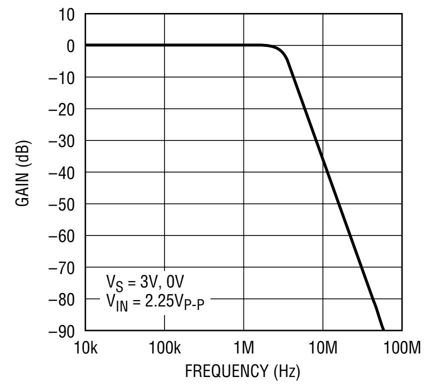


Figure 6. Frequency response of Figure 5's filter

Buffering Data Converters

Driving ADCs is a tricky business. Looking at the circuit of Figure 9, you would correctly surmise that the signal flows from left to right. Entering the noninverting input, this signal takes a gain of 2 in the LT1809. It passes through the 6.8MHz lowpass filter formed by R3 and C1 and is applied to the LTC1420 ADC. With the 10Msps, 12-bit LTC1420 set in a gain of 1 and its internal reference set at 2.048V, the full-scale signal is about 1V_{P-P}, input referred. Figure 10, a 4096 point FFT, shows results achieved with a 1.394MHz signal. The spurious free dynamic range is about 90dB, with performance limited by the ADC's nonlinearities rather than by the LT1809. (Typical SFDR for the LTC1420 is 83dB.)

However, there is also a signal, the ADC sampling glitch, that travels from right to left. It is caused by a small flying sample capacitor in the ADC front end, which introduces an AC short circuit at the ADC's input ten million times per second. This signal

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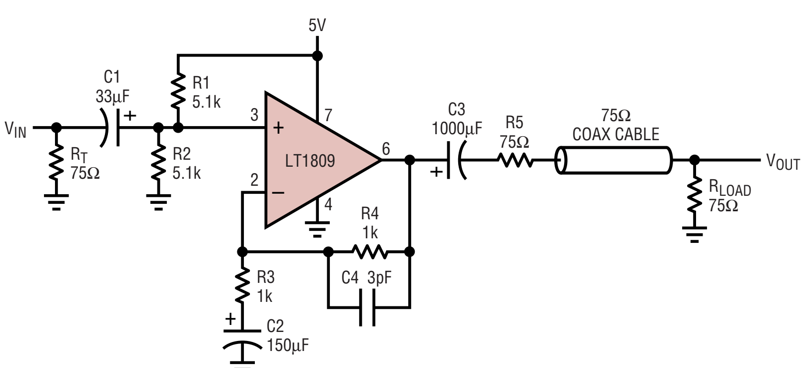


Figure 7. Single-supply video line driver

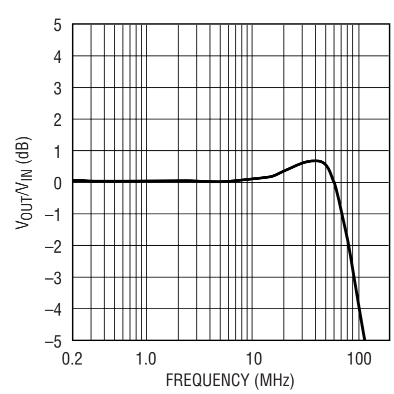


Figure 8. Frequency response of Figure 7's circuit

Phase-Shift Full-Bridge Controller Enables Efficient, Isolated Power Conversion for High Power Applications

by John Bazinet

Introduction

The distributed power supply systems of large data processing and communications equipment use isolated, high power converters to generate intermediate bus distribution voltages and lower voltages for CPU, mass storage and I/O circuitry. Power supply isolation is necessary for regulatory agency requirements, shielding of sensitive circuitry and ground loop elimination. Unfortunately, adding isolation increases complexity and reduces efficiency due to a variety of factors, including magnetic core and copper loss of the power transformer. These problems increase as the power level and input voltage increase. In addition, parasitic leakage inductance can generate high voltage transients across the power MOSFETs reducing efficiency even further and generating undesirable EMI. Any efficiency improvement to these power supplies results in reduced cooling requirements, shrinking volume, weight and cost. Phase-shifted full-bridge power converters have gained attention because of their ability to harness the usually undesirable elements of the power transformer and MOSFETs to significantly reduce switching losses and noise.

The 20-pin G or N packaged LTC1922-1 (Figure 1) is a full featured controller for the phase-shifted

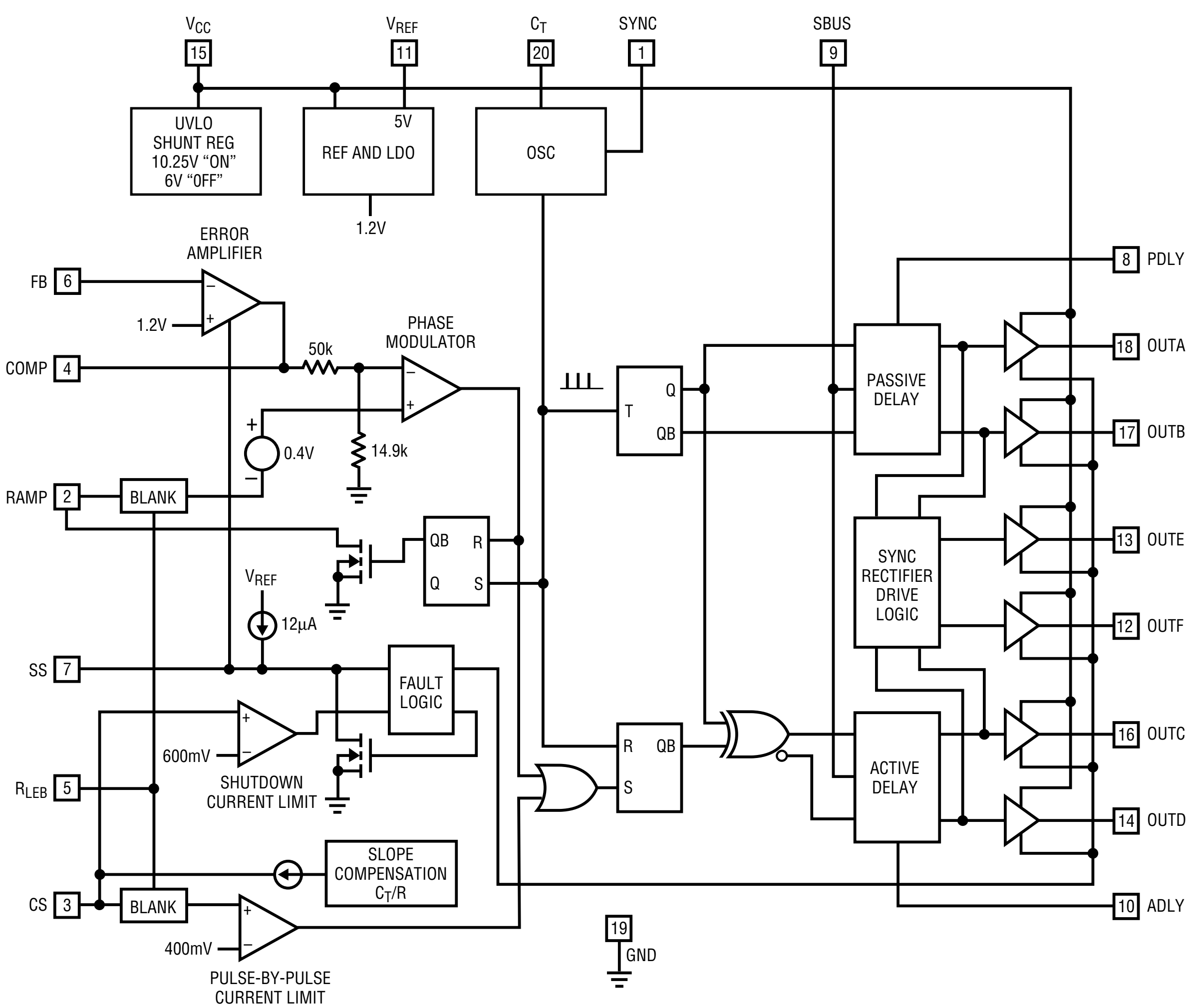


Figure 1. LTC1922 block diagram

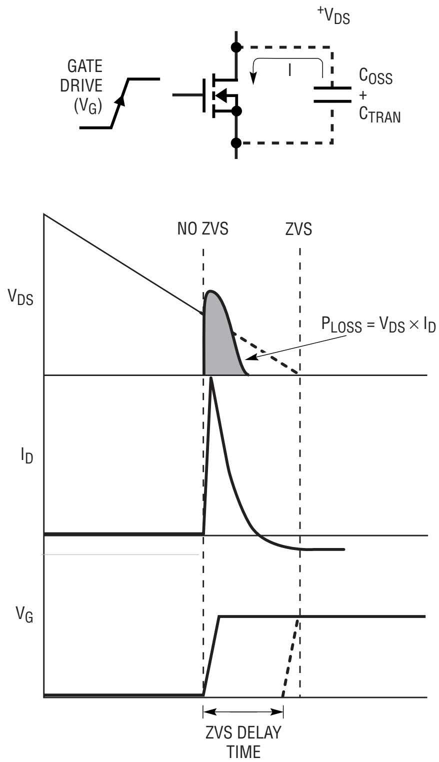


Figure 2. Instantaneous switching loss from capacitive discharge

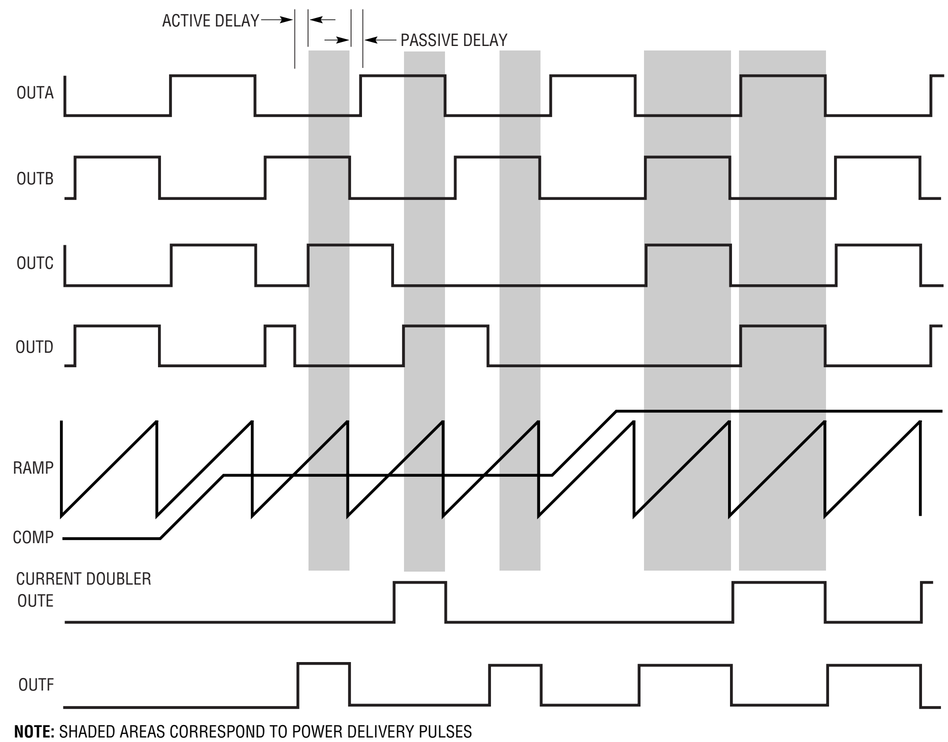


Figure 3. LTC1922 timing diagram

full-bridge converter. Offering a wide range (0%–99.5%) phase modulator, the LTC1922-1 also combines programmable (10kHz to 1MHz) fixed frequency, current mode control with novel circuitry to invoke zero voltage switching (ZVS) over all operating conditions, optimizing efficiency. Built-in current-doubler synchronous rectification control improves efficiency further and reduces output voltage ripple. Low start-up and operating quiescent currents ease the burden on external bias circuitry, while the accurate 5V low dropout regulator provides up to 15mA to power auxiliary circuits. In addition, the LTC1922-1 provides simple programmability for current limit, leading edge blanking, soft-start and short-circuit protection, reducing circuit complexity and design time.

What is a Phase-Shifted Full Bridge?

Rather than hard switching the power MOSFETs like a conventional full bridge or forward converter, the phase-shifted full-bridge converter clamps and recycles the energy stored in the power transformer's leakage inductance to softly turn on each of the four power MOSFETs in the full bridge. ZVS (zero voltage switching) occurs when the external power MOSFETs are turned on and off when their respective drain to source voltages are at or near zero volts, effectively eliminating the instantaneous turn on-power loss of the MOSFETs caused by C_{OSS} (drain-to-source capacitance) and parasitic capacitance discharge (see Figure 2). This improves efficiency, reduces switching related EMI and eliminates the need for primary-side snubbers.

Phase-Shift Control

Referring to Figure 3, alternate diagonal switches in the full bridge (A-D or B-C) conduct simultaneously in order to deliver energy to the load (secondary). Each switch-drive signal has a 50% duty cycle less a small ZVS turn-on delay. Outputs A and B are 180 degrees out of phase and change state every time the oscillator clocks the internal PWM flip flop. Similarly, outputs C and D are 180 degrees out of phase and change state every time RAMP exceeds the PWM control level defined by COMP. As the PWM control level is increased, a corresponding increase of switch conduction overlap (A–D or B–C) or phase shift occurs. The maximum overlap per switch pair is 50%. Since both pairs of switches conduct during a transformer cycle, the maximum attainable duty cycle is 100%. Once a switch turns off, the inherent momentum of the transformer's magnetizing and leakage inductances under phase-shift control help to commutate the respective bridge leg voltages toward a zero voltage condition.

Adaptive DirectSense™ Technology

The LTC1922-1 implements ZVS with closed loop DirectSense technology. Optimal ZVS delay time is a complex nonlinear function of load current, MOSFET C_{OSS}, transformer interwinding capacitance, leakage and magnetizing inductance and output inductance. In addition, each bridge leg exhibits unique behavior necessitating different delays. An optimal delay time prevents hard switching and/or increased body diode conduction, maximizes the duty cycle range and minimizes EMI. Referring to

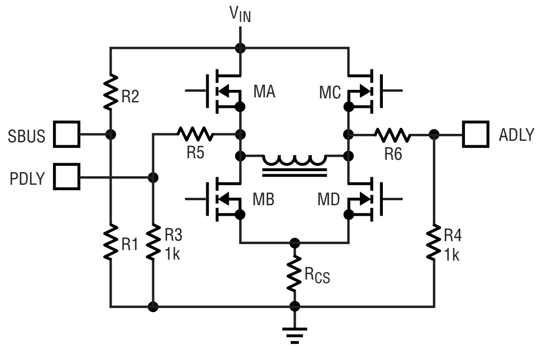


Figure 4. Direct sensing of full bridge

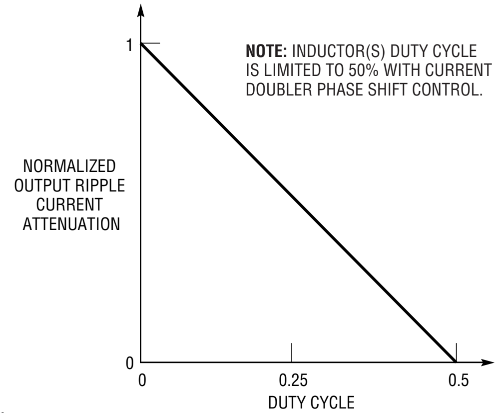


Figure 5. Output inductor ripple vs duty cycle

Figure 4, the LTC1922 senses each leg of the full bridge with a voltage divider on PDLY and ADLY and senses the input supply with a voltage divider on SBUS. Internal high speed latching comparators, state and PWM logic and fail-safe circuits command the respective high-side MOSFETs (MA, MC) to turn on when the rising voltages on PDLY and ADLY cross the threshold level determined by the voltage on SBUS. In addition, every rising edge on ADLY and PDLY initiates an accurate current out of ADLY and PDLY, respectively. This current, along with the external resistor divider, produces a lower threshold level for use when the bridge legs commutate towards ground, providing ZVS to the lower MOSFETs (MB, MD). After the falling edge transition occurs, the current is reset. By sensing the bridge and input supply directly, the LTC1922-1 can intelligently adapt to any change in load current, temperature, component tolerances, driver circuitry delay offset or input voltage. The benefits include simple design, high efficiency, increased duty cycle capability, lower EMI and consistent performance without tweaking.

Synchronous Rectification

Synchronous rectification can provide significant efficiency improvements, especially at lower output voltages and when the synchronous switch timing is optimal. The LTC1922-1 includes the internal timing and logic required to produce drive signals for secondary-side synchronous rectifiers, as shown in Figure 3. These switching intervals have been internally programmed to prevent premature turn on and delayed turn off of the external synchronous rectifiers, maximizing the benefit over silicon or Schottky rectifiers and eliminating external glue logic and discrete timing circuitry.

The synchronous rectifier MOSFETs and transformer secondary power stage are configured as an interleaved current doubler. The current doubler employs two inductors that share the output current equally and, more importantly, are driven 180 degrees out of phase. These properties reduce output capacitor ripple current significantly depending on duty ratio (see Figure 5), reducing voltage ripple and improving output capacitor reliability while producing twice the output current per inductor volume of comparable single inductor power stages.

48V to 3.3V/40A Isolated Converter

The circuit of Figure 6 features the LTC1922-1, regulating 3.3V at up to 40A from an isolated 36V to 72V input voltage. Only surface mount components are used in this design. Peak efficiency is just over 90%, drop-

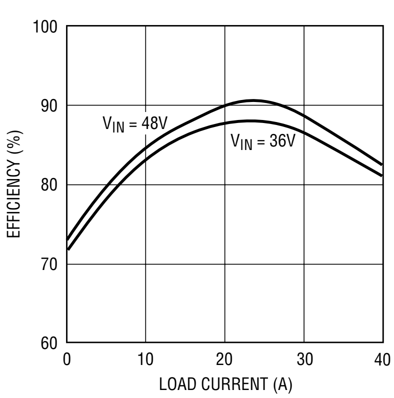


Figure 7. 48V to 3.3V conversion efficiency

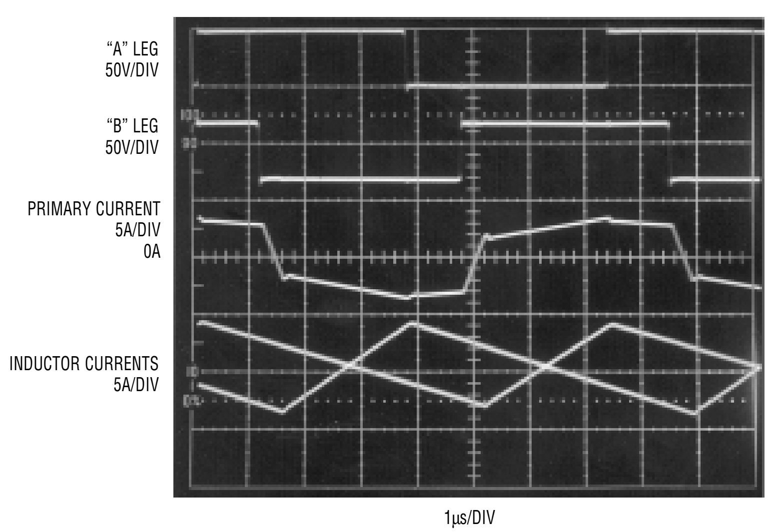


Figure 8. 48V input to 3.3V/20A output waveforms

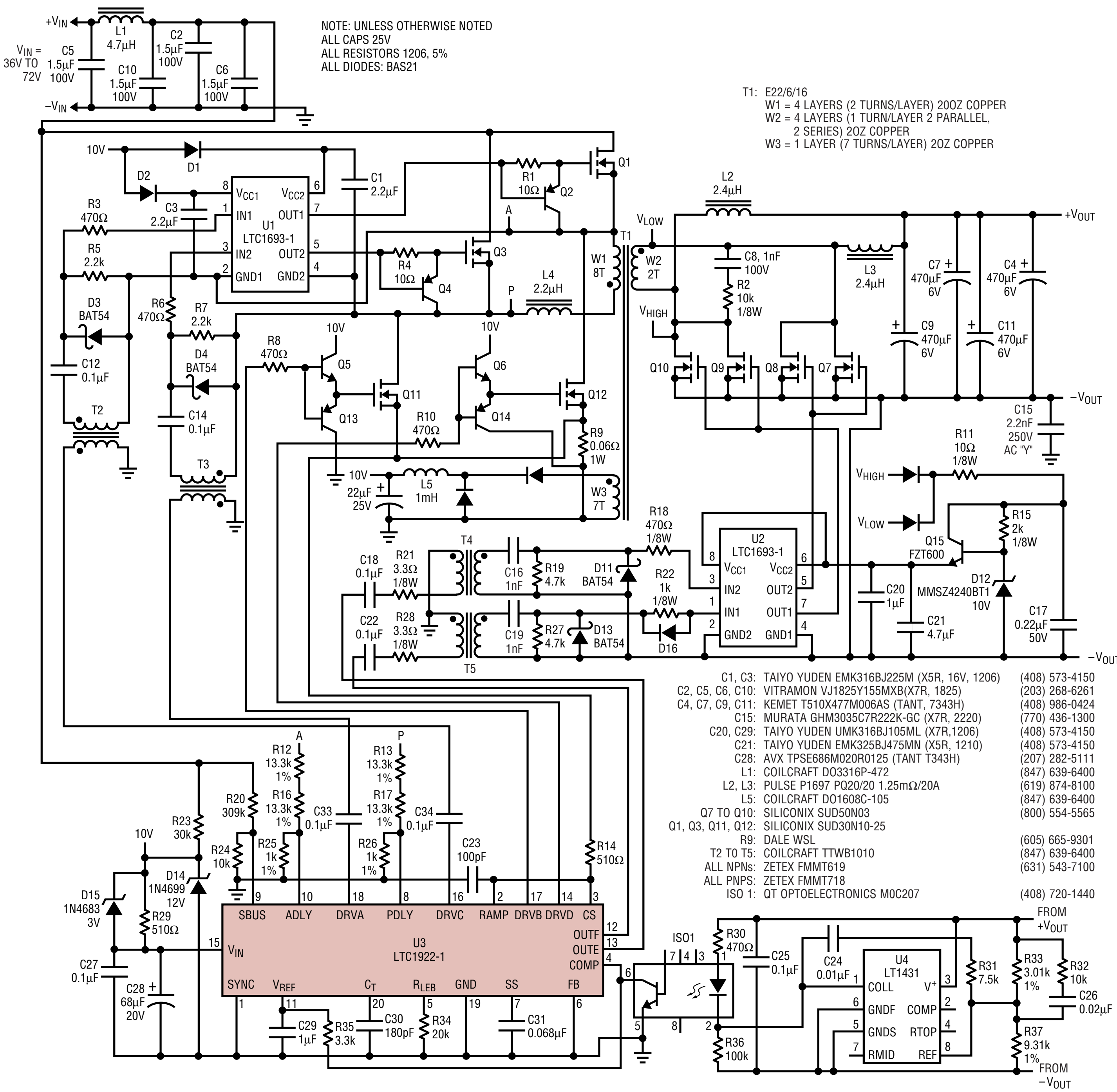


Figure 6. LTC1922 all–surface mount 3.3V/40A converter

ping to 85% at a 40 amp load (Figure 7). The high efficiency eliminates the need for forced air cooling, faceplates or bulky heat sinks. A single LTC1693-1 and tiny signal transformers are used to provide gate drive to the two high-side bridge MOSFETs. A second LTC1693-1 provides the drive to the secondary synchronous rectifiers. The LT1431 and a standard optical coupler provide voltage regulation information across the isolation boundary.

Primary side scope waveforms (Figure 8) exhibit the very clean transitions typical with the phase-shifted full bridge. Since the LTC1922-1 is a current mode controller, it is easily adaptable to standard load-sharing techniques used in redundant power system applications. Additional features of this converter include undervoltage lockout, soft start, leading edge blanking, current limit and short-circuit protection.

Conclusion

The phase-shifted full-bridge converter is an ideal candidate for high power isolated power conversion, as evidenced by its high efficiency and low noise performance. The LTC1922-1 is a next generation control solution for this type of converter offering optimal zero voltage switching and integrated synchronous rectification control among several other features tailored to high power applications.

Zero-Drift Operational Amplifier Family in Small-Footprint Packages Features 3µV Maximum DC Offset and 30nV/°C Maximum Drift

by David Hutchinson

Introduction

The LTC2050, LTC2051 and LTC2052 are single, dual and quad zero-drift operational amplifiers, available in SOT-23, MS8, and GN16 packages, respectively. The smallest zero-drift op amps available, they occupy minimal board space while providing the lowest input offset (3µV max) and offset drift (30nV/°C max) currently available. In addition, they operate over a wide supply range, from 2.7V to ±5V. They have rail-to-rail outputs that can drive loads as small as 1k to either supply rail and they have an input range from the negative supply to typically less than 1V from the positive supply.

Extended Input Common Mode Range with Uncompromising CMRR

At room temperature, and with the input common mode level at mid-supplies, the parts typically have 0.5µV of input-referred offset and are guaranteed to have less than ±3µV. To ensure this DC accuracy over the common mode input range, the LTC2050/LTC2051/LTC2052 have exceptionally high CMRR over a wide range from the negative supply to typically within 0.9V of the positive rail, as shown in Figure 1. For example, as the input is varied over the entire 5V common mode range, the input-referred offset changes typically by less than 0.4µV. Similar levels of PSRR (typically less than 0.1µV of offset per volt of supply change) and the near zero temperature drift ensure that the offset does not exceed 5µV over the entire supply voltage and commercial temperature range.

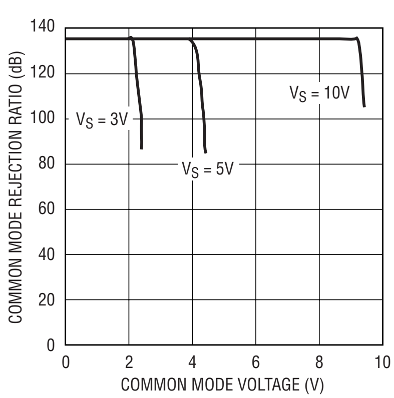


Figure 1. DC CMRR vs input common mode

Rail-to-Rail Output Drive with a 1k Load

The LTC2050/LTC2051/LTC2052 maintain their DC characteristics while driving resistive loads sourcing or sinking currents as high as 5mA. Figure 2 shows the op amps' rail-to-rail swing versus output resistance loading. With a 1k or 5k load, the output typically swings to within 100mV or 30mV, respectively, of the rails.

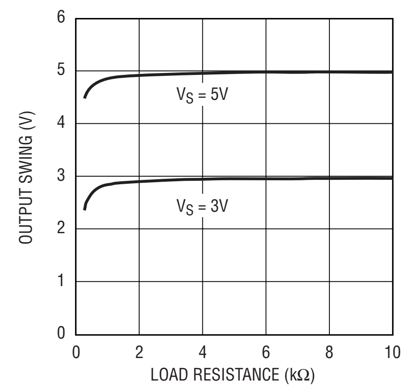


Figure 2. Output voltage swing vs load resistance

Clock Feedthrough and Input Bias Current Virtually Eliminated

The LTC2050 family uses autozeroing circuitry to achieve its zero-drift offset and other DC specifications. The clock used for autozeroing is typically 7.5kHz. There are two types of clock feedthrough in autozeroed op amps like the LTC2050/51/52. The first is caused by the settling of the internal sampling capacitor. The input-referred magnitude of this clock

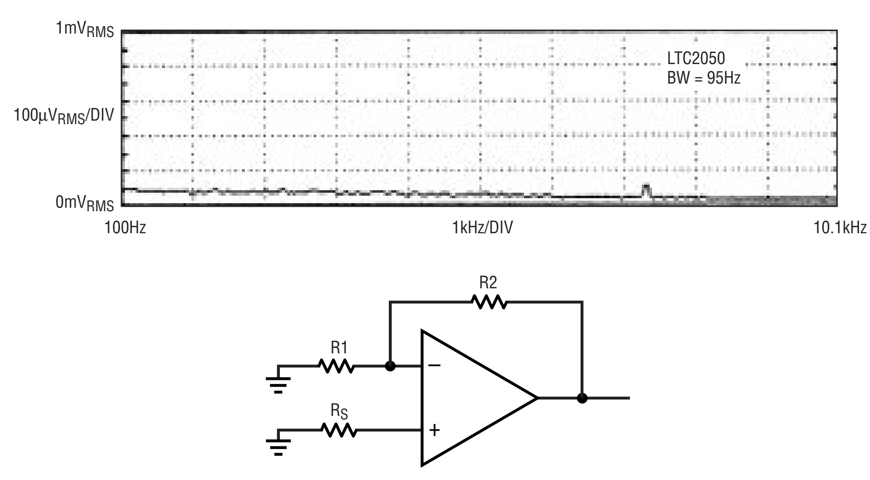


Figure 3. Output spectrum with a gain of 101; R2 = 100k, R1 = R_s= 1k

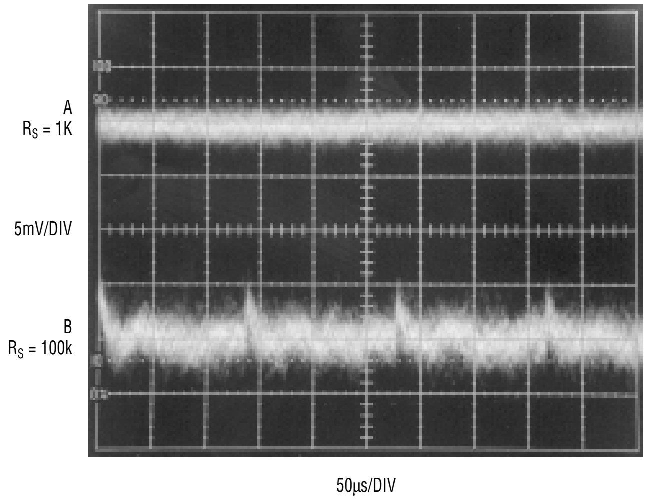


Figure 4. Output with a gain of 101; V_S = 5V, R2 = 100kΩ, R1 = 1kΩ, input common mode at V^-; trace A: R_S = 1kΩ, trace B: R_S = 100kΩ

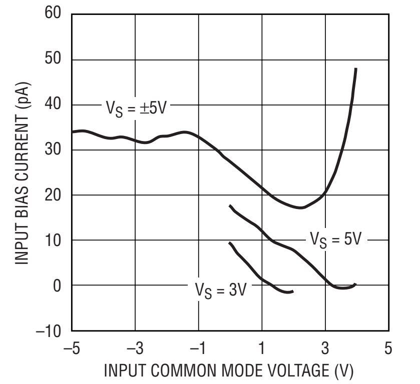


Figure 5. Input bias current vs input common mode voltage (LTC2050HV)

feedthrough is independent of input source resistance or gain setting resistors. Figure 3 shows the output spectrum of the LTC2050 with a closed-loop gain of 101 with R2 = 100k, and R1 = R_S = 1k. There is a residual clock feedthrough of less than 1µV_{RMS}, input referred, at 7.5kHz. This very low clock feedthrough is achieved in the LTC2050/LTC2051/LTC2052 by internal circuitry that improves settling of the internal auto-zero storage capacitors.

The second form of clock feedthrough is caused by the charge injection of the internal MOS switches connected to the op amp inputs. These current spikes are not evident in the output when the source resistance of the op amp inputs are small (that is, R1 and R_S are small in Figure 3). Figure 4 shows the output of the LTC2050HV operating with a gain of 101, 5V supply and the input common mode level at the negative supply (ground). Trace A shows the output when the source resistance (R_S) is 1k, whereas trace B shows the output for R_S = 100k. The charge injection of the input switches appears in the high input-resistance case. However, the average value of the charge injection current (which is the input bias current) is less than 15pA, as shown in Figure 5. Therefore, even with 100k source resistance, the spikes in Figure 4, trace B can be reduced to 1.5µV input-referred DC with a feedback capacitor across R2.

High Resistance Bridge Amplifier Application

A very common application of zero drift amplifiers is amplifying signals from a differential resistive bridge, as shown in Figure 6. The gain is 2R2/R, where R is the bridge resistance. In applications where the bridge resistance is high, input bias current of the op amp can cause errors. With 5V supplies, the LTC2050HV typically has 5pA of input bias current at mid-supply (see Figure 5). Therefore, bridge resistances as high as 100k contribute less than 1µV of additional offset due to input bias current and bridge resistance.

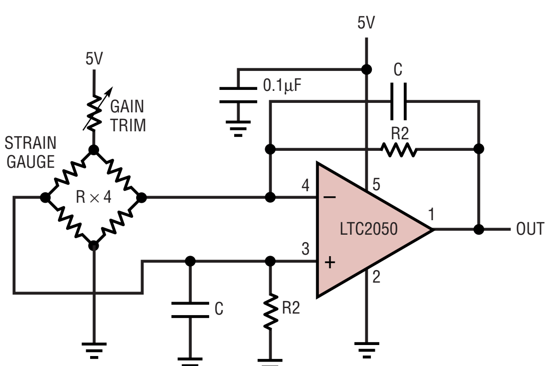


Figure 6. Typical differential bridge amplifier

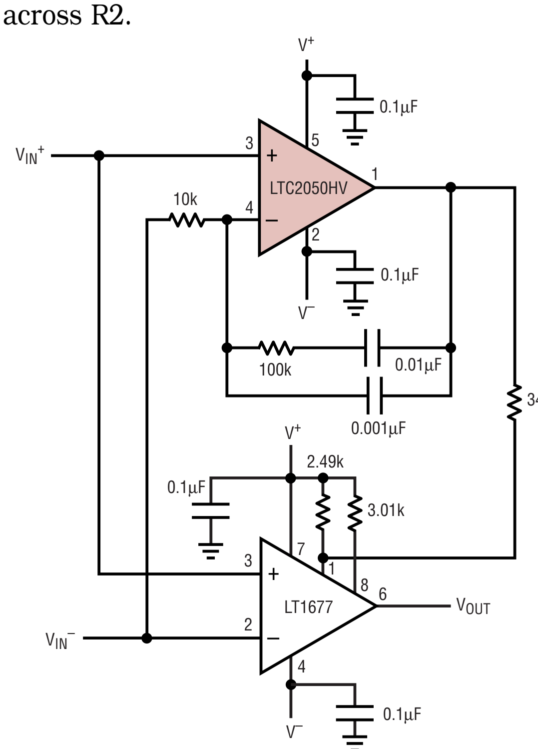


Figure 7. Zero drift, low noise composite operational amplifier

Ultralow V_{OS} Drift, Low Noise Composite Amplifier

The LTC2050 family of amplifiers has about 1.5µV peak-to-peak noise between DC and 10Hz. If an application needs less noise but requires the LTC2050's DC performance, a composite amplifier such as the one shown in Figure 7 may be the solution.

The LT1677 is a low noise rail-to-rail input and output op amp that operates over a very wide supply range (3V to ±15V). The integrator formed by the LTC2050HV nulls the offset of the composite amplifier via the offset trim pins of the LT1677. The resulting offset and drift are those of the LTC2050HV but the noise is close to that of the LT1677 (about 100nV peak-to-peak, DC to 10Hz). With the values shown, the warm-up time is about ten seconds.

Negative Supply-Current Monitor

Figure 8 shows the LTC2051 being used to sense the current in the negative power supply. The low offset of the LTC2051 allows the use of a very small sense resistor, R_S. The output is level shifted to ground using M1.

Conclusion

The LTC2050/LTC2051/LTC2052 family of zero-drift operational amplifiers offer smaller packages than any other operational amplifiers with their DC specifications. In addition, they are the first to run on single 2.7V supplies, yet are capable of operation with higher ±5 supplies.

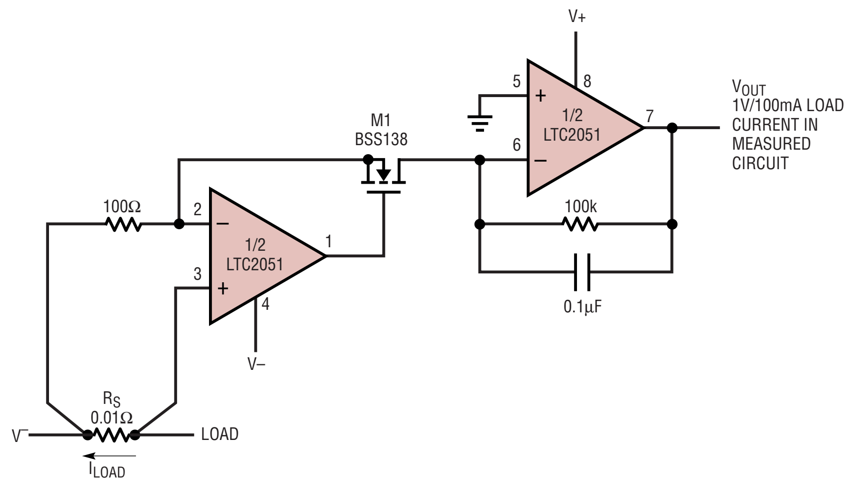


Figure 8. Negative supply current monitor

LT1806/LT1809, continued from page 10

can cause grief to upstream circuitry unless means are taken to attenuate it. The LT1809 performs admirably in this task. Tracing the reverse signal path from the LTC1420, C1 serves as a storage capacitor and R3 limits the glitch current into the LT1809's output. The LT1809's collector output stage incorporates proprietary local feedback to reduce its output impedance (about 20Ω at 100MHz) and this helps attenuate the glitch as well. However, a remnant glitch persists and works its way through R2 and R1, being attenuated by a factor of 2 in the process, and arrives at the LT1809 inverting input. For best performance, the amplitude of the glitch at this point should have been reduced to several millivolts. If it is larger than about 25mV, the rule-of-thumb for BJT differential pairs, the input stage will begin to be driven outside of its linear region and excess distortion will result. The excellent results of Figure 10 indicate that the circuit is not suffering from this effect.

Conclusion

The LT1806 and LT1809 provide complementary solutions for high speed, low voltage signal conditioning. The LT1806, with its low voltage noise of $3.5nV/\sqrt{Hz}$ and a maximum offset voltage of 550µV, is ideal for applications requiring low noise or DC precision, whereas the LT1809 provides the ultimate in distortion performance. The rail-to-rail inputs and outputs of the devices maximize dynamic range and can simplify designs by eliminating the need for a negative supply. This combination of features in a SOT-23 package makes the devices a top choice for handling the challenges of low voltage signal conditioning.

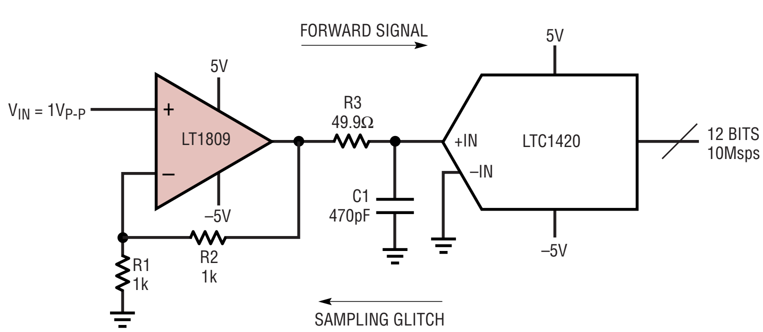


Figure 9. High speed ADC driver

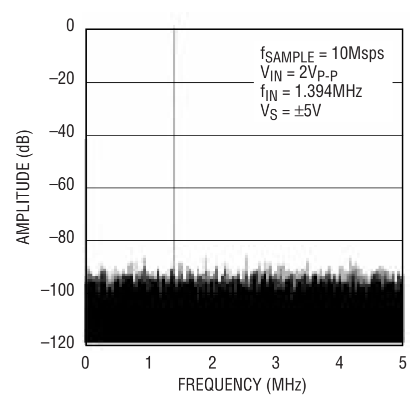


Figure 10. 4096 point FFT of the 12-bit ADC's output

Low Dropout Linear Li-Ion Charge Controllers Prevent Overcharging, Save Board Space

by James Herr

Introduction

Lithium-ion (Li-Ion) batteries are the power source of choice for today's small handheld electronic devices due to their light weight and high energy density. There are a number of difficulties involved in charging these batteries. If overcharged, they can become hazardous to users.

The LTC1731/LTC1732 are constant-current/constant-voltage linear charger controllers for single-cell lithium-ion batteries. Output voltage accuracy is 1% (max) over the –40°C to 85°C range, thus preventing the possibility of overcharging. The output float potential is internally set to either 4.1V or 4.2V for the LTC1731 and is pin selectable for the LTC1732, eliminating the need for an expensive external 0.1% resistor divider. The charging current is user programmable with 7% accuracy. The small size of the LTC1731 and LTC1732, along with the small number of external parts required, makes them ideal for use in portable and handheld products, where board space is at a premium.

At the beginning of the charging cycle, if the battery voltage is low (less than 2.457V), the LTC1731/LTC1732 will precharge the battery with 10% of the full-scale current to avoid stressing the depleted battery. Charging is terminated by a user-programmed timer. After the timer has run out, the charging can be restarted by removing and reapplying the input voltage source or by shutting down the part momentarily. A built-in end-of-charge (**C**/10) comparator indicates that the charging current has dropped to 10%

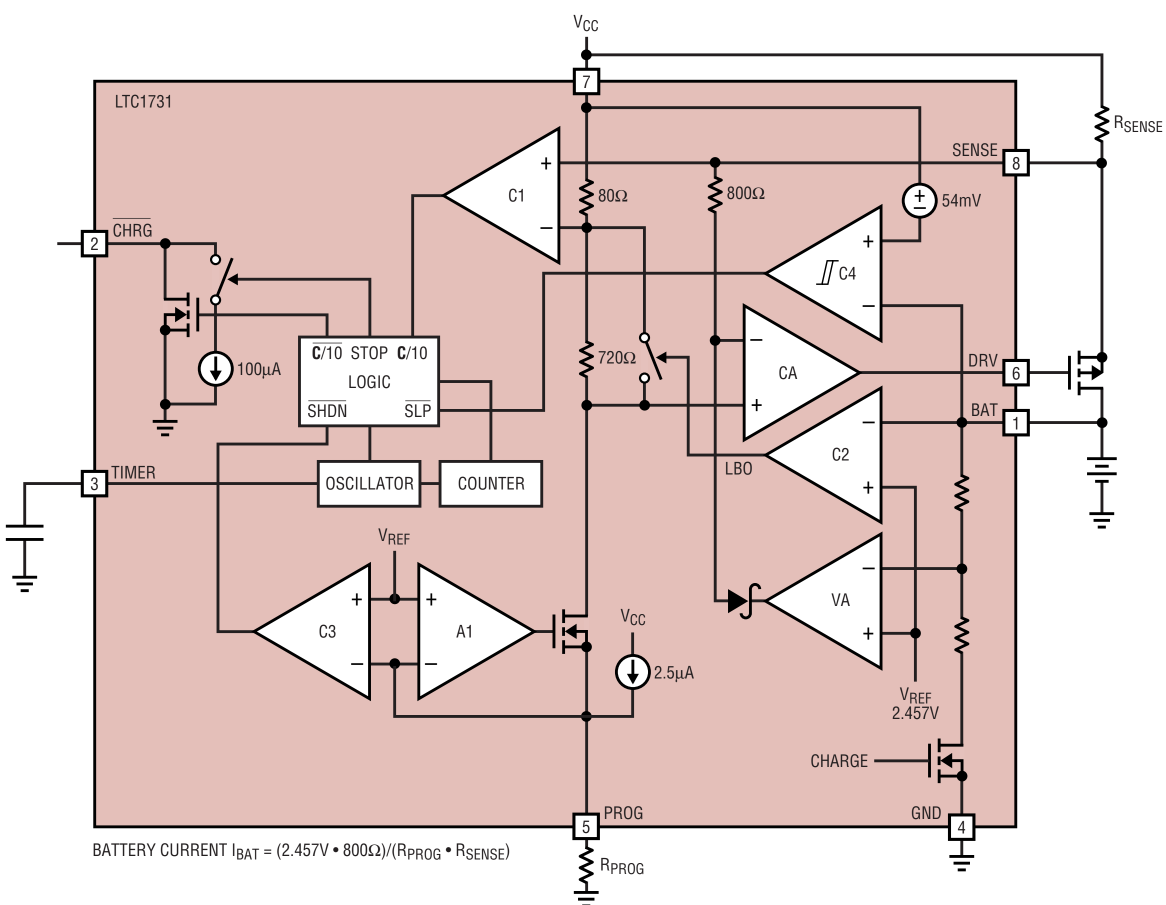


Figure 1. LTC1731 block diagram

of the full scale current. The output of this comparator can also be used to stop charging before the timer runs out.

The LTC1731 is available in the 8-pin MSOP and SO packages, whereas the LTC1732 is available in the 10-pin MSOP package.

LTC1731/LTC1732 Features

The LTC1731 and LTC1732 provide the following features:

- ❏ Complete linear charger controller
- ❏ 1% voltage accuracy
- ❏ Preset 4.1V or 4.2V output versions
- ❏ Programmable charge termination timer
- ❏ Programmable charge current
- ❏ **C**/10 charge current detection output
- ❏ Automatic sleep mode when input supply is removed
- ❏ Automatic trickle charging of low voltage cells
- ❏ Low dropout
- ❏ Select pin to set either 4.1V or 4.2V (LTC1732)
- ❏ Battery insertion detect and automatic low battery charging (LTC1732)

Circuit Description

Figure 1 is a block diagram of the LTC1731. The charge current is programmed by the combination of a program resistor, R_{PROG}, and a sense resistor, R_{SENSE}. R_{PROG} sets the programming current through an internal, trimmed 800Ω resistor, setting up a voltage drop from V_{CC} to the input of the current amplifier (CA). The current amplifier controls the gate of an external P-channel MOSFET to force an equal voltage drop across R_{SENSE}, which, in turn, sets the charge current. When the potential at the BAT pin approaches the preset float voltage, the voltage amplifier (VA) starts sinking current, which decreases the required voltage drop across R_{SENSE}, reducing the charge current.

Charging begins when the potential at the V_{CC} pin rises above the UVLO level and a program resistor is connected from the PROG pin to ground. At the beginning of the charge cycle, if the battery voltage is below 2.457V, the charger goes into trickle charge mode. The trickle charge current is 10% of the full-scale current. If the battery voltage stays low for one quarter of the total programmed charge time, the charge sequence will be terminated.

The charger goes into the fast-charge, constant-current mode after the voltage on the BAT pin rises above 2.457V. In constant-current mode, the charge current is set by the combination of R_{SENSE} and R_{PROG}. When the battery approaches the final float voltage, the voltage loop takes control and the charge current begins to decrease. When the current drops to 10% of the full-scale charge current, an internal comparator turns off the pull-down N-channel MOSFET at the $\overline{CHRG}$ pin and connects a weak current source to ground to indicate an end-of-charge (**C**/10) condition.

An external capacitor on the TIMER pin sets the total charge time. After a time-out occurs, the charging is terminated immediately and the $\overline{CHRG}$ pin is forced to a high impedance state. To restart the charge cycle, simply remove the input supply and reapply it or float the PROG pin momentarily.

For batteries such as lithium-ion that require accurate final float potential, the internal 2.457V reference, voltage amplifier and the resistor divider provide regulation with better than 1% accuracy. For NiMH and NiCd batteries, the LTC1731/LTC1732 can be turned into a current source by connecting the TIMER pin to V_{CC}. When in the constant-current only mode, the voltage amplifier, timer and the trickle charge function are disabled.

When the input voltage is not present, the charger goes into a sleep mode, dropping I_{CC} to 7µA. This greatly reduces the current drain on the battery and increases the standby time. The charger can be shut down by floating the PROG pin. An internal current source will pull this pin's voltage high and clamp it at 3.5V.

The LTC1732 is equipped with an AC power ($\overline{ACPR}$) pin to indicate that the input supply (wall adapter) is applied and above the undervoltage lockout level. The SEL pin allows users to set the final float potential of the battery to either 4.1V or 4.2V. The LTC1732 also has an internal comparator that monitors the battery potential and turns the charger back on when V_{BAT} drops below 3.8V. This feature will keep the battery near fully charged after a time-out has occurred while the battery remains inserted.

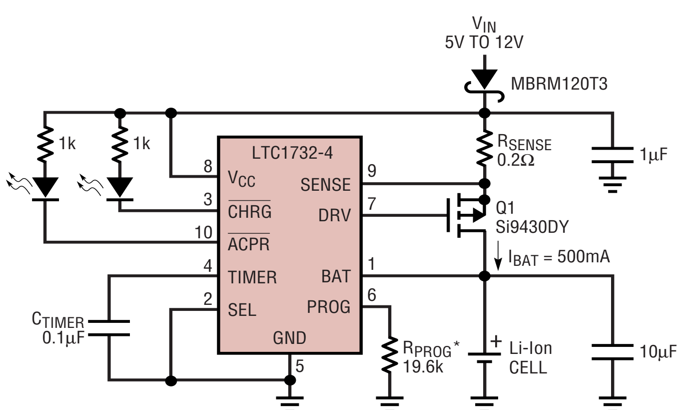


Figure 2. LTC1732-4 5V to 12V in, single-cell Li-Ion charger

Programming Charge Current

The formula for the battery charge current is:

$$I_{BAT} = (I_{PROG}) \bullet (800\Omega/R_{SENSE})$$
$$= (2.457V/R_{PROG}) \bullet (800\Omega/R_{SENSE})$$

where R_{PROG} is the total resistance from the PROG pin to ground.

For example, if a 500mA charge current is needed, select a value for R_{SENSE} that will drop 100mV at the maximum charge current.

$R_{SENSE} = 0.1V/0.5A = 0.2\Omega$,
then calculate:
$R_{PROG} = (2.457V/500mA) \bullet (800\Omega/0.2\Omega) = 19.656k$

For best accuracy over temperature and time, 1% resistors are recommended. The closest 1% resistor value is 19.6k.

Typical Applications

500mA Single-Cell Linear Battery Charger

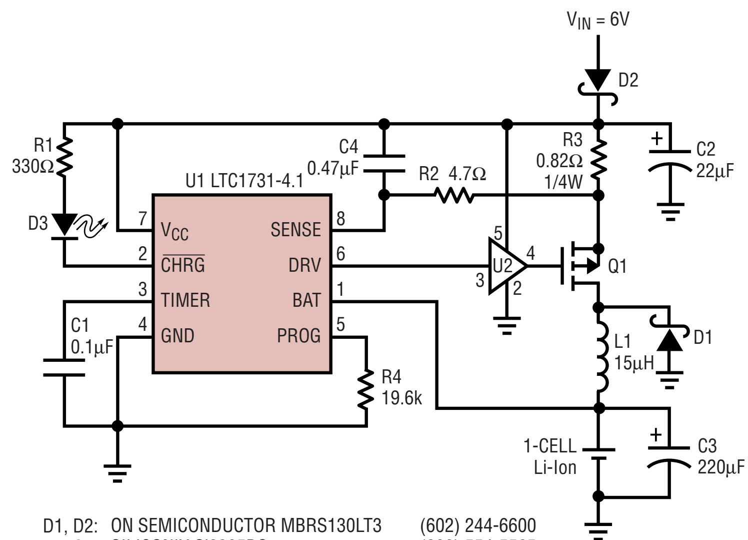
Figure 2 shows a typical single-cell battery charger using the LTC1732-4 with a 5V to 12V input range and a 500mA charging current. A program resistor (R_{PROG}) sets a 100mV voltage drop across the sense resistor (R_{SENSE}). With $R_{SENSE} = 0.2\Omega$, the charging current is set at 500mA. When the battery voltage rises to the preset level of 4.1V, the LTC1732 goes into constant voltage mode and the charging current is gradually reduced. When the charging current reaches 10% of the full-scale current, the $\overline{\text{CHRG}}$ pin output switches from a strong N-channel MOSFET pull-down to a weak 25µA pull-down current source to indicate the **C**/10 condition. Once the timer runs out (three hours), the DRV pin is pulled high and the $\overline{\text{CHRG}}$ pin output goes to a high impedance state. The SEL pin is shorted to ground to set the final battery float potential to 4.1V.

1.5A Single-Cell Battery Charger

The LTC1731 can also be connected as a switcher-based battery charger for higher charging current applications (see Figure 3). As in the linear charger, the charge current is set by R3 and R4. The $\overline{\text{CHRG}}$ pin output will indicate an end-of-charge (**C**/10) condition when the average current drops down to 10% of the full-scale value. A 220µF bypass capacitor is required at the BAT pin to keep the ripple voltage low.

Conclusion

The LTC1731 makes a very compact, low parts count and low cost lithium-ion battery charger. The onboard programmable timer provides charge termination without interfacing to a microprocessor.



D1, D2:	ON SEMICONDUCTOR MBRS130LT3	(602) 244-6600
Q1:	SILICONIX Si2305DS	(800) 554-5565
L1:	SUMIDA CDRH6D28-150NC	(847) 956-0666
U2:	TEXAS INSTRUMENTS TPS2829DBVR	(800) 477-8924

Figure 3. The LTC1731 configured as a switcher-based charger for higher current applications

Authors can be contacted at (408) 432-1900

SwitcherCAD III Provides Fast Spice Simulation of Switching Regulators and Built-In Schematic Capture

by Keith Szolusha and Robert Sheehan

Introduction

SwitcherCAD III is Linear Technology's new SPICE and schematic capture program that has the full functionality of commercial SPICE. SCAD III also contains primitives and macromodels for LTC switching regulators, enabling users to perform quick-and-easy simulations of switch-mode regulator circuits. This Windows®-based switching regulator SPICE tool is even available for free Internet download. Existing part libraries feature over seventy of LTC's integrated circuits, including but not limited to, LTC's switching regulators. LTC's proprietary, high speed, mixed-mode simulation method enables the simulation of in-depth models of switching regulators that was previously much more complicated and time-consuming. A simple switching regulator steady state, start-up or load-transient SPICE analysis can be completed in minutes rather than hours. Behavioral-level modeling compatible with industry standard SPICE programs is twice as fast in SCAD III. For users unfamiliar with either SPICE tools or circuit design, there are currently over twenty fully functional demonstration circuits available. More advanced users can design and simulate custom circuits from scratch in the same fashion as in commercial SPICE programs. A field update utility provides lifetime free downloads of the latest version of SCAD III and new models from the Internet. This allows users to quickly update their circuits with new regulators as soon as they are introduced.

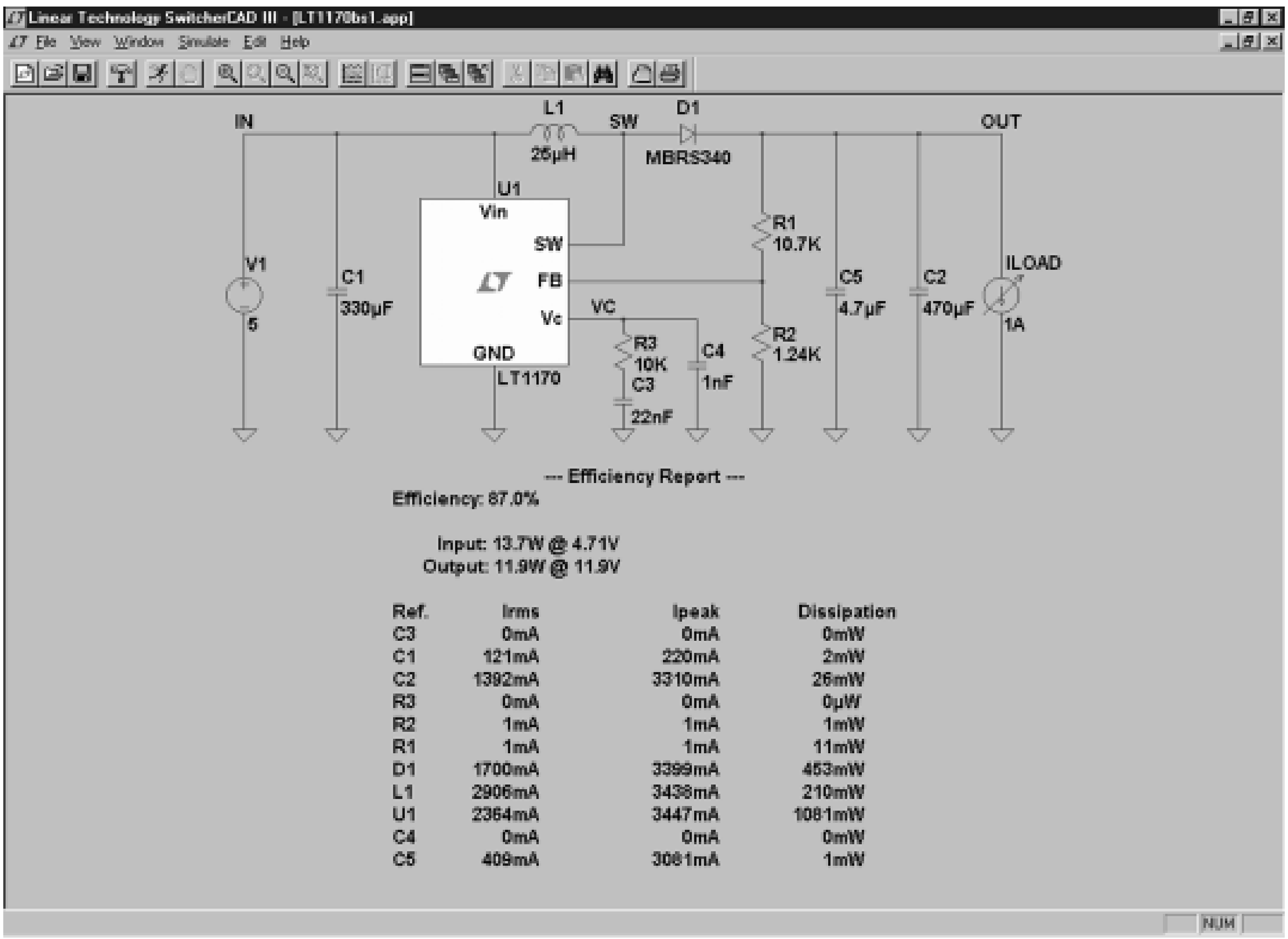


Figure 1. SCAD demonstration circuit: LT1170, 5V to 12V/1A 100kHz, high efficiency application

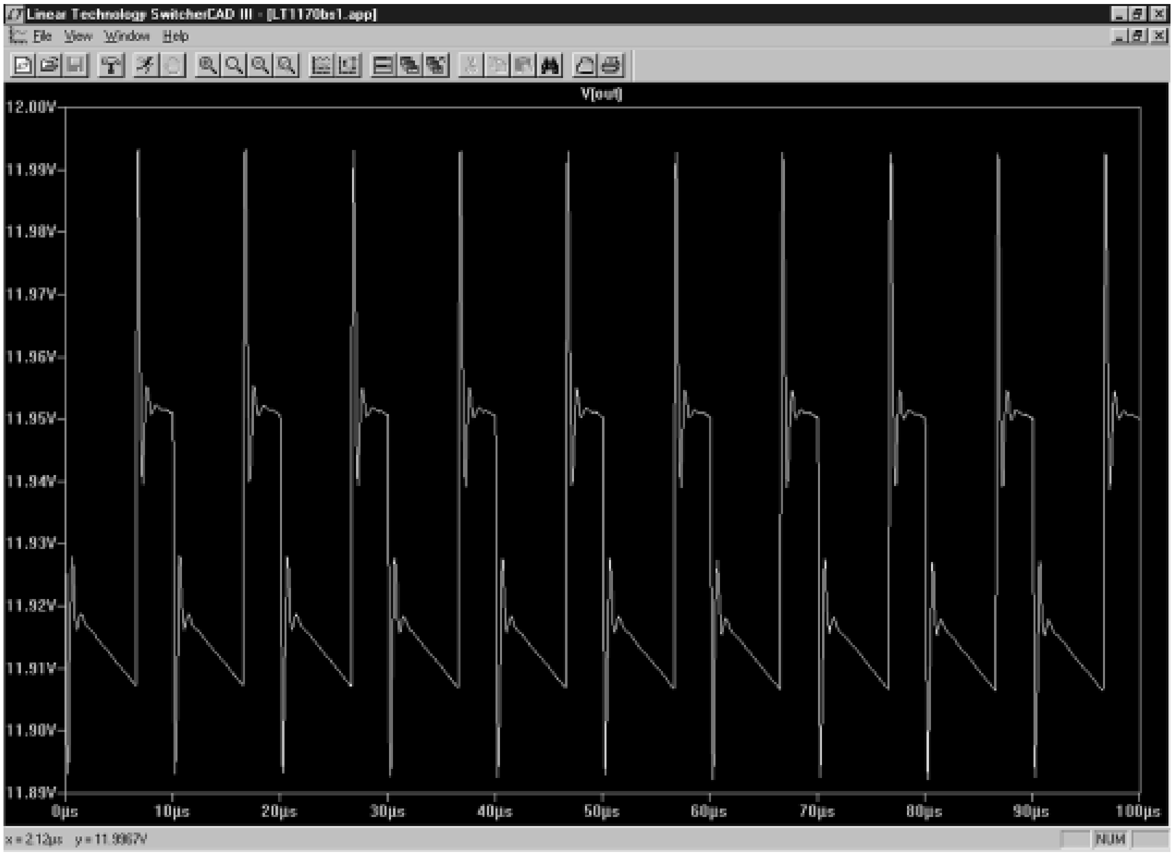


Figure 2. SCAD III steady-state analysis of LT1170, 5V to 12V/1A 100kHz, high efficiency application

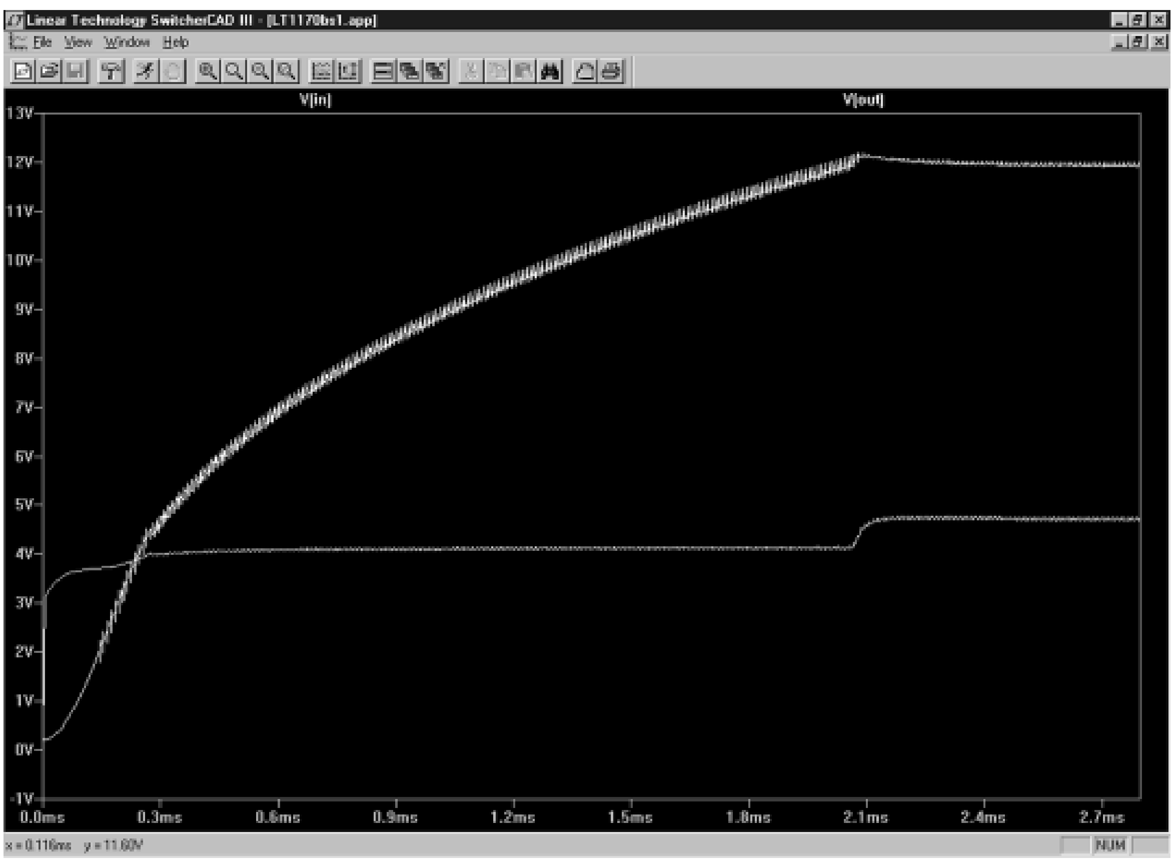


Figure 3. SCAD III start-up transient waveform for LT1170, 5V to 12V/1A 100kHz, high efficiency application

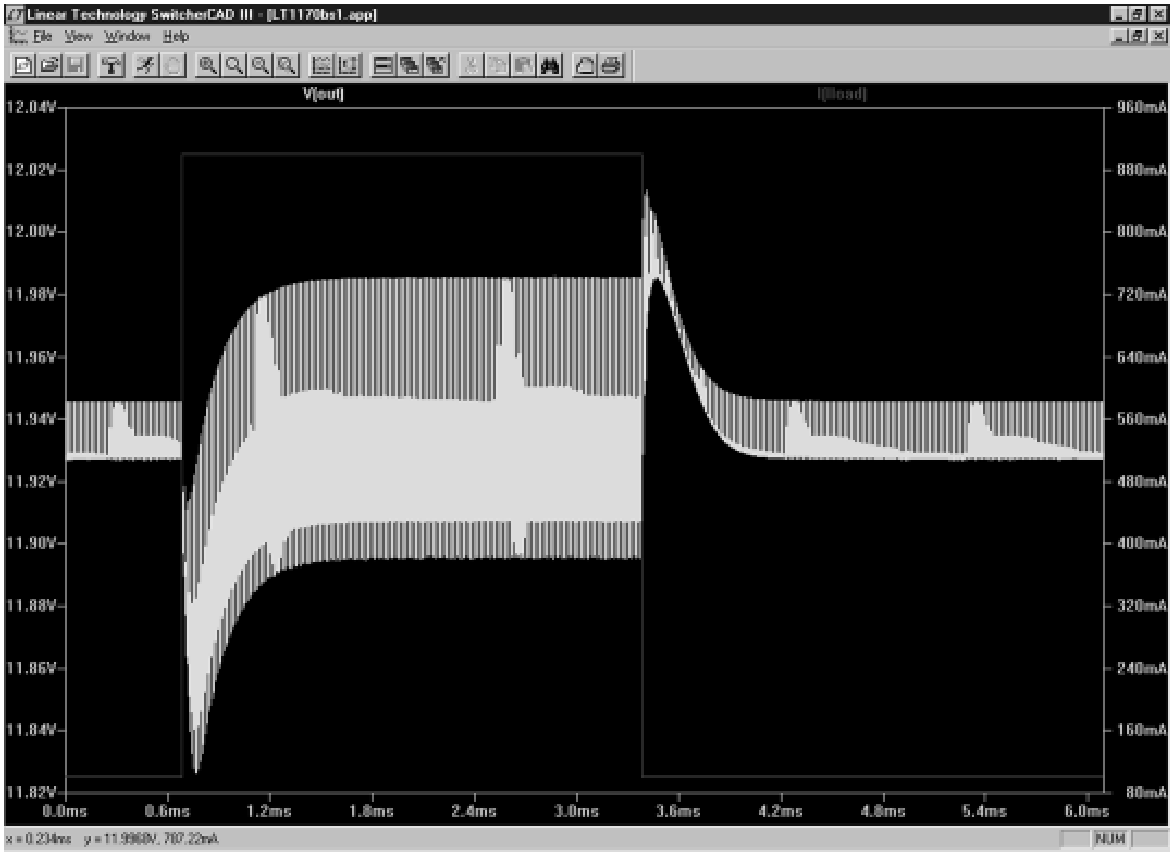


Figure 4. SCAD III step-response waveform for LT1170, 5V to 12V/1A 100kHz, high efficiency application

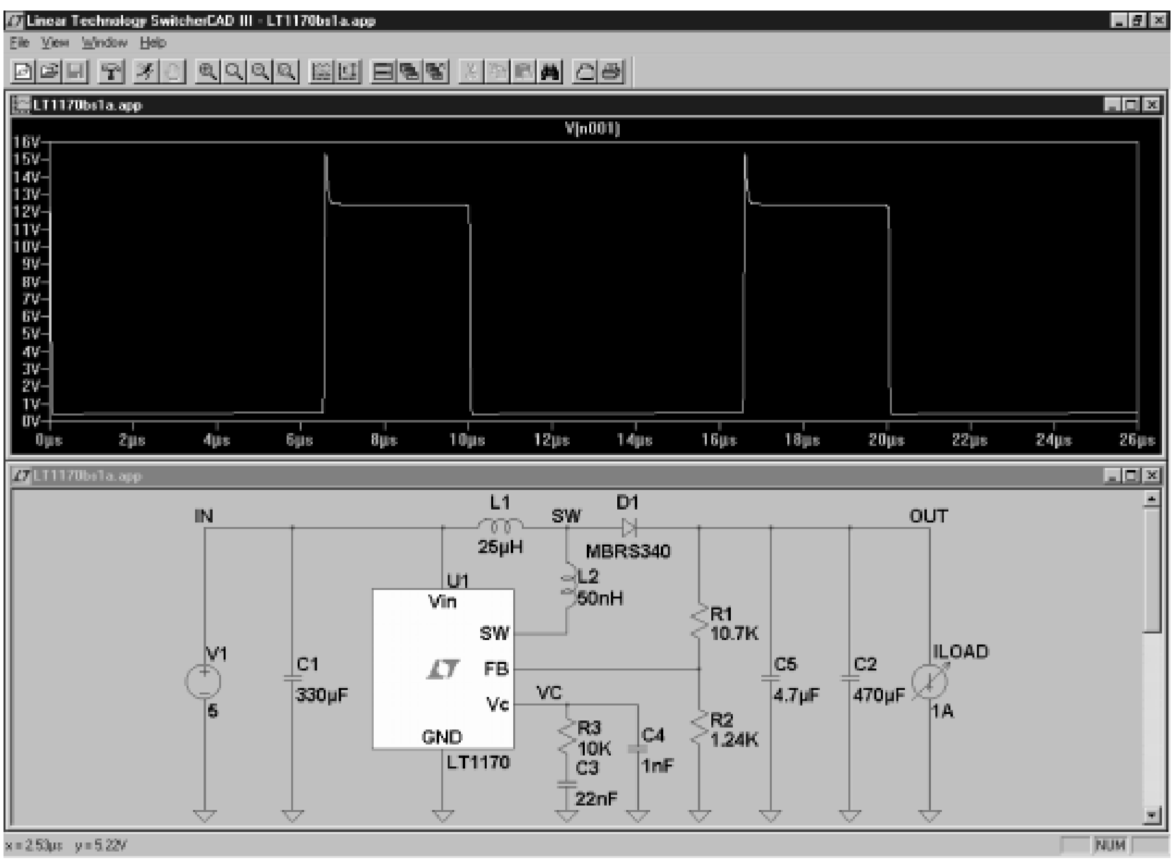


Figure 5. Voltage spike at the switch node on the LT1170 chip resulting from the inclusion of 50nH of lead and wiring inductance (V[n001] in the switch node at the chip shared by the LT1170 and L2)

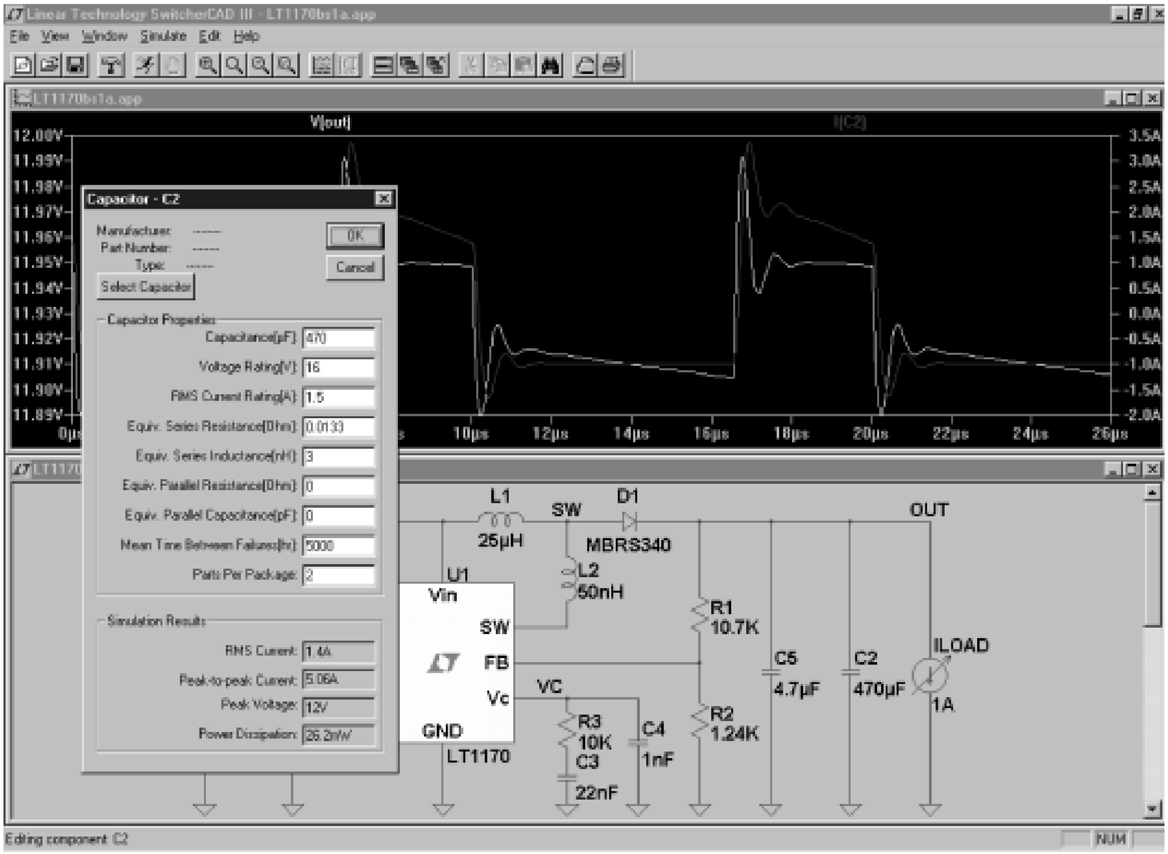


Figure 6. The resulting voltage and current ringing effects of changing the parasitics in a typical capacitor (C2) can be seen.

Demonstration Models

SCAD III currently provides over twenty demonstration circuits for many of LTC's most popular DC/DC switching regulators. One example is the LT1170 5V to 12V, 1A, 100kHz, high efficiency application shown in Figure 1. The efficiency report included in the schematic is generated upon completion of the steady-state analysis. Upon selecting one of the available demo applications, SCAD III displays the schematic of the circuit and immediately performs a steady-state analysis, as shown in Figure 2.[1] An efficiency report, including RMS and peak currents as well as power dissipation in each component, is displayed in the schematic window. The "Start Up Transient" and "Step Response" waveforms in Figures 3[2] and 4,[3] respectively, are simulated by simply selecting either one from the "Simulate" pull-down menu. These application schematics can be easily modified, edited and resimulated in order to explore custom variations.

Custom Designs

For the more advanced SPICE engineer or switching regulator designer, new schematics can be created from scratch by selecting "New Schematic" under the "File" pull-down menu. Components, wires and new SPICE directives can all be added to the schematic by clicking the appropriate selection on the "Edit" menu. Note that SCAD III does not serve as a guide for selecting the most appropriate switching regulator. The user must have previous knowledge of the components chosen from LTC data sheets, application notes or other reliable sources. All of the necessary publications for selecting necessary switch-mode power supply components, such as data sheets and application notes, are available for free on LTC's website (www.linear-tech.com).

When editing custom designed .asc files, as opposed to the provided .app demonstration circuits, choosing "Run" from the "Simulate" pull-down menu generates the user-specified SPICE simulation.

As SCAD III performs its calculations and simulations, you can view the desired waveforms being created on the screen. The simulation process, such as finding a steady-state output, is much faster than in previous SPICE programs. SCAD III is fast enough that the computer need not run overnight to generate a steady-state waveform.

Real Circuit Parasitics

For in-depth design analysis, SCAD III makes it simple for the engineer to include the parasitic aspects of real components, such as the series resistance and series inductance of capacitors. Figure 5 demonstrates the use of a series inductor to simulate the lead and wiring inductance of a real circuit. Note the 50nH inductor, L2, in series with the switch node of the regulator and the voltage spike

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A New, Fully Differential, No Latency Delta-Sigma ADC Family

by Michael K. Mayes

Introduction

In recent years, Linear Technology has introduced a family of high resolution delta-sigma analog-to-digital converters. Originating from the LTC2400, this product family features high accuracy (10ppm total error), ease of use (8-pins, on-chip oscillator, no latency) and low drift (user-transparent offset/full-scale calibration). This product family includes single-ended one-, two-, four- and eight-channel input devices with user-selectable 50Hz or 60Hz line-frequency rejection.

A new family of differential-input delta-sigma analog-to-digital converters is introduced here. These converters offer features similar to those of the previous family, with the addition of differential input and differential reference. All devices offer compatible timing and interface with the original LTC2400, as well as transparent calibration, no latency, on-chip oscillator and wide supply (2.7V–5.5V), input and reference ranges.

The first part, the LTC2410, features 0.1ppm offset error, 2ppm INL, 0.16ppm RMS noise, and a common mode reference/input range of GND to V_{CC}, all in a GN-16 package. The second part, The LTC2411, is packaged in a tiny 10-pin MSOP package with differential input and differential reference. The third part, the LTC2413, offers simultaneous 50Hz and 60Hz rejection and is pin and performance compatible with the LTC2410.

These new differential delta-sigma devices are presented here in applications exemplifying their performance and ease-of-use, including a full-bridge digitizer, a DC-accurate digital voltmeter (DVM), a remote 4-wire half-bridge interface and an application that features simultaneous 50Hz/60Hz rejection.

Full-Bridge Digitizer

As shown in Figure 1, the LTC2410 (the LTC2413 can be substituted in any LTC2410 application) directly interfaces to a 4- or 6-terminal bridge. Its small size (GN-16, the same footprint as an SO-8) and the ease-of-use (no external oscillator, no user calibration required, 10nV/°C offset drift) allow the LTC2410 to be incorporated inside a load-cell body. This replaces long analog wiring with a 2- or 3-wire digital interface, simplifying input protection, RFI suppression and errors associated with these wires.

The LTC2410/LTC2413 noise performance is 800nV$_{RMS}$ with a 5V reference (22.6 noise-free bits). The typical bridge produces 2mV/volt of excitation, corresponding to a full-scale output of 10mV. The LTC2410 produces over 12,000 counts for this range without the added complexity of a programmable gain amplifier (PGA), offset calibration, full-scale calibration or external amplification. The absolute accuracy (offset + full-scale + linearity) of the LTC2410 is 3 parts per million, independent of the supply voltage and ambient temperature. This allows the user to reliably average multiple readings from the LTC2410. As a result, over 100,000 counts can be obtained by averaging 64 samples.

Digital Voltmeter (DVM)

An analog-to-digital converter used as the front end of a digital voltmeter requires excellent linearity and low noise over a wide dynamic range. Additionally, the converter's offset error, offset drift, full-scale error and full-scale drift are critical to the overall performance. The LTC2410 offers 2ppm linearity with 0.16ppm$_{RMS}$ noise over the complete 5V input range. The part offers 0.1ppm offset with 10nV/°C drift and 2.5ppm full-scale accuracy with 0.03ppm/°C drift. With

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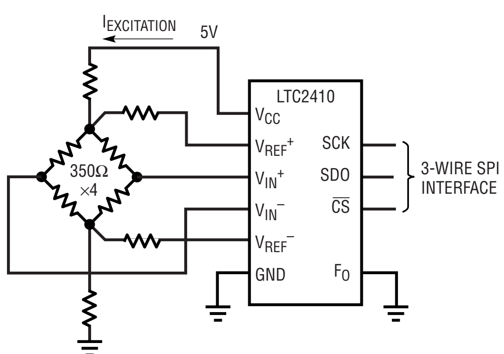


Figure 1. Direct bridge connection

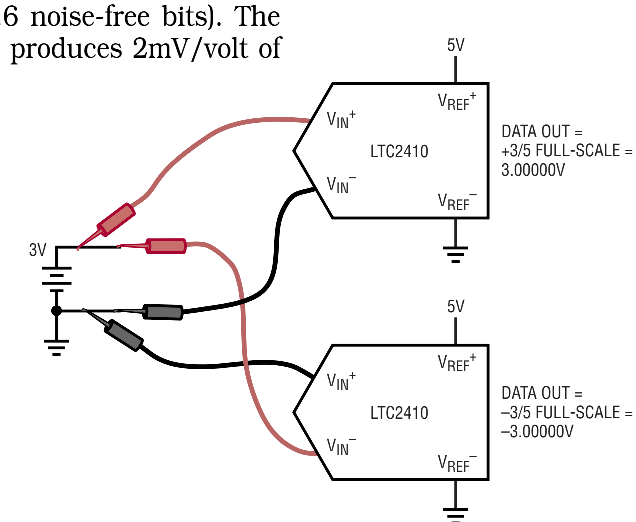


Figure 2. DVM lead-reversal experiment

Dual 60µA 10-Bit Serial DAC in MS-8 Saves Power and Space

by Vic Schrader

Introduction

The LTC1661 is a dual, serially addressable 10-bit, rail-to-rail voltage output DAC with Sleep mode. Operating on a single 2.7V–5.5V supply rail, its small size and low power consumption make it most appropriate for use in products with stringent space and/or power constraints. In the 8-lead MSOP package, it occupies just 0.02in^2 of board space, 50% less area than a standard SO-8 package; each buffered DAC draws just 60µA of supply current at 5V (48µA at 3V). Sleep mode operation further reduces total supply-plus-reference current to just 1µA.

The LTC1661 has a reference-to-output gain of one and the REF pin can be tied to V_{CC} for ratiometric, 0V-to-V_{CC} output without the use of a separate reference. Each of the output amplifiers is stable driving capacitive loads of up to 1000pF, so the designer need not be concerned with the capacitance of long board traces. The serial interface is SPI/MICROWIRE™-compatible and uses a simple, flexible control word that allows the addressing of individual DACs; the data path is double buffered to allow for simultaneous updates. The digital inputs have internal Schmitt triggers, which eliminate the need for external Schmitts when the input signals are slow or noisy, such as when using optoisolators. The block diagram of the LTC1661 is shown in Figure 1.

Performance

Load Driving

Despite its tiny operating current, the LTC1661 can deliver substantial load currents; Figure 2 shows output voltage vs load current performance. At V_{CC} = 5V, the LTC1661 can drive over 20mA into a grounded load, the equivalent of driving a 250Ω load over the full 0V-to-V_{CC} range. The output impedance is just 0.5Ω.

The LTC1661 output amplifiers have been optimized for driving capacitive loads (see Figure 3). Capacitances of up to 1000pF, or greater than or equal to 10µF, may be driven directly; in between these values, a small resistor may be inserted in series with the load to successfully drive any capacitance. The example in Figure 3 shows a 20Ω resistor placed in series with a 1µF load to stabilize the combination.

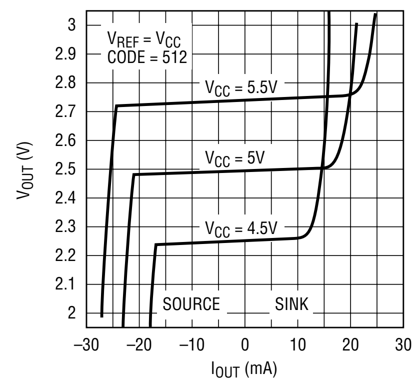


Figure 2. The LTC1661 drives over 20mA into a grounded load at 5V

Linearity

The LTC1661 uses a patented architecture that guarantees monotonicity over the full industrial temperature range. Differential nonlinearity (DNL) is typically ±0.1LSB (±0.75 max) (see Figures 4 and 5).

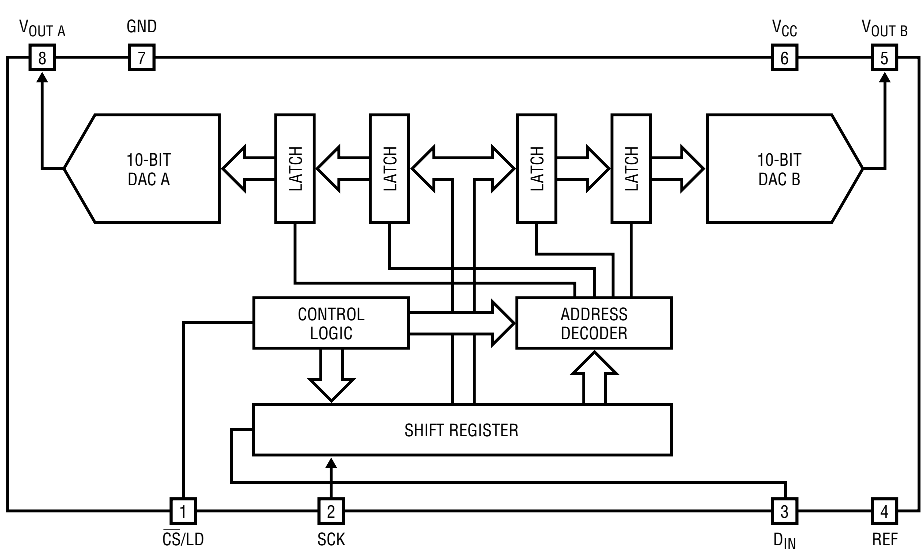


Figure 1. LTC1661 block diagram: each DAC draws just 60µA at 5V. Double-buffered input logic allows simultaneous updates.

Operation

Serial Interface

The simple-yet-flexible SPI/MICROWIRE-compatible interface uses a 16-bit input word, which is divided into Control and Data sections (see Figure 6). The Control section of the word specifies the desired operation and selects one or both DACs to receive the instruction, whereas the Data section specifies the DAC input code. Data is captured on the rising edge of the clock with $\overline{CS}$/LD held at a logic low. Once the full 16-bit word has been captured, the rising edge of $\overline{CS}$/LD executes the instruction.

Conclusion

Low supply current, power-saving Sleep mode and extremely compact size make the LTC1661 ideal for battery-powered devices, while its ease of use, high performance and wide supply range make it an excellent choice for a wide spectrum of voltage adjustment and trimmer potentiometer applications.

MICROWIRE is a trademark of National Semiconductor Corp.

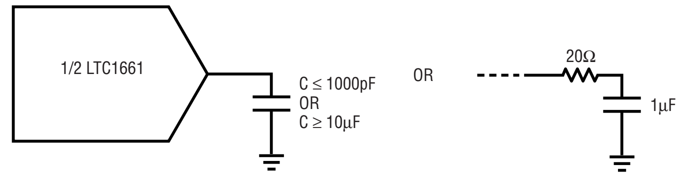


Figure 3. Allowable capacitive loads; the rail-to-rail output amplifiers have been optimized for driving capacitance.

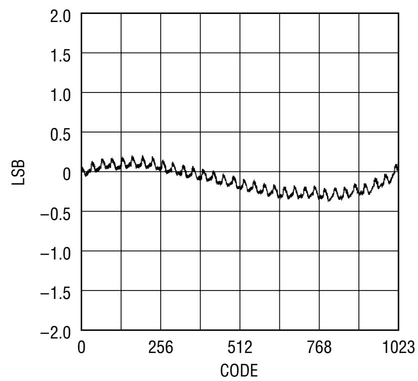


Figure 4. LTC1661 integral nonlinearity (INL)

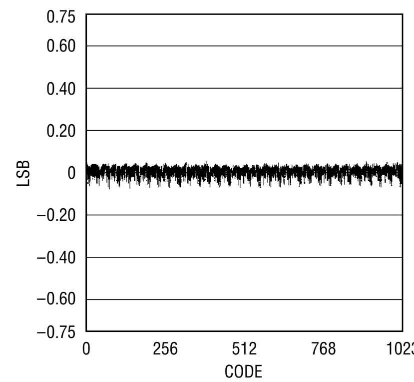


Figure 5. LTC1661 differential nonlinearity; patented architecture guarantees monotonicity

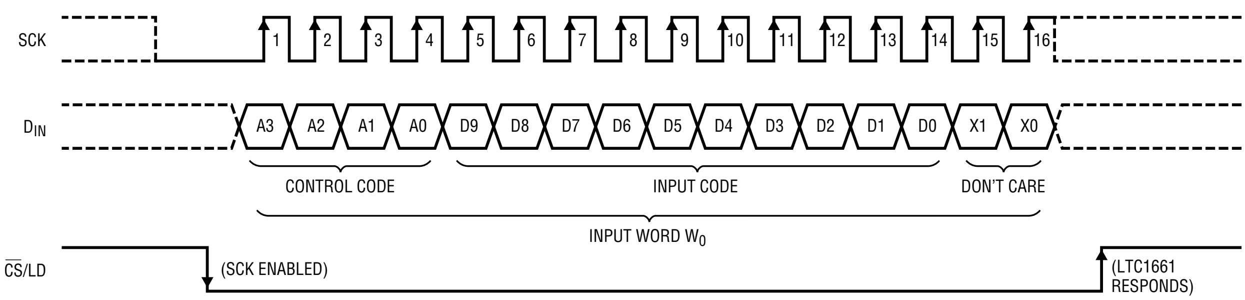


Figure 6. The simple 3-wire interface is used for software control of the individual DAC channels. Loading of input codes, updates and Sleep mode control are all available.

1.25MHz, 1.5A, MS8 Monolithic Step-Down Converter Keeps Switching Noise above the Signal Spectrum

by Karl Edwards

The size of communication devices is shrinking while data rates continue to rise. Building a small, efficient switching power supply in proximity to sensitive signal circuitry is increasingly difficult. The LT1767 has been designed to address this problem. At 1.25MHz, the switching frequency is above the bandwidth of many systems. If needed, the Sync pin can be used to further increase the operating frequency to 2MHz, keeping switching noise out of any particularly sensitive frequency bands. The high switching frequency reduces the size of the input and output filtering components and allows the use of chip inductors, reducing overall system cost. The lower storage requirements of these filters make possible an all-ceramic-capacitor design.

Inside its MS8 package, the LT1767 provides regulation and control circuitry along with a high efficiency 0.22Ω switch. This small-footprint monolithic approach both reduces board space and simplifies associated circuitry. Its wide 2.7V to 25V operating supply range and 1.5A maximum switching current limit makes this part ideal in a wide range of applications. Other useful features of the LT1767 include an internal undervoltage lockout and a shutdown mode that reduces quiescent current to 6µA.

The LT1767 can be used in a variety of high-side switch converter configurations. The circuit shown in Figure 1 is a dual-output SEPIC converter, producing both 5V and –5V using only a single magnetic component. The two inductors shown are wound on a single BH Electronics toroidal core. The topology for the 5V output is a standard buck converter. If C4 were not present, the –5V topology would be a simple flyback winding coupled to the buck converter. C4 creates a SEPIC topology, which improves regulation and helps share current between L1A and L1B. Without C4, the voltage swing on L1B compared to L1A would vary due to relative loading and coupling losses. C4 provides a low impedance path to maintain an equal voltage swing in L1B, improving regulation. Figure 2 shows negative load regulation with constant positive load currents of 100mA, 200mA and 400mA. Positive load regulation error is insignificant at less than 1%. For more information on this circuit, refer to Linear Technology Design Note 100.

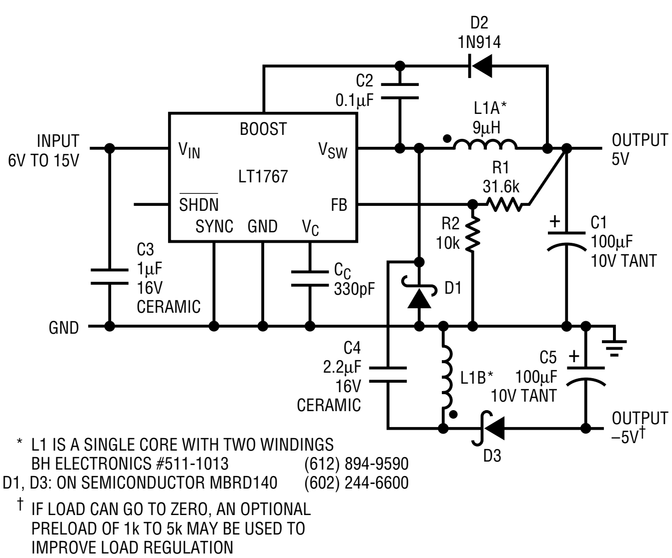


Figure 1. Dual-output SEPIC converter

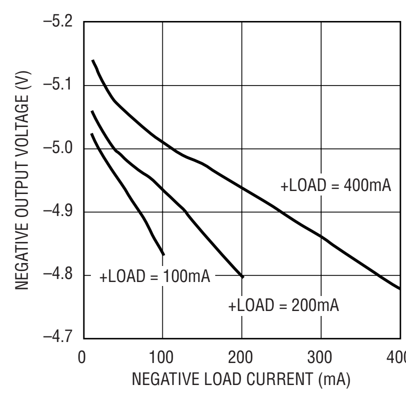


Figure 2. Negative load regulation at several positive loads

Triple, High Output Current Supply Requires only 3.3V Input and Minimal Input Capacitance

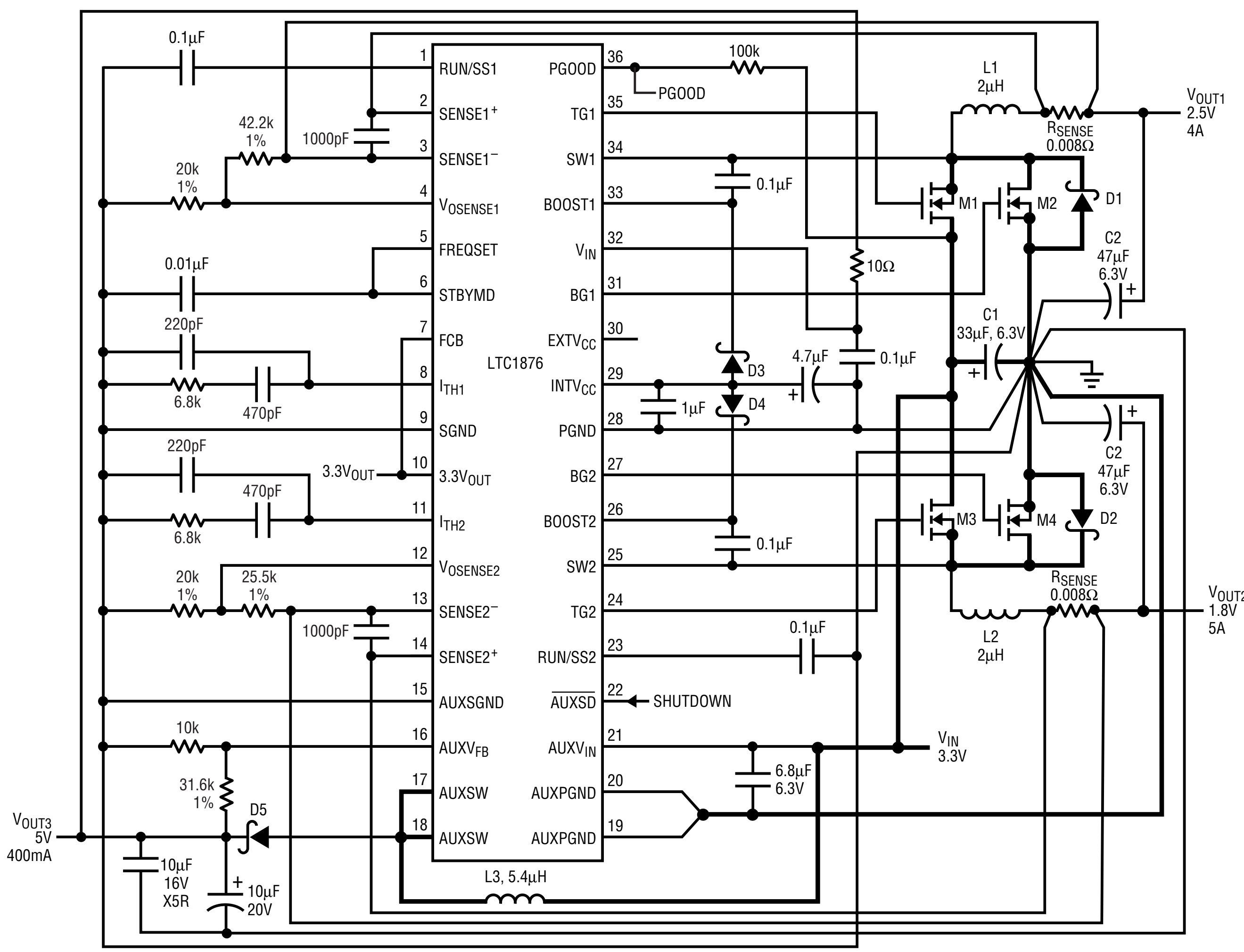
by San-Hwa Chee

Introduction

The LTC1876 is ideally suited for traditional system power supplies, where outputs of 3.3V, 5V and 12V are required from an input ranging from 4.5V to 24V. Another possible configuration allows the LTC1876 to operate from a low 3.3V input supply. The two out-of-phase step-down controllers allow off-the-shelf inductors to be used instead of bulky, custom-wound transformers. The PolyPhase™ architecture of the step-down controllers minimizes input capacitance requirements, reducing overall system cost and footprint. A built-in boost regulator provides a third output.

3.3V Input, 1.8V, 2.5V and 5V Outputs

Figure 1 shows a low input voltage application with the input supply at 3.3V. The boost regulator is set up to provide 5V and is used to power the control circuitry of the step-down controllers and to provide gate drive



M1–M4: FAIRCHILD FDS6912A (408) 822-2126
L1, L2: SUMIDA CEP123-2RO (847) 956-0667
L3: SUMIDA CDRH5D18
C1: PANASONIC EEFCDOJ330R (201) 392-4511
C2: PANASONIC EEFCD0J470R
D1, D2: ON SEMICONDUCTOR BAT54A (800) 282-9855
D3, D4: ON SEMICONDUCTOR MBRM140T3
D5: ON SEMICONDUCTOR MBR0520
THICK TRACES = HIGH CURRENT PATH

Figure 1. Low voltage 3.3V to 1.8V and 2.5V power supply

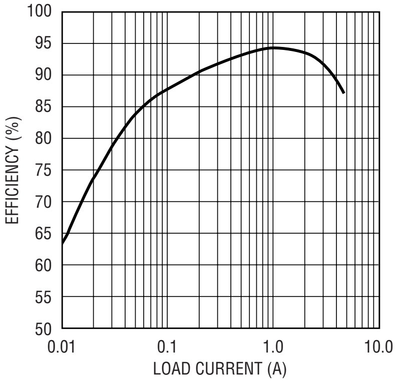


Figure 2. Overall efficiency vs load current for Figure 1's circuit; load current is kept the same for the 1.8V and 2.5V outputs.

voltage to the N-channel MOSFETs. This allows standard logic-level MOSFETs to be used. In addition, the 5V output can also be used for other light loads. The maximum output current that the 5V output can provide is 400mA, including gate-charge currents.

The 3.3V input is converted to 2.5V and 1.8V by the high efficiency controllers. The N-channel MOSFETs, FDS6912As, were selected for both their low gate charge and low $R_{DS(ON)}$ resistance. Due to the use of an out-of-phase topology for the step-down controllers, the ripple current requirement for the input capacitance is minimized. Ceramic capacitors are used to further reduce the ESR, thus reducing ripple voltage and losses. Since the controllers and the boost regulator operate independently, the 5V output can be used to power keep-alive circuitry while the step-down controllers are shut down.

Figure 2 shows the efficiency of Figure 1's circuit. The curve is plotted with the 1.8V and 2.5V outputs loaded with the same amount of current. Figure 3 shows the output voltage ripple for all the outputs, with the 1.8V and 2.5V outputs loaded at 4A.

Conclusion

By using the LTC1876 boost regulator to power the control circuitry and provide the gate drives to its step-down controllers, high efficiency is obtained with a low input voltage supply. Ideally suited for applications that require three different supply voltages, the LTC1876 provides high performance both in low input voltage applications and traditional system power supplies. With its narrow 36-pin SSOP package and its multiphase technology, the LTC1876 provides high performance power supply solutions in a small board space.

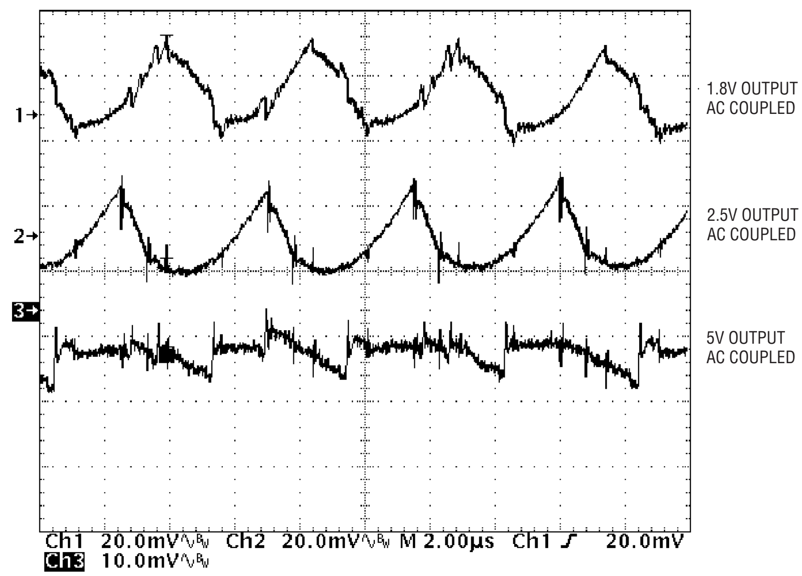


Figure 3. Output voltage ripple for Figure 1's circuit

SCAD III, continued from page 24

that it creates in the switching waveform. This shows why trace lengths should be minimized in a real circuit. The switch voltage rating can be exceeded if the trace length and the subsequent inductance are ignored.

Figure 6 demonstrates the available parasitic characteristics of a typical capacitor. Diodes and inductors also have parasitic elements that can be used to enhance the accuracy of a design. However, setting these parameters increases both the number of calculations performed by SCAD III and the overall simulation time.

Conclusion

SCAD III represents the state-of-the-art in schematic capture/SPICE software. It provides power supply circuit simulation and allows designers of all levels to model switching regulator performance. SCAD III includes, for the first time, black-box switching regulator models that dramatically decrease design and simulation time.

Notes:

[1] Completed in 12 seconds. All times are for a 400MHz Pentium® II PC with 128MB of RAM, under Windows® 98.

[2] 34 seconds to complete.

[3] 1 minute, 44 seconds to complete

Pentium is a registered trademark of Intel Corp.

Windows is a registered trademark of Microsoft Corp.

1.4MHz Switching Regulator Draws Only 10µA Supply Current

by Jaime Tseng

High switching frequencies and low quiescent currents are no longer conflicting requirements in the design of battery-powered products. Linear Technology's LTC3404 is the industry's first step-down switching regulator that runs at 1.4MHz while drawing only 10µA of supply current (using Burst Mode™ operation) at no load. This impressive feat allows for better than 90% efficiency over three decades of output load current while allowing the use of tiny external components. With the on-chip main and synchronous switches, minimal external components are necessary to make a complete, high efficiency (up to 95%) step-down regulator. Low component count and the LTC3404's tiny MSOP package provide a minimum-area solution to meet the limited space requirements of today's portable applications.

The LTC3404 incorporates a constant-frequency, current mode architecture that provides low noise and fast transient response. Its input voltage supply range of 2.65V to 6V and 100% duty cycle capability for low dropout make the LTC3404 ideal for moderate current (up to 600mA) battery-powered applications.

For maximum efficiency over the widest range of output load current, Burst Mode operation can be selected by driving SYNC/MODE pin HIGH with a logic-level signal or by tying it to V_{IN}. For lower noise, pulse skipping mode can be selected by driving the SYNC/MODE pin LOW with a logic level signal or by tying it to ground. In this case, constant-frequency operation is maintained at lower load currents together with lower output ripple. If the load current is low enough, cycle skipping will eventually occur to maintain regulation. In this mode, the efficiency will be lower at very light loads, but becomes comparable to Burst Mode operation when the output load exceeds 50mA. For switching-frequency-sensitive applications, the LTC3404 can be externally synchronized to frequencies from 1MHz to 1.7MHz by applying an external clock signal to the SYNC/MODE pin. During synchronization, Burst Mode operation is inhibited and pulse skipping mode is selected.

3.1V/600mA Step-Down Regulator

Figure 1 shows a typical application suitable for a single Li-Ion cell or 3- to 4-cell NiCd or NiMH battery input. Note the small component values used in this application, made possible by the high switching frequency of the LTC3404. Also, because of the part's internal synchronous switch, the Schottky diode normally seen on the SW pin is absent from Figure 1. This regulator occupies only 0.47" x 0.31" (0.146in^2) of board area.

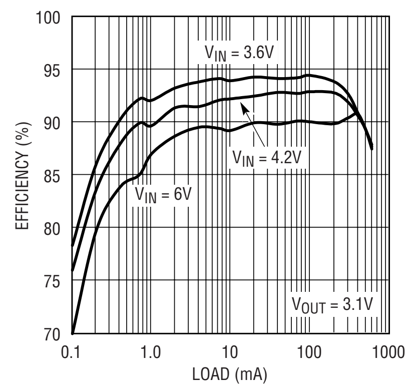


Figure 2. Efficiency vs load current for Figure 1's circuit (Burst Mode operation enabled)

Figure 2 shows the efficiency for three different input voltages. The efficiency for a 3.6V input exceeds 90% over three decades of output current. The efficiency remains high down to loads as small as 100µA due to the LTC3404's ultralow quiescent current. Even though the quiescent current is very low, the transient performance is not compromised. Innovative new circuitry ensures that

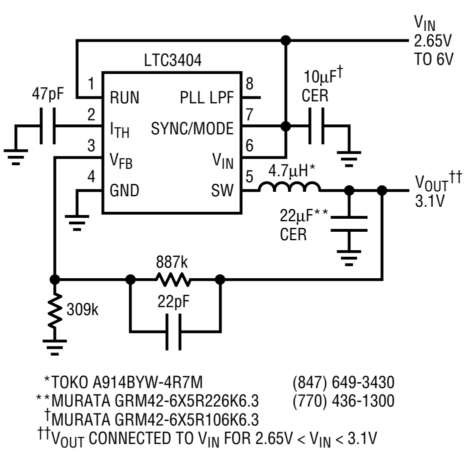


Figure 1. 3.1V/600mA step-down regulator

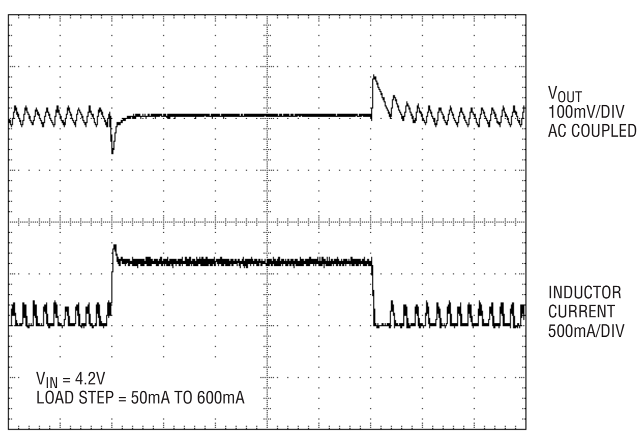


Figure 3. Load-step response for Figure 1's circuit

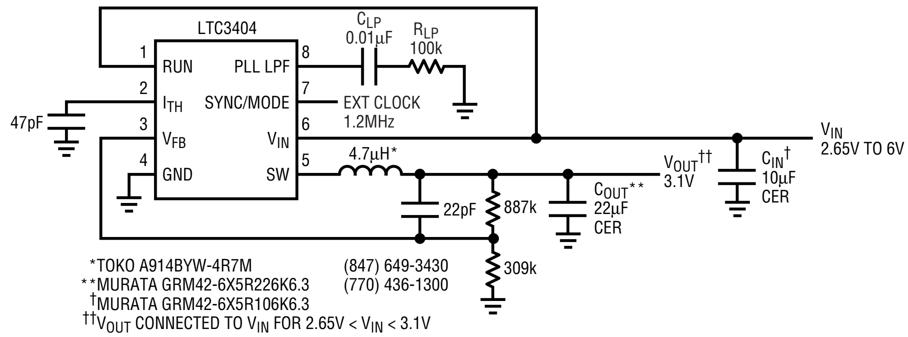


Figure 4. Externally synchronized 3.1V/600mA step-down regulator

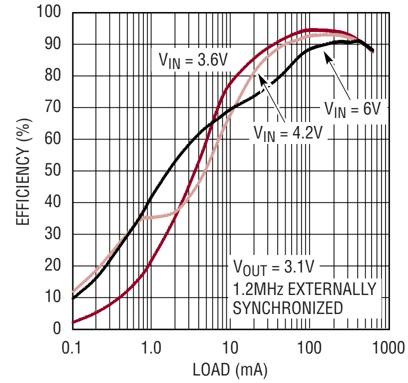


Figure 5. Efficiency vs load current for Figure 4's circuit (Burst Mode operation disabled)

the error amplifier, while operating on less than 10µA at no load, can quickly respond to load changes. The oscilloscope photo in Figure 3 shows the part's outstanding transient performance when subjected to a 600mA load step.

Externally Synchronized 3.1V/600mA Step-Down Regulator

Figure 4 shows an application for low switching frequency noise. The LTC3404 is synchronized to an external clock signal whereby Burst Mode operation is disabled automatically. This provides constant-frequency operation at lower load currents, reducing the ripple voltage. In this mode the efficiency is lower at light loads, as shown in Figure 5. However, the efficiency becomes comparable to that of Burst Mode operation when the output load exceeds 50mA.

The LTC3404 uses an internal phase-locked loop circuit to synchronize to an external signal. A voltage-controlled oscillator and a phase detector comprise the phase-locked loop. Filter components C_{LP} and R_{LP} smooth out the current pulses from the phase detector to provide a stable input to the voltage controlled oscillator. These components determine how fast the loop acquires lock. With the components shown in Figure 4, the loop acquires lock in about 100µs. When not synchronized to an external clock, the internal connection to the VCO is disconnected to prevent noise from altering the internal oscillator frequency. The oscilloscope photo in Figure 6 shows the transient performance with a 600mA load step.

Conclusion

The LTC3404 demonstrates that high switching frequency and low quiescent current can coexist, and thereby opens up a world of new possibilities in the design of battery-powered products.

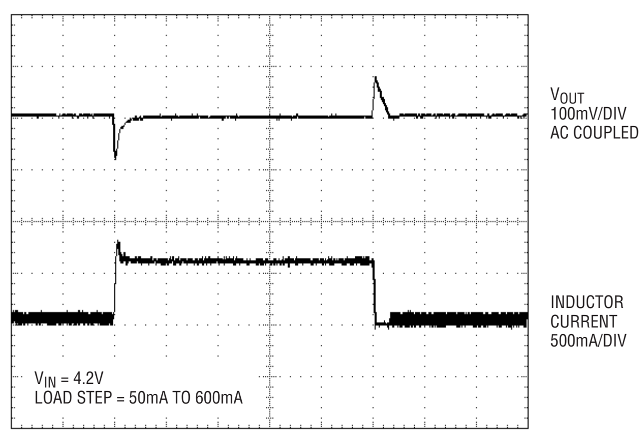


Figure 6. Load-step response for Figure 6's circuit

Authors can be contacted at (408) 432-1900

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Infinite Sample-and-Hold Outperforms Many Legacy Sample-and-Hold Amplifiers

by Derek Redmayne

Many applications requiring sample-and-hold amplifiers have been left high and dry by the dearth of these devices in today's catalogs. The use of an ADC followed by a DAC can provide this function, as well as producing characteristics not possible with a conventional sample-and-hold. The circuit shown in Figure 1 is a simple and compact implementation of a topology referred to as an "infinite sample-and-hold." It does not, in fact, hold for an infinite length of time but will do so until the power is turned off or until a new sample is required. The reason it is termed "infinite" is that it does not droop. It is formed from an ADC feeding a DAC. There is no droop because the sample is held as a digital code in the registers of the DAC.

The overall accuracy of the infinite sample-and-hold is determined by the error contributions of both the ADC and the DAC but is comparable to or better in most aspects than many of the older, and now obsolete, integrated sample-and-hold amplifiers. The disappearance of sample-and-hold amplifiers from the market is largely due to the fact that most ADCs now incorporate internal sampling circuits. Why not use these devices as the sampler? The alternative is building sample-and-hold amplifiers out of analog switches or diode bridges, and FET amplifiers. Most design engineers do not find this to be a very attractive alternative.

The infinite sample-and-hold in Figure 1 uses an LTC1417 serial 14-bit ADC interfaced to an LTC1658 serial 14-bit DAC. The short acquisition time of the ADC, coupled with external trigger circuitry, can produce a variety of useful functions, such as peak detection, a means for sampling dwell in a waveform such as the black reference level in video, phase measurement schemes, capacitance measurement or time division multiplexing, all without processor intervention. Such functions can, of course, be implemented by a microprocessor reading the output of an ADC, optionally modifying the result and sending it to one or more DACs. The advantage of a scheme that does not require a processor is, of course, low power and cost; in addition, the sample rate can be much higher than practical with a low powered processor. The uses of this type of function are almost endless, as are the possible variations.

Circuit Operation

The circuit in Figure 1 passes the serial output from the LTC1417 directly to the LTC1658, without requiring glue logic. If the reference voltages of the two parts are essentially the same, the function is very similar

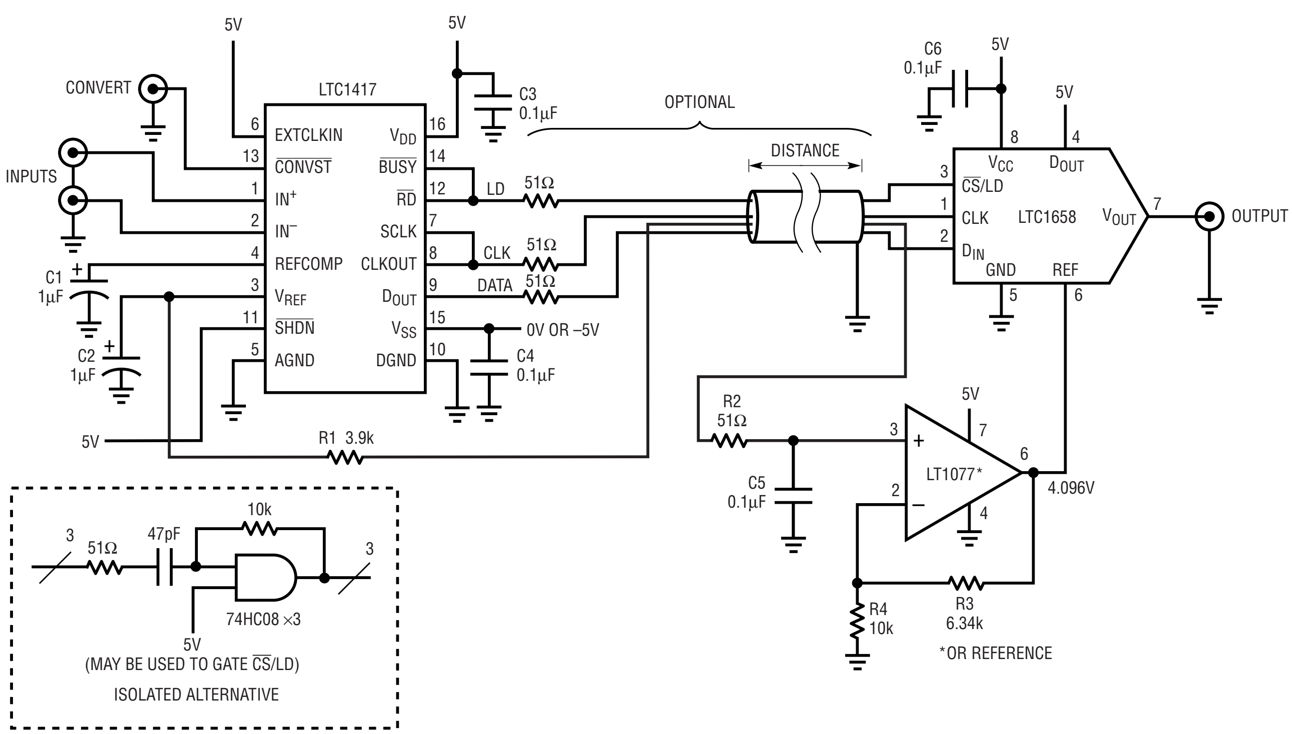

Figure 1. Infinite sample-and-hold schematic diagram

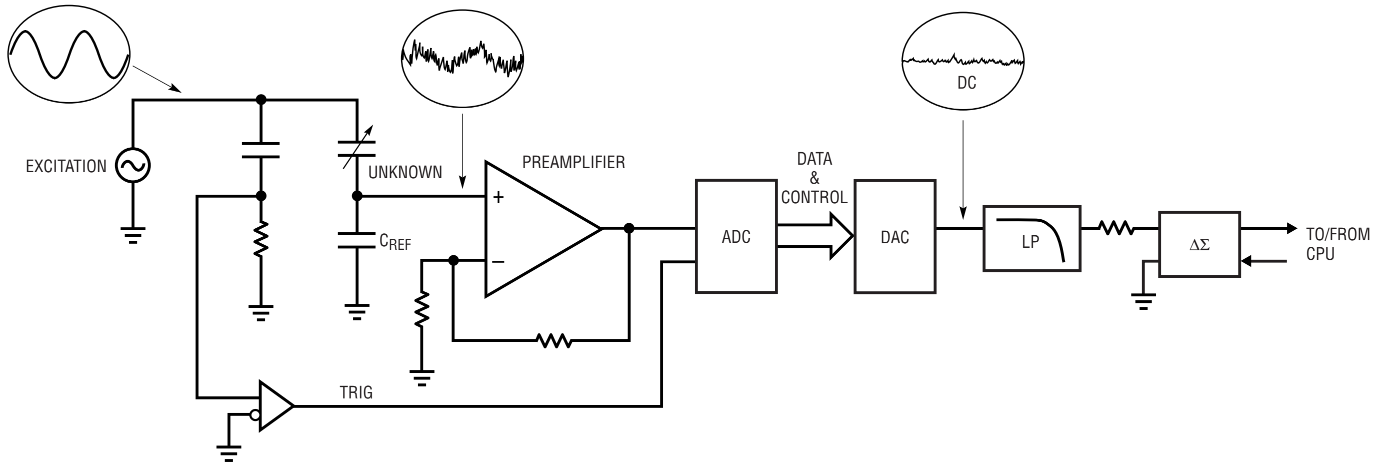

Figure 2. Block diagram of sample-rate conversion scheme

to an instrumentation amplifier followed by a sample-and-hold amplifier. In the case of the LTC1417, the internal 2.5V reference is stable but high impedance, but the REFCOMP terminal, which is labeled 4.096V and determines the full scale of the ADC, is only nominally at 4.096V. The LT1077 buffers the 2.5V output and provides a gain of 1.634 to produce the appropriate 4.096V reference for the LTC1658. If the output section is located at a distance or across a potential barrier, it needs a separate 4.096V reference at the LTC1658.

The LTC1417 is used in "internal conversion clock mode," where conversion and data transfer occur simultaneously. There is a one-conversion delay between the data sampled and the data output. If the waveform is sampled infrequently and an update is required as soon as possible, a first conversion must be performed at the time of the required sample, followed by a dummy conversion to transfer the data. The CS/$\overline{LD}$ line to the DAC can be gated to allow only the desired conversion to be passed to the DAC. Alternately, the fastest update will occur with parallel devices.

The use of a field-programmable gate array (FPGA) between the ADC and DAC allows the digital data to be modified prior to sending it to the DAC. If parallel I/O converters are used, some simple and useful operations, such as conversion of signed to absolute valued data, are possible even in a simple programmable-array-like device (PAL). The resulting output is a full-wave-rectified version of the original AC signal.

Sample-Rate Converter

There are cases where the infinite sample-and-hold can be useful as a sample-rate conversion scheme (see Figure 2). The LTC1417 can synchronously sample some recurring feature in the input waveform, possibly at a fairly high conversion rate or, alternatively, perform undersampling. Undersampling involves sampling a frequency that is above (possibly far above) Nyquist ($f_S/2$). The resulting output frequency is then the difference between the sample frequency or one of its harmonics and the input frequency. This type of sampling usually requires the bandwidth of the signal being sampled to be less than Nyquist (1/2 f_S) or multiple signal components will fold into the same signal band and interfere with each other. The output of the DAC can then be bandpass filtered and resampled at a lower and potentially unrelated rate by a slower ADC associated with a low power processor. This circuit can be used in capacitive sensing schemes with repetition rates up to 400kHz, using a lowpass filter after the DAC to reduce the noise for subsequent resampling with a slower ADC. This effectively reduces the bandwidth of the system to 2× that of the lowpass filter. If the noise present at the original ADC is greater than several LSB, the filtering effects following the DAC and the use of a higher resolution ADC for resampling can reveal details below the quantization floor of the original ADC and DAC. The integral linearity is limited by the infinite sample-and-hold, but resolution can be greater. If a recurring waveform is noisy, the use of the infinite sample-and-hold at a high sample rate, followed by a lowpass filter and resampling at a lower rate can provide a $\sqrt{N}$ improvement (where N = the number of samples) in noise level relative to what would be achieved by sampling directly at the lower rate. This approach makes sense if the power or budget restrictions do not allow the use of a DSP. The total current consumption of this circuit is less than 5mA.

Other advantages of using this topology are in the area of aperture uncertainty. Where a low powered processor may have limitations on how fast and how consistently it can respond to interrupts, sampling a signal in response to an external timebase or trigger can eliminate the uncertainty associated with nondeterministic behavior in the processor. If a direct control voltage is also required from the sampled waveform, the DAC may be the best way to produce it, even if the digital output is subsequently used by the processor.

The acquisition time of the LTC1417 is typically 150ns, and aperture jitter is only 5ps. The pedestal error common with classic

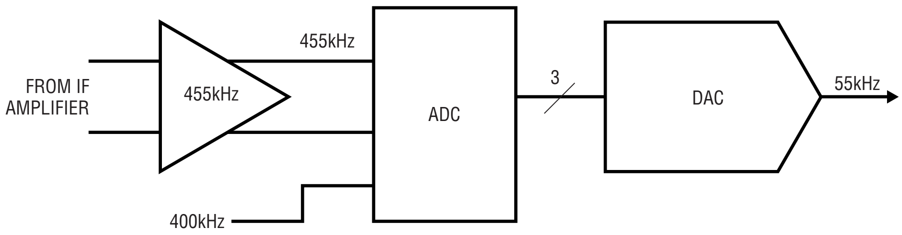

Figure 3. Down converter samples in Nyquist zone 3 (zone 3 extends from f_S to $f_S \times 1.5$).

sample-and-hold amplifiers and caused by charge injection is not an issue with this infinite sample-and-hold. There are, however, other error sources, such as offset voltage, quantization error and differential and integral nonlinearity contribution in both the ADC and the DAC. In this particular example, the DAC has more significant nonlinearity and offset error than the ADC. If higher linearity and offset performance are required, a 16-bit multiplying DAC, such as the LTC1595 could be used, because the 14-bit ADC (LTC1417) delivers 16-bit words.

As this serial scheme only requires three interface lines, the use of opto-isolators or some other isolation scheme is practical, allowing the output to be at different potential or distant from the input and, of course, with the variable gain offered by the multiplying feature of the DAC.

The inset in Figure 1 shows a very inexpensive scheme by which the output of the ADC can be level shifted hundreds of volts, provided that there is minimal high frequency noise between the ADC and the DAC. This would often be the case where a high voltage power supply has a common ground with lower voltage circuitry. This means of capacitively coupling digital data uses the high frequency content in the waveform only. It should not be used in situations where transients will be seen between the two subsystems. The voltage rating of the capacitors must be adequate and agency-accepted creepage distances should be observed.

Down Converter

If the conversion clock of the ADC is driven with a fixed frequency and the incoming signal is undersampled, the circuit in Figure 3 can down-convert frequencies up to the full linear bandwidth of the LTC1417. For example, if a band-limited 455kHz IF signal is being received at the input of the LTC1417 and a conversion clock of 400kHz is used, a 55kHz difference frequency appears at the output of the DAC. This output could be used in a variety of ways after active low-pass or bandpass filtering. For example, in conjunction with a frequency synthesizer, a mixer, and precision rectifier, a spectrum analyzer could be built using an LTC2420 20-bit micropower No Latency™ ΔΣ converter and a PIC. The subsequent filtering and resampling of this signal with a lower speed ADC permits a low power processor to characterize a high frequency signal and gain the benefit of a sample rate that far exceeds its processing capability. The use of an active filter after the DAC produces a narrow-band response that is not possible if the filtering is done at the IF frequency.

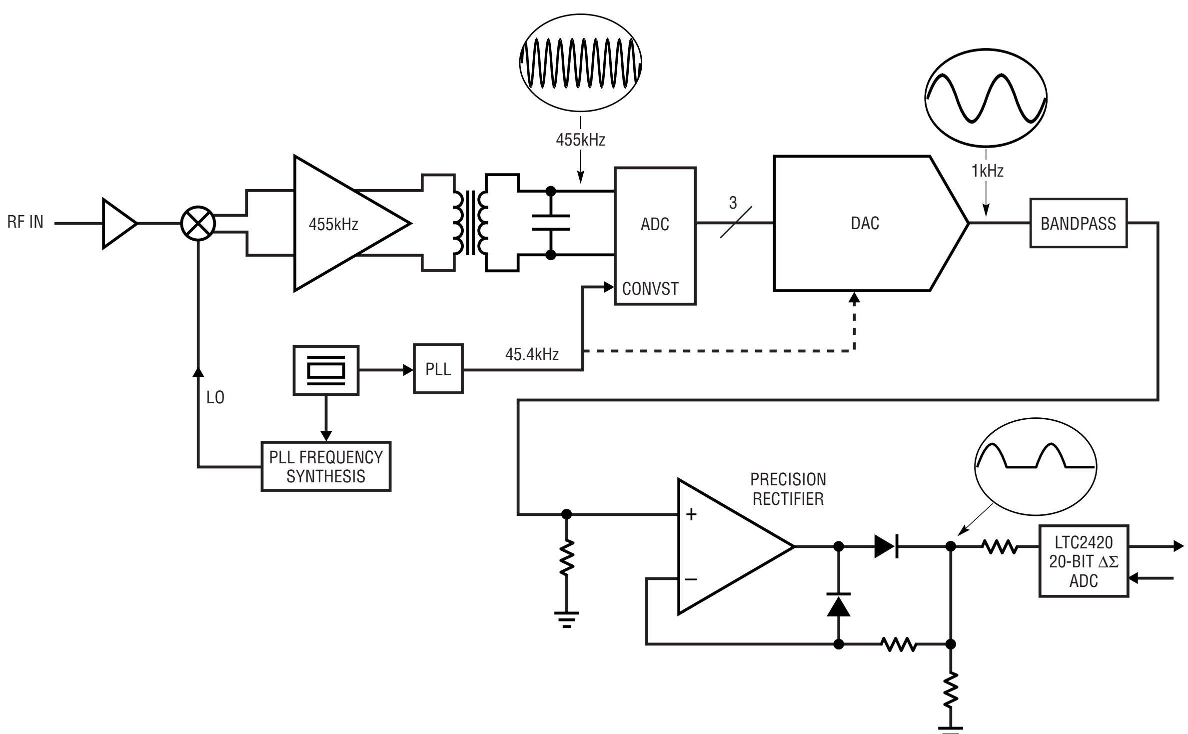

Figure 4. Block diagram of spectrum analyzer based on infinite sample-and-hold and LTC2420 20-bit ΔΣ ADC

In cases where the infinite sample-and-hold is used to undersample a higher frequency, the down conversion that is performed exaggerates the effects of phase jitter. This can be both a blessing and a curse. The blessed effect is that frequency stability and jitter effects are much easier to measure. The curse is that the use of a phase-locked loop as a tunable sample clock for spectrum analysis applications may simply expose the phase jitter of the phase-locked loop, rather than the incoming signal. Note also that undersampling a signal requires that the frequencies correspondingly below the sampling clock must be suppressed or they will fold into the baseband and become inseparable from the signal of interest.

An alternate down-conversion scheme in a single stage can use undersampling at a submultiple of an offset frequency (see Figure 4). If, for example, it is necessary to produce a 1kHz tone directly from a 455kHz IF signal, sampling at 454kHz is beyond the capability of the both the LTC1417 and the LTC1658. At the above mentioned 55kHz output rate, the output does not actually settle, but because each step is well within the slew limits of the DAC, the results are reasonable. On the other hand, if the ADC were sampling at 454kHz/10 (45.4kHz), the difference frequency would be 1kHz but the DAC update rate would allow plenty of time for settling, and distortion would be lower than would result from running at or near the full rate of the ADC. If the DAC update rate is 45kHz, the lowpass filter following the DAC should suppress the 45kHz update rate by 50dB or more.

Conclusion

The use of the infinite sample-and-hold as a sample-and-hold is straightforward and provides hold times not possible with a capacitor-based sample-and-hold amplifier. The characteristics can be tailored to suit many different applications by addition of circuitry before or after the ADC/DAC combination. Other Linear Technology ADCs and DACs can be used and multiple outputs derived from a single waveform can be provided by many DACs driven by a single ADC, as can multiple inputs be sampled via a multiplexer.

Authors can be contacted at (408) 432-1900

LTC2410/11/13, continued from page 25

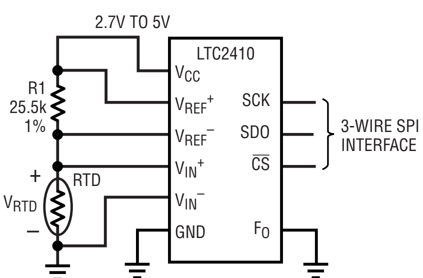

Figure 3.Half-bridge interface

overall errors typically summing to less than 3ppm of V_{REF}, this corresponds to six digits of accuracy.

The LTC2410's 2-terminal reference and 2-terminal input have common mode input ranges extending from GND to V_{CC}, independent of each other. As a result, ratiometric voltage measurements can be made directly with the LTC2410. As shown in Figure 2, the absolute accuracy of the LTC2410 enables reversal of input leads without shifts in the output code. For example, if V_{REF}^+ is tied to 5V, V_{REF}^- is tied to 0V, V_{IN}^+ is tied to 3V and V_{IN}^- is tied to 0V, the ADC will output a code corresponding to +3/5 of full-scale to within 3ppm. On the other hand, if V_{IN}^+ is tied to 0V and V_{IN}^- is tied to 3V (the input leads reversed), the ADC output will read –3/5 of full-scale to within 3ppm.

Half-Bridge Interface

Applications using RTDs and thermistors benefit from the large input common mode range of the LTC2410. As shown in Figure 3, this flexibility allows the reference resistor to directly drive the reference input and the RTD/thermistor to directly drive the input. Nonlinearity errors over the output voltage span of the RTD are eliminated using this configuration.

Simultaneous 50Hz and 60Hz Rejection

Many applications require simultaneous 50Hz and 60Hz rejection. While the LTC2410 offers pin-selectable 50Hz or 60Hz rejection, the LTC2413 simultaneously rejects both frequencies to 140dB common mode and 87dB normal mode. This is useful in applications where the destination country (line frequency) is unknown and a jumper or switch to select either 50Hz or 60Hz rejection is not practical.

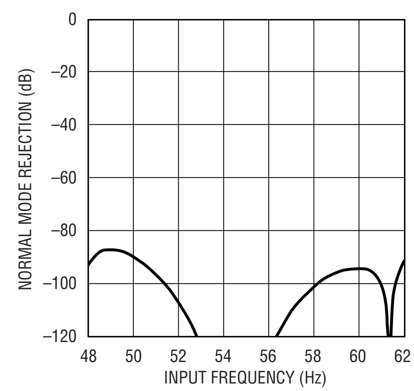

Figure 4. Simultaneous 50Hz/60Hz rejection

Conclusion

Linear Technology has introduced a new family of fully differential delta sigma analog-to-digital converters. The family consists of the LTC2410, a 800nV$_{RMS}$ noise device with 3ppm total unadjusted error, a pin/performance compatible simultaneous 50Hz/60Hz rejection device, the LTC2413, and the tiny (10-pin MSOP) LTC2411. These devices allow a direct connection to bridge sensors as well as a novel half-bridge interface. Their absolute DC accuracy rivals the performance of 6-digit DVMs.

New Device Cameos

LTC1773 Synchronous Buck Controller Extends Battery Life and Fits in Small Footprint

The LTC1773 is a current mode synchronous buck regulator controller that drives external complementary power MOSFETs using a constant frequency architecture. The operating supply range is from 2.65V to 8.5V, making it suitable for 1- or 2-cell Li-Ion battery-powered applications. The LTC1773's low quiescent current of 80µA, combined with its ability to operate at 100% duty cycle in dropout, maximizes the life of the battery. The LTC1773's operating frequency is internally set at 550kHz, allowing the use of small surface mount inductors and capacitors. Synchronous rectification increases efficiency and eliminates the need for a Schottky diode, further reducing components and board space. With its small MS10 package, the LTC1773 provides an efficient and compact total solution for portable power supplies.

Besides its high efficiency and small package, the LTC1773 also comes with many popular features. To protect the battery from excessive discharge, the LTC1773 has a precise 2.5V undervoltage lockout that monitors the input voltage. Peak inductor current limit is user programmable with an external high-side sense resistor. For noise-sensitive applications, the SYNC/FCB pin can be grounded to force continuous switching operation, or it can be synchronized to frequencies from 585kHz to 750kHz by connecting the SYNC/FCB pin to an external clock signal. To limit inrush current during start up, an external capacitor can be placed on the Run/SS pin for soft start. Also, to minimize output capacitance, OPTI-LOOP ™ compensation is available to the user through the I_{TH} pin.

For low voltage portable systems that require small footprint and high efficiency, the LTC1773 is the ideal solution.

LT1461 ±0.04%, 3ppm/°C Micropower, Low Dropout Reference Now Available in 3.0V, 3.3V, 4.096V and 5V Output Versions

Four new voltage options, 3.0V, 3.3V, 4.096V and 5V, complete the LT1461 family of voltage references, which was introduced with the 2.5V version. The LT1461 family of references features an extremely low temperature coefficient of 3ppm/°C, initial accuracy of ±0.04%, micropower operation (50µA max) with shutdown and low dropout operation (dropout voltage = 300mV max at I_{OUT} = 1mA). The LT1461 has been extensively characterized for both long term drift and thermal hysteresis and features specifications of 60ppm/$\sqrt{\text{kHr}}$ for the former and 40ppm for the latter.

The LT1461 features a wide operating voltage range (V_{OUT} + 0.3V to 20V) that allows it to be directly powered from a lithium battery or a low cost wall adapter. The LT1461 is available in the SO-8 package in three temperature grades: H (–40°C to 125°C), I (–40°C to 85°C) and C (0°C to 70°C).

LT1725 Controller Implements Isolated Flyback Topology without Optoisolators

The LT1725 implements isolated flyback switching power supplies without the traditional need for optoisolators and/or other additional circuitry to sense the output voltage. The LT1725 typically obtains its power from a third transformer winding. This allows operation from relatively high input voltage applications such as telecom (32V–72V) or offline potentials (85V–270V). The LT1725 includes the circuitry required to implement a trickle-charge start-up scheme.

The LT1725 uses a patented technique to sense the isolated output voltage via information in the primary-side flyback voltage waveform. No optoisolator control loop is required, thus simplifying the design and reducing cost. The limited dynamic response often associated with optoisolators is also eliminated. This technique achieves moderately accurate regulation without user trims and regulation is maintained well into discontinuous mode (light load). The target output voltage is set by an external resistor divider in conjunction with the transformer turns ratio. The resolution available in setting the resistor divider generally allows for a simple integer turns ratio such as 1:1, 1:2, 2:3 or the like. This eases the design of the transformer and allows more freedom in selecting winding inductance values.

The part drives an external N-channel MOSFET and uses an external resistor to sense current. Its gate-drive capability coupled with a suitable choice of MOSFET and other power path components typically allows load power up to tens of watts. It uses current mode switching control with all its well known advantages. The LT1725 features constant frequency operation in the range of 50kHz to 275kHz, with the operating frequency set by an external capacitor. Optional features include undervoltage lockout, soft start and load compensation.

The LT1725 is presently available in commercial grade, specified with a junction temperature of –40°C to 100°C. An industrial grade version, specified from –40°C to 125°C is planned for future release. The part is available in either the GN-16 or SO-16 package.

LT1784: 2.5MHz, Low Power Rail-to-Rail SOT-23 Op Amp Operates with Inputs above the Positive Supply

Featuring Over-The-Top™ inputs that operate above the positive supply, a small footprint and a rail-to-rail output, the 750µA LT1784 SOT-23 op amp delivers 2.5MHz gain-bandwidth product and a 2.5V/µs slew rate. Over-The-Top operation is important in many current sensing applications, where the inputs are required to operate at or above the supply.

Operating with supply voltages from 2.5V to 18V, the LT1784 also provides exceptional ruggedness. The op amp is internally protected for up to 18V of reverse supply and can withstand inputs up to 9V below the negative supply without phase reversal. The amplifier handles input voltages as high as 18V, both differential and common mode, independent of the supply voltage, making it ideal for applications with wide input range requirements and/or unusual input conditions.

The LT1784 is available in two pinouts, a standard SOT-23 5-lead version and a SOT-23 6-lead version with a shutdown feature that disables the part, making the output high impedance and reducing supply current to 5µA.

Low Distortion Dual Rail-to-Rail Amplifiers Drive ADCs and Cables

Operating from supplies as low as 2.5V, the 325MHz LT1807 and the 180MHz LT1810 dual rail-to-rail amplifiers provide the distortion and noise performance required by low voltage signal conditioning and data acquisition systems. Rail-to-rail inputs and outputs allow the entire supply range to be used and the high output current capability, 60mA typical on a 3V supply, is ideal for cable driver applications. The LT1807 is optimized for noise and DC performance, featuring a low voltage noise of $3.5nV/\sqrt{Hz}$ and a maximum offset voltage of 550µV. The LT1810 is optimized for slew rate and distortion, featuring a slew rate of 350V/µs and low harmonic distortion of HD_2 = –90dBc at f_C = 5MHz (V_S = 5V, V_O = $2V_{P-P}$). Both parts are fully specified for 3V, 5V and ±5V operation and are available in 8-lead SO and MSOP packages.

Authors can be contacted at (408) 432-1900

For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

DESIGN TOOLS

Technical Books

1990 Linear Databook, Vol I —This 1440 page collection of data sheets covers op amps, voltage regulators, references, comparators, filters, PWMs, data conversion and interface products (bipolar and CMOS), in both commercial and military grades. The catalog features well over 300 devices. $10.00

1992 Linear Databook, Vol II — This 1248 page supplement to the 1990 Linear Databook is a collection of all products introduced in 1991 and 1992. The catalog contains full data sheets for over 140 devices. The 1992 Linear Databook, Vol II is a companion to the 1990 Linear Databook, which should not be discarded. $10.00

1994 Linear Databook, Vol III —This 1826 page supplement to the 1990 and 1992 Linear Databooks is a collection of all products introduced since 1992. A total of 152 product data sheets are included with updated selection guides. The 1994 Linear Databook Vol III is a companion to the 1990 and 1992 Linear Databooks, which should not be discarded. $10.00

1995 Linear Databook, Vol IV —This 1152 page supplement to the 1990, 1992 and 1994 Linear Databooks is a collection of all products introduced since 1994. A total of 80 product data sheets are included with updated selection guides. The 1995 Linear Databook Vol IV is a companion to the 1990, 1992 and 1994 Linear Databooks, which should not be discarded. $10.00

1996 Linear Databook, Vol V —This 1152 page supplement to the 1990, 1992, 1994 and 1995 Linear Databooks is a collection of all products introduced since 1995. A total of 65 product data sheets are included with updated selection guides. The 1996 Linear Databook Vol V is a companion to the 1990, 1992, 1994 and 1995 Linear Databooks, which should not be discarded. $10.00

1997 Linear Databook, Vol VI —This 1360 page supplement to the 1990, 1992, 1994, 1995 and 1996 Linear Databooks is a collection of all products introduced since 1996. A total of 79 product data sheets are included with updated selection guides. The 1997 Linear Databook Vol VI is a companion to the 1990, 1992, 1994, 1995 and 1996 Linear Databooks, which should not be discarded. $10.00

1999 Linear Data Book, Vol VII — This 1968 page supplement to the 1990, 1992, 1994, 1995, 1996 and 1997 Linear Databooks is a collection of all product data sheets introduced since 1997. A total of 120 product data sheets are included, with updated selection guides. The 1999 Linear Databooks is a companion to the previous Linear Databooks, which should not be discarded.
$10.00

1990 Linear Applications Handbook, Volume I —
928 pages full of application ideas covered in depth by 40 Application Notes and 33 Design Notes. This catalog covers a broad range of "real world" linear circuitry. In addition to detailed, systems-oriented circuits, this handbook contains broad tutorial content together with liberal use of schematics and scope photography. A special feature in this edition includes a 22-page section on SPICE macromodels. $20.00

1993 Linear Applications Handbook, Volume II — Continues the stream of "real world" linear circuitry initiated by the 1990 Handbook. Similar in scope to the 1990 edition, the new book covers Application Notes 40 through 54 and Design Notes 33 through 69. References and articles from non-LTC publications that we have found useful are also included. $20.00

1997 Linear Applications Handbook, Volume III — This 976 page handbook maintains the practical outlook and tutorial nature of previous efforts, while broadening topic selection. This new book includes Application Notes 55 through 69 and Design Notes 70 through 144. Subjects include switching regulators, measurement and control circuits, filters, video designs, interface, data converters, power products, battery chargers and CCFL inverters. An extensive subject index references circuits in LTC data sheets, design notes, application notes and *Linear Technology* magazines. $20.00

1998 Data Converter Handbook — This impressive 1360 page handbook includes all of the data sheets, application notes and design notes for Linear Technology's family of high performance data converter products. Products include A/D converters (ADCs), D/A converters (DACs) and multiplexers—including the fastest monolithic 16-bit ADC, the 3Msps, 12-bit ADC with the best dynamic performance and the first dual 12-bit DAC in an SO-8 package. Also included are selection guides for references, op amps and filters and a glossary of data converter terms. $10.00

Interface Product Handbook — This 424 page handbook features LTC's complete line of line driver and receiver products for RS232, RS485, RS423, RS422, V.35 and AppleTalk® applications. Linear's particular expertise in this area involves low power consumption, high numbers of drivers and receivers in one package, mixed RS232 and RS485 devices, 10kV ESD protection of RS232 devices and surface mount packages.
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Data Conversion Solutions Brochure — This 64 page collection of data conversion circuits, products and selection guides serves as excellent reference for the data acquisition system designer. Over 60 products are showcased, solving problems in low power, small size and high performance data conversion applications—with performance graphs and specifications. Topics covered include ADCs, DACs, voltage references and analog multiplexers. A complete glossary defines data conversion specifications; a list of selected application and design notes is also included.
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FilterCAD™ 3.0 CD-ROM — This CD-ROM contains the latest release of FilterCAD, version 3.0. FilterCAD is a powerful filter design tool that supports all of Linear Technology's high performance active RC and switched capacitor filters. You can run FilterCAD directly from the CD or install it on your computer's hard disk for much faster operation. FilterCAD requires a PC running Windows® 95 or later.

The CD-ROM also contains a filter selection guide that lists all of Linear Technology's filter products, along with links to their data sheets. Adobe® Acrobat Reader, version 3.0 or later, is required to use the selection guide. Available at no charge.

Noise Disk — This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp. Available at no charge

SPICE Macromodel Disk — This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models and a demonstration copy of PSPICE™ by MicroSim. Available at no charge

SwitcherCAD™ — The SwitcherCAD program is a powerful PC software tool that aids in the design and optimization of switching regulators. The program can cut days off the design cycle by selecting topologies, calculating operating points and specifying component values and manufacturer's part numbers. 144 page manual included. $20.00

SwitcherCAD supports the following parts: LT1070 series: LT1070, LT1071, LT1072, LT1074 and LT1076. LT1082. LT1170 series: LT1170, LT1171, LT1172 and LT1176. It also supports: LT1268, LT1269 and LT1507. LT1270 series: LT1270 and LT1271. LT1371 series: LT1371, LT1372, LT1373, LT1375, LT1376 and LT1377.

Micropower SwitcherCAD™ — The MicropowerSCAD program is a powerful tool for designing DC/DC converters based on Linear Technology's micropower switching regulator ICs. Given basic design parameters, MicropowerSCAD selects a circuit topology and offers you a selection of appropriate Linear Technology switching regulator ICs. MicropowerSCAD also performs circuit simulations to select the other components which surround the DC/DC converter. In the case of a battery supply, MicropowerSCAD can perform a battery life simulation. 44 page manual included. $20.00

MicropowerSCAD supports the following LTC micropower DC/DC converters: LT1073, LT1107, LT1108, LT1109, LT1109A, LT1110, LT1111, LT1173, LTC1174, LT1300, LT1301 and LT1303.

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CD-ROM Catalog

LinearView — LinearView™ CD-ROM version 4.0 is Linear Technology's latest interactive CD-ROM. It allows you to instantly access thousands of pages of product and applications information, covering Linear Technology's complete line of high performance analog products, with easy-to-use search tools.

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World Headquarters

Linear Technology Corporation
1630 McCarthy Boulevard
Milpitas, CA 95035-7417
Phone: (408) 432-1900
FAX: (408) 434-0507

U.S. Area Sales Offices

NORTHEAST REGION
Linear Technology Corporation
3220 Tillman Drive, Suite 120
Bensalem, PA 19020
Phone: (215) 638-9667
FAX: (215) 638-9764

15 Research Place
North Chelmsford, MA 01863
Phone: (978) 656-4750
FAX: (978) 656-4760

NORTHWEST REGION
Linear Technology Corporation
720 Sycamore Drive
Milpitas, CA 95035
Phone: (408) 428-2050
FAX: (408) 432-6331

SOUTHEAST REGION
Linear Technology Corporation
17000 Dallas Parkway, Suite 219
Dallas, TX 75248
Phone: (972) 733-3071
FAX: (972) 380-5138

9430 Research Blvd.
Echelon IV Suite 400
Austin, TX 78759
Phone: (512) 343-3679
FAX: (512) 343-3680

1080 W. Sam Houston Pkwy., Suite 225
Houston, TX 77043
Phone: (713) 463-5001
FAX: (713) 463-5009

5510 Six Forks Road, Suite 102
Raleigh, NC 27609
Phone: (919) 870-5106
FAX: (919) 870-8831

CENTRAL REGION
Linear Technology Corporation
2010 E. Algonquin Road, Suite 209
Schaumburg, IL 60173
Phone: (847) 925-0860
FAX: (847) 925-0878

Kenosha, WI 53144
Phone: (414) 859-1900
FAX: (414) 859-1974

SOUTHWEST REGION
Linear Technology Corporation
21243 Ventura Blvd., Suite 208
Woodland Hills, CA 91364
Phone: (818) 703-0835
FAX: (818) 703-0517

15375 Barranca Parkway, Suite A-213
Irvine, CA 92618
Phone: (949) 453-4650
FAX: (949) 453-4765

International Sales Offices

FRANCE
Linear Technology S.A.R.L.
Immeuble "Le Quartz"
58 Chemin de la Justice
92290 Chatenay Malabry
France
Phone: 33-1-41079555
FAX: 33-1-46314613

GERMANY
Linear Technology GmbH
Oskar-Messter-Str. 24
D-85737 Ismaning
Germany
Phone: 49-89-962455-0
FAX: 49-89-963147

Haselburger Damm 4
D-59387 Ascheberg
Germany
Phone: 49-2593-9516-0
FAX: 49-2593-951679

Zettachring 12
D-70567 Stuttgart
Germany
Phone: 49-711-1329890
FAX: 49-711-7285055

HONG KONG
Linear Technology Corp. Ltd.
Unit 2109, Metroplaza Tower 2
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Phone: 852-2428-0303
FAX: 852-2348-0885

JAPAN
Linear Technology KK
5F NAO Bldg.
1-14 Shin-Ogawa-cho Shinjuku-ku
Tokyo, 162
Japan
Phone: 81-3-3267-7891
FAX: 81-3-3267-8510

6F Tokyo Seimei Honmachi Bldg.
1-6-13 Awaza, Nishi-ku
Osaka-shi, 550-0011, Japan
Phone: 81-6-6533-5880
FAX: 81-6-6533-5885

KOREA
Linear Technology Korea Co., Ltd
Yundang Building #1002
Samsung-Dong 144-23
Kangnam-Ku, Seoul 135-090
Korea
Phone: 82-2-792-1617
FAX: 82-2-792-1619

SINGAPORE
Linear Technology Pte. Ltd.
507 Yishun Industrial Park A
Singapore 768734
Phone: 65-753-2692
FAX: 65-752-0108

SWEDEN
Linear Technology AB
Sollentunavägen 63
S-191 40 Sollentuna
Sweden
Phone: 46-8-623-1600
FAX: 46-8-623-1650

TAIWAN
Linear Technology Corporation
Rm. 602, No. 46, Sec. 2
Chung Shan N. Rd.
Taipei, Taiwan, R.O.C.
Phone: 886-2-2521-7575
FAX: 886-2-2562-2285

UNITED KINGDOM
Linear Technology (UK) Ltd.
The Coliseum, Riverside Way
Camberley, Surrey GU15 3YL
United Kingdom
Phone: 44-1276-677676
FAX: 44-1276-64851

LINEAR TECHNOLOGY CORPORATION
1630 McCarthy Boulevard
Milpitas, CA 95035-7417
(408) 432-1900 FAX (408) 434-0507
www.linear-tech.com
For Literature Only: **1-800-4-LINEAR**