LINEAR TECHNOLOGY

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Ideal Diode Controller Eliminates Energy Wasting Diodes in Power OR-ing Applications

by David Laude

Introduction

Many modern electronic devices need a means to automatically and smoothly switch between power sources when prompted by the insertion or removal of any source. The LTC4412 permits low loss OR-ing of multiple power sources for extended battery life and low self-heating. The LTC4412 controls external P-channel MOSFET power switches to create a near ideal diode function for power switchover applications or load sharing PowerPath™ management applications. When conducting, the voltage drop across the MOSFET is typically only 20mV. It also provides power monitoring circuitry and external control for integration with other parts of the power management system. The low component count results in a low overall system cost and, with its ThinSOT™ 6-pin package, a compact design solution. It's versatile enough to be used in a variety of diode OR-ing applications.

For battery powered applications that also can be powered from a wall adapter or other "auxiliary" power source, the load is automatically disconnected from the battery when the auxiliary source is connected, so that no current is drawn from the battery. When the auxiliary source is disconnected, operation reverts back to the battery. An AC adapter present signal is available. The LTC4412 also has built in reverse supply protection. Multiple LTC4412s can be ganged together to provide load sharing between multiple batteries, or to allow multiple batteries to be charged from a single battery charger. The precisely controlled ideal diode behavior of the LTC4412 is crucial to maintain current balance when multiple batteries are discharged or charged while connected to a single load or source,

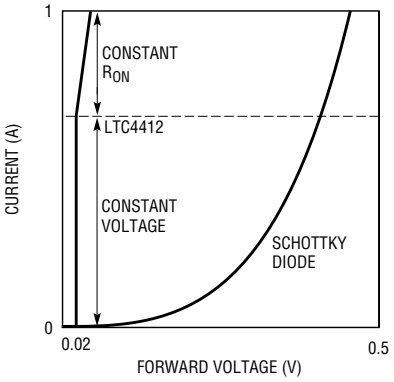

Figure 1. LTC4412 Ideal diode controller vs Schottky diode characteristics

The advantages of the LTC4412 ideal diode PowerPath controller are shown in Figure 1. The forward voltage drop of the ideal diode is far less than that of a conventional diode and the reverse current leakage can be

continued on page 3

Issue Highlights

This issue of *Linear Technology* magazine is rich in Design Features, showcasing innovative new devices that advance the state of the art of analog circuit development.

We begin with the LTC4412 ideal diode controller, which permits low loss OR-ing of multiple power sources for extended battery life and low self-heating. The LTC4412 controls external P-channel MOSFET power switches to create a near ideal diode function for power switchover or load sharing applications. When conducting, the voltage drop across the MOSFET is typically only 20mV. It also provides power monitoring circuitry and external control for integration with other parts of the power management system. The low component count results in a low overall system cost and, with its ThinSOT 6-pin package, a compact design solution. It's versatile enough to be used in a variety of diode OR-ing applications.

This magazine's first RF feature covers the LT5502 high performance limiting amplifier and quadrature IF demodulator. The LT5502 operates with a 70MHz to 400MHz input frequency over the widest supply voltage range in the industry—from 5.25V down to 1.8V. This allows the LT5502 to run directly from a single Lithium Ion battery or from two or more NiCd or NiMH batteries. In combination with an appropriate RF front end and RF/IF bandpass filters, the LT5502 forms a wideband receiver for applications at 900MHz, 1.8GHz, 2.4GHz–2.5GHz or other frequencies. The LT5502 can even be used as a free-standing receiver at frequencies below 400MHz.

This issue continues with the second part of the three-part series about Powered Ethernet. The article appearing here covers the operation of the PD in detail. Part 1 appeared in the August 2002 issue of the *Linear Technology* magazine and covered the power details of the system, with a focus on the PSE (Power Sourcing Equipment) and its characteristics.

The next two features cover two versatile new amplifiers.

The first is the LT1818 and LT1819 family of low distortion single and dual operational amplifiers. Each offers 400MHz gain bandwidth product and 2500V/µs slew rate. The parts operate with supplies from ±2V to ±6V and draw a typical supply current of only 9mA per amplifier.

The second covers the LTC6910-1, which is programmable for eight gain magnitudes of 0, 1, 2, 5, 10, 20, 50, or 100 Volts/Volt. This tiny DC-coupled, low-noise, self-contained amplifier, useful to low Megahertz frequencies, replaces expensive combinations of op amps and resistor arrays. The 8-lead TSOT-23 package needs no other analog components.

We end with three power product features. The first covers three new power supply supervisors that improve system reliability by offering more accurate reset thresholds than other supervisors on the market. They also save design time, production costs and board space with easy-to-use, flexible interfaces and a low external parts count.

The second introduces the LT1961 monolithic, current-mode, boost converter with a very high switching frequency and an onboard monolithic, high-current power switch. The power switch is included in the tiny MSOP 8-pin exposed leadframe package, dramatically shrinking layout and board space for most designs.

The final feature showcases the LT3710 controller, which brings simplicity, high efficiency and precision regulation to multiple output isolated power supply applications.

On page 33 is a short informational article about the LTC1744, a 14-bit ADC that has excellent dynamics and linearity at sampling rates up to 50Msps.

Starting on page 34 are three new Design Ideas covering a variety of applications, from a simple solution to low noise isolated power conversion, to a bootstrapped power supply that permits single rail amplifier output swing to ground (and below).

At the back are four New Device Cameos. See www.linear.com for complete device specifications and more applications information.

LTC in the News...

On October 15, Linear Technology Corporation announced its financial results for the 1st quarter of fiscal year 2003. According to Robert H. Swanson, Chairman of the Board and CEO, "Due to uncertainties surrounding worldwide economies, particularly in the United States, our sales and profits, while improving year over year, have been largely unchanged from the prior quarter. We continue to be strongly profitable, as demonstrated by our 38% return on sales, and also strongly cash flow positive from operations.

Looking forward, general economic conditions do not appear that they will improve significantly in the short-term. Nevertheless, we are well positioned, especially internationally, in some new programs at customers, which should ramp up during the December quarter. However, within the quarter, it is likely that December will be a slow month, particularly in the United States, as many customers will have plant shutdowns this calendar year-end around the holiday season. Therefore, confidently and accurately forecasting short-term future results is difficult. In summary, we estimate that sales and profits will be similar to or slightly up from the September quarter."

The Company reported net sales of $142,011,000 and net income of $53,802,000 for the quarter ended September 29, 2002. Diluted earnings were $0.17 per share.

LT1970, continued from page 1

smaller for the ideal diode as well. The tiny forward voltage drop lowers power losses and self-heating, resulting in extended battery life. The very low reverse leakage, when compared to Schottky diodes, is also beneficial in some applications.

The wide supply operating range of 2.5V to 28V supports operation with one to six Li-Ion batteries in series. The types of power sources that can be used include all those that are within the supply operating range. The low quiescent current of 11µA with a 3.6V supply is independent of the load current. The LTC4412 also features a status pin that can be used to enable an auxiliary MOSFET power switch for additional power savings when an auxiliary input is utilized. It may also be used to indicate to a microcontroller that an auxiliary supply, such as a wall adapter, is present. A control input pin is provided to extend applications to those that can benefit from external control, such as from a microcontroller.

Applications include anything that must take power from several inputs, including cellular phones, portable computers, PDAs, MP3 players and electronic video and still cameras, USB peripherals, wire-ORed multi-powered equipment, uninterruptible power supplies for alarm and emergency systems, systems with standby capabilities, systems that use load sharing between two or more batteries, multi-battery chargers, and logic controlled power switches.

How It Works

Figure 2 shows a circuit that automatically switches the power supply between a battery and a wall adapter (or other types of power inputs). The supply inputs are slowly ramped, as seen in Figure 3, to illustrate operation of the circuit. For the sake of this discussion the load is purely resistive, and the terms primary and auxiliary are arbitrary and interchangeable.

First the battery primary input, which powers the V_{IN} pin, is ramped up from 0V while the auxiliary input is absent. At about 0.6V the drain-source diode of the P-channel MOSFET transistor begins to forward bias and pulls the output up (time B1). Once the primary input reaches a voltage sufficient to drive the MOSFET gate and power the LTC4412, the forward regulation mode is achieved (B2). Now the output voltage is regulated to typically 20mV (10mV min) below the input. If the load current varies, the GATE pin voltage is controlled to maintain 20mV unless the load current exceeds the P-channel MOSFET's ability to deliver the current with a 20mV V_{DS}. If the R_{ON} is not low enough to maintain forward regulation then the gate voltage reaches ground or clamps 7V below the higher of the voltages on the V_{IN} or SENSE pins. Once clamped the MOSFET behaves as a constant low value resistor, and the forward voltage increases slightly. During this forward regulation mode of operation the STAT pin is an open circuit and the 470k resistor pulls the voltage up to the V_{CC} supply, which can be as high as 28V.

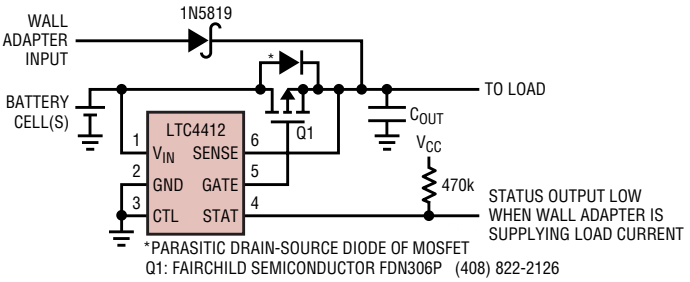

Figure 2. Automatic power switching between a battery and a wall adapter

"The forward voltage drop of the ideal diode is far less than that of a conventional diode..."

When a wall adapter or other supply connected to the auxiliary input is applied the SENSE pin voltage rises. The battery voltage also rises slightly from being unloaded. As the SENSE voltage pulls above V_{IN} – 20mV the LTC4412 pulls the GATE voltage up to turn off the P-channel MOSFET (A1). When the voltage on SENSE exceeds V_{IN} + 20mV the STAT pin sinks 10µA of current to indicate that an AC wall adapter is present. The system is now in the reverse turn off mode. Power to the load is being delivered through the external diode and no current is drawn from the battery. Should the primary input now be removed there is no effect (A2). When the primary input is applied and the

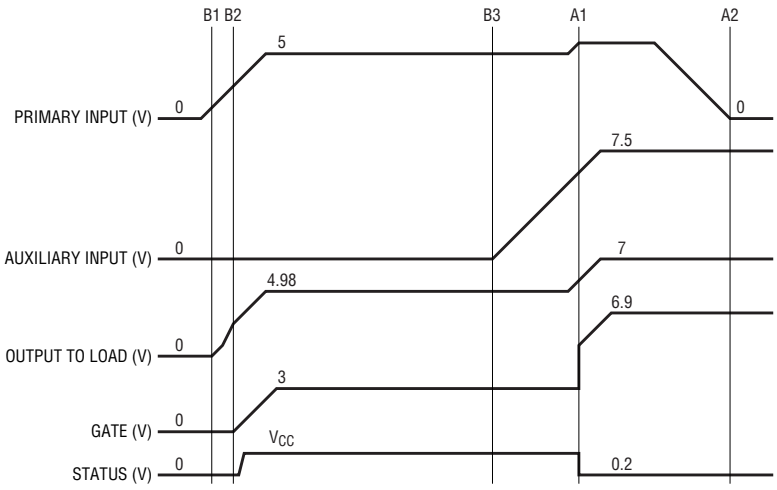

Figure 3. Operation waveforms

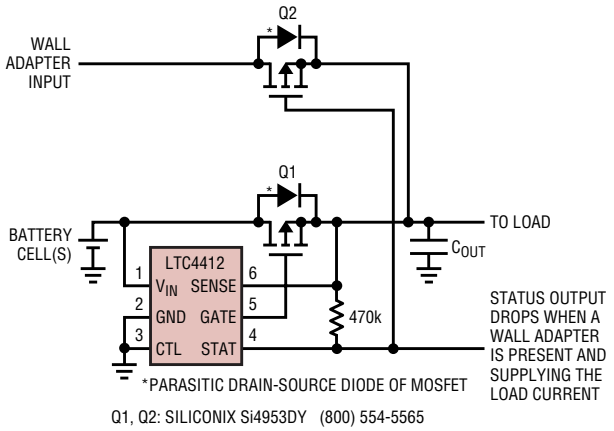

Figure 4. Lowest loss automatic power switching between a battery and a wall adapter

auxiliary input is removed the circuit reverts to battery operation (B3).

The external diode is used to protect against auxiliary input faults. A silicon diode could be used instead of the Schottky, but will result in higher power dissipation and heating due to the higher forward voltage drop. The wall adapter voltage must be high enough to overcome the diodes forward voltage drop. Note that the external MOSFET is wired so that the drain to source diode will reverse bias when a wall adapter input is applied. If the control input (CTL pin) is asserted high the GATE voltage is forced to the higher of the voltages on the V_{IN} pin or the SENSE pin turning the MOSFET off. Also the STAT pin will sink 10µA of current if connected. This feature is useful for forced switching of the load between two power sources. The drain to source diode inherent in MOSFETs require that series back to back MOSFETs, with gates tied together, be used to fully isolate a power source.

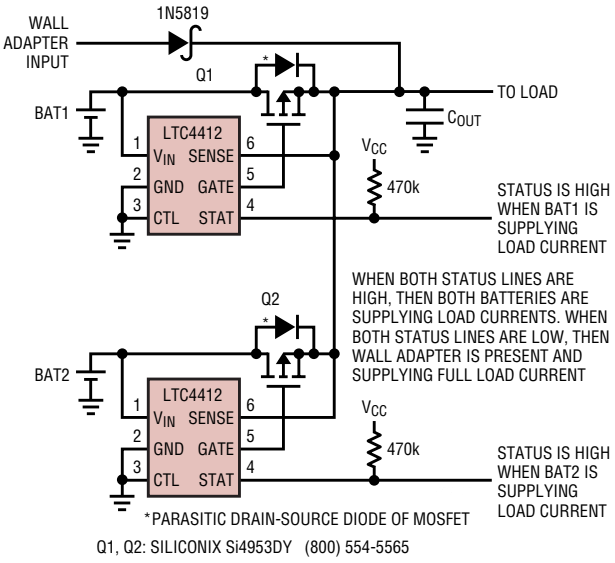

Figure 5. Dual battery load sharing with automatic switchover of power from batteries to wall adapter

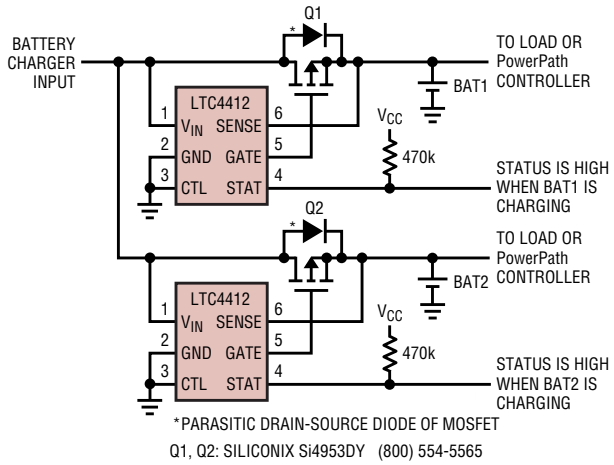

Figure 6. Automatic dual battery charging from single charging source

Lowest Loss Automatic PowerPath Control

Figure 4 illustrates an application circuit for automatic switchover of load between a battery and a wall adapter that features lower power loss in the auxiliary path than the circuit of Figure 2. Operation is similar to Figure 2 except that a P-channel MOSFET (Q2) replaces the diode. The STAT pin is used to turn on Q2 once the SENSE pin voltage exceeds the battery voltage by 20mV. When the wall adapter input is applied the drain-source diode of Q2 turns on first to pull up the SENSE pin and load voltages, followed by Q2's gate turning on. Once Q2 has turned on, the voltage drop across it can be very low depending on the MOSFET's characteristics.

Load Sharing

Figure 5 illustrates an application circuit for dual battery load sharing with automatic switchover of power between batteries and a wall adapter. Whichever battery can supply the higher voltage provides the load current until it is discharged to the voltage of the other battery. Then, the load is shared between the two batteries with the higher capacity battery providing proportionally higher current to the load. When a wall adapter input is applied both MOSFETs turn off and

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High Performance 400MHz Quadrature IF Demodulator Runs from 1.8V Supply

by Min Zou and Vladimir Dvorkin

Introduction

The LT5502 is a high performance limiting amplifier and quadrature IF demodulator that operates with 70MHz to 400MHz input frequency over the widest supply voltage range in the industry—from 5.25V down to 1.8V. This allows the LT5502 to run directly from a single Lithium Ion battery or from two or more NiCd or NiMH batteries. In combination with an appropriate RF front end and RF/IF bandpass filters, the LT5502 forms a wideband receiver for applications at 900MHz, 1.8GHz, 2.4GHz–2.5GHz or other frequencies. The LT5502 can even be used as a free-standing receiver at frequencies below 400MHz.

Circuit Description

The LT5502 consists of an IF limiting amplifier with 84dB small-signal gain, quadrature-converting mixers, lowpass filters and a receive signal strength indicator (RSSI) section. Figure 1 shows the LT5502 block diagram. In operation, an IF signal is limited by high gain amplifiers and is then demodulated into in-phase (I) and quadrature (Q) baseband signals using quadrature local oscillator (LO) carriers that are generated on-chip from an external 2 × LO signal. The demodulated I/Q baseband signals are passed through fully integrated 5th order lowpass filters and output drivers.

The LT5502 has a 4dB noise figure and an achievable sensitivity of –86dBm. Figure 2 shows the baseband I/Q output voltage swing versus IF input power at an IF frequency of 280MHz. The RSSI is built into the IF limiter, and offers a linear IF signal detection range of 90dB.

The quadrature demodulators are double-balanced mixers. The quadrature LO carriers are obtained from an on-chip divide-by-two circuit. For this reason, the external 2 × LO signal must be twice the LO frequency.

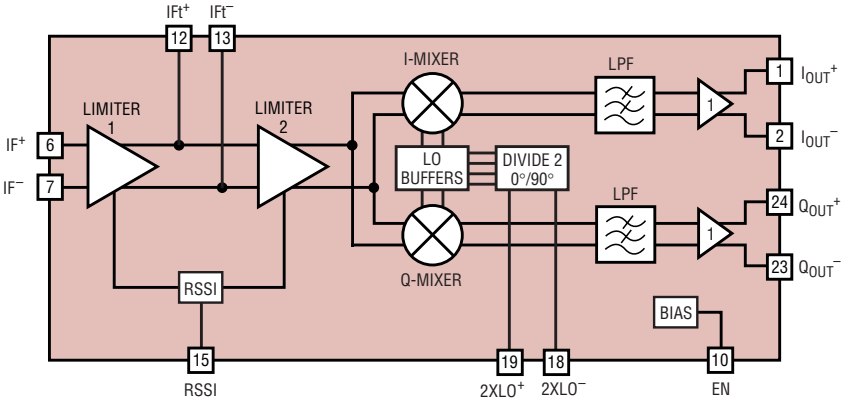


Figure 1. LT5502 block diagram

The lowpass filters on the I and Q channels serve for antialiasing and pulse shaping. The 3dB corner frequency is 7.7MHz and the group delay ripple is less than 17ns. The filter characteristics are stable over the –40°C to 85°C temperature range.

The LT5502 has two reduced-power modes of operation. In shutdown mode, supply current is reduced to less than 1µA. In standby mode with current consumption of 2.6mA, the baseband outputs are prebiased at their nominal quiescent voltages. This allows instant turn-on with no delay when the LT5502 is interfaced to a baseband chip using large coupling capacitors.

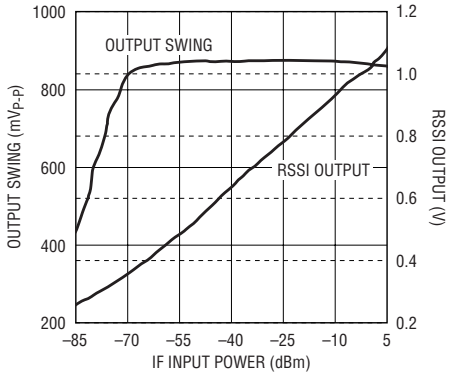


Figure 2. Baseband I/Q differential output voltage swing and RSSI output versus IF input power (IF Frequency = 280MHz, with a 1:4 IF input transformer, and without IF interstage filtering)

Applications and Implementation Issues

The LT5502 can be implemented on 2-layer, 4-layer or multilayer printed circuit boards, depending on the product circuit complexity and cost considerations. FR-4, GETEK and other PCB materials can be used. Product designers should provide a solid ground plane on the top layer of the PCB and multiple ground vias around the IC's ground pins. The ground plane on the top layer of the PCB should also be connected to the designated RF ground plane (located on the second layer) with multiple ground vias. All of the RF bypass capacitors should be placed adjacent to their designated IC pins. Bypass capacitors and IC ground pins should not share ground vias, to avoid ground loops. The IF input single-ended-to-differential conversion/matching circuit should be placed as close as possible to pins 6 and 7 of the LT5502. The LO input single-ended-to-differential conversion/matching circuit

Table 1: Typical receiver NF performance (high gain mode)

	1st BPF	RF switch	LNA	2nd BPF	Mixer	IF BPF	LT5502	Cascaded
Noise Figure, dB	2.5	1.0	4.0	2.5	14.0	10.0	4	9.77
Gain, dB	–2.5	–1.0	15	–2.5	6.0	–10.0	84.0	89.0

should be placed as close as possible to pins 18 and 19 of the LT5502.

Application Example

In the example of Figure 3, an input signal of 2.4GHz to 2.5GHz is converted to a popular 280MHz IF frequency. The Rx front end (refer to Figure 4) typically consists of an input bandpass filter to provide image frequency rejection and an LNA (low noise amplifier) to establish a low system noise figure to meet sensitivity requirements, followed by a down-converting mixer.

The main LO uses low-side injection. A 280MHz IF SAW bandpass filter provides protection from strong interfering signals in adjacent alternate channels and out of band. The LT5502's 5th order I/Q lowpass filters offer very good adjacent channel rejection at the baseband outputs, allowing product designers to relax requirements for the IF SAW filter performance and to use lower cost parts. The limiting IF amplifiers eliminate the need for an AGC function, and the dedicated RSSI output offers an unfiltered signal in real time with minimal delay. This simplifies requirements for the baseband and DSP portions of the product. External single-ended-to-differential converter circuits are employed at the IF and LO inputs. Direct termination of the IF input with a 50Ω resistor is possible, with small sensitivity degradation.

For time-division-duplex or half-duplex receive/transmit applications (IEEE 802.11 et al.), the receiver front-end shares the input bandpass filter (BPF) and antenna with the transmitter (again, see Figure 4). The LNA is followed by an optional BPF (depending on the application's image rejection requirements), a mixer and an IF filter. Typically, for IEEE 802.11 applications, the LNA has two gain settings: HIGH gain (15dB to 20dB) and LOW gain (0dB to –15dB) to satisfy input signal ranges from –80.0dBm to –4.0dBm.

The typical receiver NF performance is shown in Table 1. The cascaded NF of the receiver is 9.77. Considering the case where the noise BW is 7.7MHz and the signal-to-noise ratio (S/N) is 10dB, the receiver sensitivity at room temperature is given by:

kTB + NF + S/N =
–105.14dBm + 9.77dB + 10.00dB =
–85.37dBm

which satisfies the sensitivity requirements of the IEEE 802.11 standard with a conservative S/N of 10dB. Product designers must select the trip

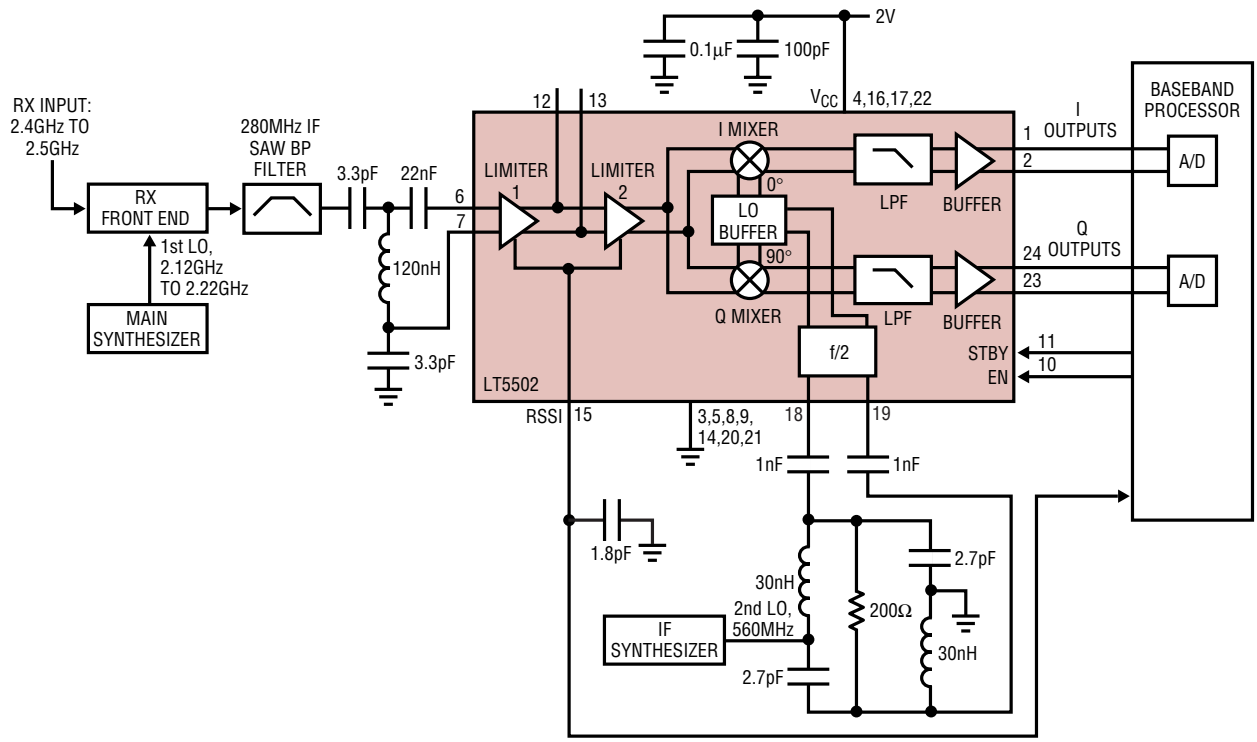


Figure 3. Example of 2.4GHz–2.5GHz receiver application (Rx IF = 280MHz)

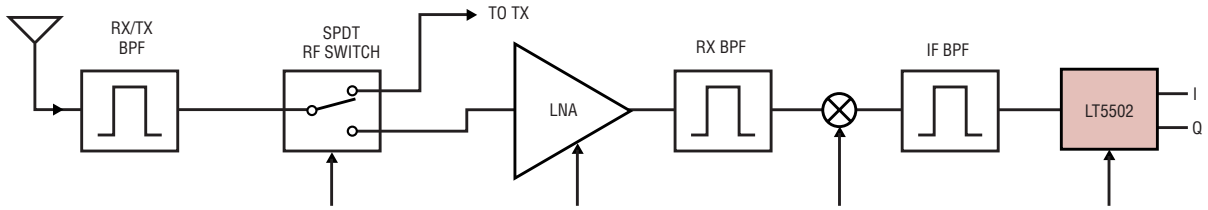


Figure 4. Example configuration of a 2.4 GHz–2.5GHz receiver

point for LNA HIGH/LOW gain switching depending on the actual application. The intermodulation performance of the overall receiver is determined by the front-end circuitry performance.

Interstage IF Filter

The LT5502 has provisions (pins 12 and 13) for an optional interstage IF filter (see Figure 5). This filter can be implemented with or without shunt resistor R1. The interstage filter can provide an additional sensitivity increase of 2dB to 3dB, depending on the Q-factor of the tank circuit. Use of the interstage filter may result in an increase of the group delay ripple at the baseband outputs.

IF Input External Circuitry

The external IF input circuitry to the LT5502 can be configured in several different ways, depending on cost, available board space and performance considerations.

The discrete single-ended-to-differential circuit in Figure 6a provides narrow band conversion and impedance matching. The cascaded NF is degraded by the input matching circuit loss, typically 0.75dB to 1.5dB. The component values shown in Figure 6a are for a 280MHz IF.

A 1:4 RF transformer with a 240Ω resistor in the secondary (Figure 6b) provides a broadband 50Ω impedance match at the primary. A Mini-Circuits JTX-4-10T 1:4 RF transformer or similar transformers from other manufacturers can be used. The cascaded NF is degraded by the transformer loss (1.0dB to 2.0dB). A 1:1 RF transformer can also be used with a 51Ω to 62Ω terminating resistor in the secondary of the transformer.

The circuit in Figure 6c offers a simple and economical solution for single-ended-to-differential conversion, although with a penalty of reduced sensitivity. A 62Ω resistor provides broadband 50Ω impedance matching. The cascaded NF for the IF circuit is degraded by 2.0dB.

LO Input External Circuitry

The LO input of the LT5502 can be configured in two different ways, depending on the cost, the available board space and performance considerations. Direct 50Ω resistive termination is not recommended because it would lead to an increase of LO leakage, which, in turn, may cause sensitivity degradation as well as deg-

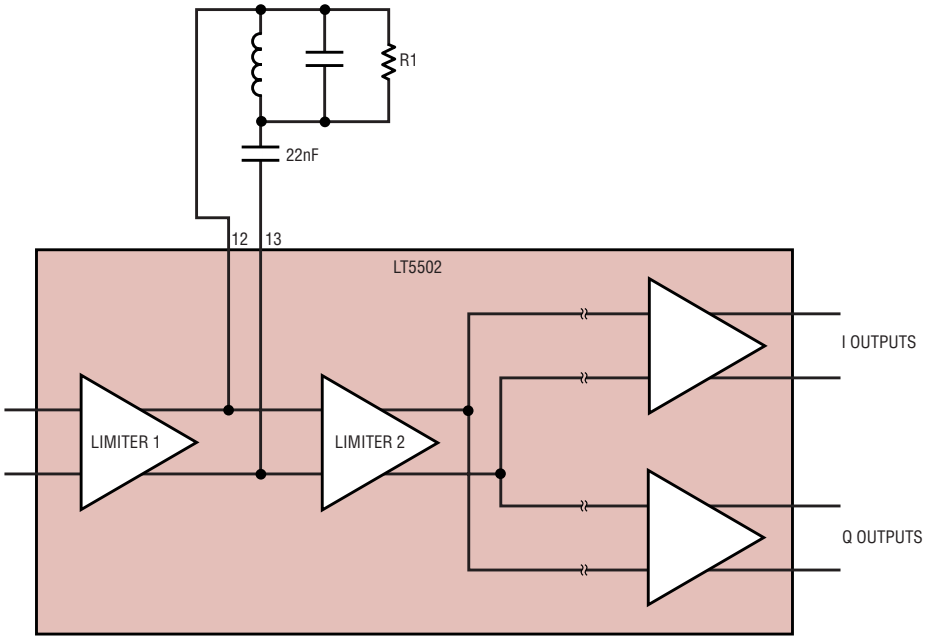


Figure 5. Example of an LT5502 interstage filter

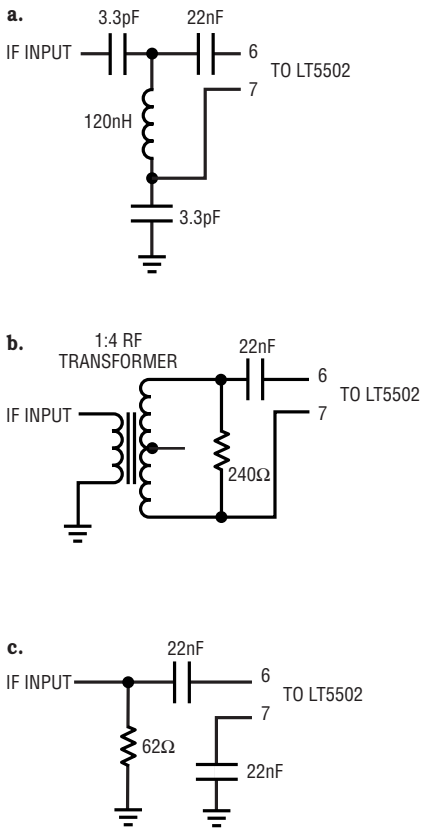


Figure 6. IF single-ended-to-differential input conversion and impedance matching

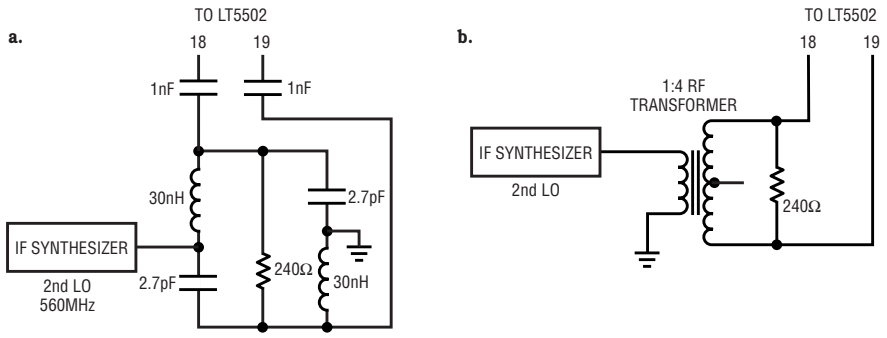


Figure 7. LO single-ended-to-differential input conversion and impedance matching

radation of the quadrature matching of the I/Q outputs.

The discrete single-ended-to-differential circuit in Figure 7a provides relatively broadband conversion and impedance matching. LO leakage to the IF input is minimal due to common mode rejection. Values shown are for a 560MHz LO frequency to support a 280MHz IF frequency.

A 1:4 RF transformer with a 240Ω resistor in the secondary (Figure 7b) provides a broadband 50Ω impedance match at the primary. LO leakage to the IF input is minimal, due to common mode rejection. A Mini-Circuits JTX-4-10T 1:4 RF transformer or similar transformers from other manufacturers can be used. A 1:1 RF transformer can also be used with a 51Ω to 62Ω terminating resistor in the secondary of the transformer.

Conclusion

The LT5502 is the first IF receiver in the industry to offer high performance with a supply voltage range spanning 1.8V to 5.25V. Its integrated on-chip, lowpass filters and intrinsically low noise operation allow it to meet radio system specifications with a wide variety of input termination options. The LT5502 is designed to simplify the job of the RF product engineer, offering a range of favorable tradeoffs depending on the cost and sensitivity requirements of the application.

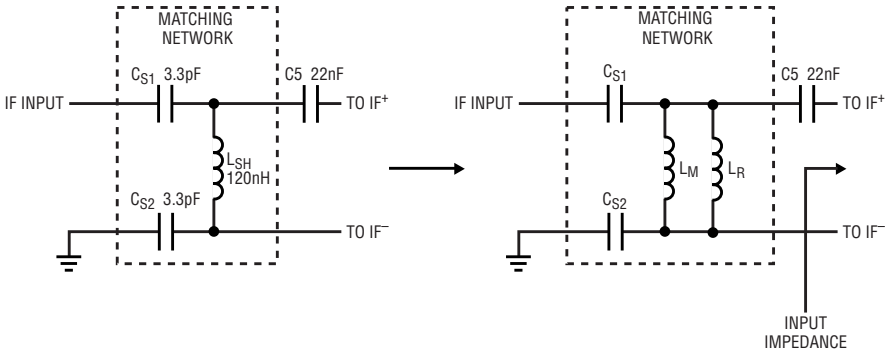


Figure 8. Input matching equivalent circuits

Addendum: Input Impedance Matching Procedures for Single-Ended-to-Differential Conversion

1. Turn input impedance into real resistance. The shunt inductor L_{SH} can be divided into two components: L_R and L_M (Figure 8). The L_R is used to resonate out the input capacitance, C_{IN}, of the LT5502, which is about 1.2pF. Its value can be determined by:

$$L_R = \frac{1}{(2\pi f_C)^2 C_{IN}} \bullet \frac{2.11 \bullet 10^{19}}{f_C{}^2} (nH)$$

2. Calculate L_M, C_{S1} and C_{S2}. After the input capacitive component is resonated out, the input impedance becomes real R_{IN}, which is about 2.2k. The L_M, C_{S1} and C_{S2} are used to convert R_{IN} into 50Ω. The following formulas can be used to calculate their values:

$$C_{S1} = C_{S2} = \frac{1}{\pi f_C \sqrt{50 \bullet R_{IN}}} \bullet \frac{9.6 \bullet 10^8}{f_C} (pF)$$

$$L_M = \frac{\sqrt{50 \bullet R_{IN}}}{2\pi f_C} = \frac{5.288 \bullet 10^{10}}{f_C} (nH)$$

3. Combine L_M and L_R into L_{SH} using the following equation:

$$L_{SH} = \frac{L_R \bullet L_M}{L_R + L_M}$$

New Power for Ethernet—Powered Devices (Part 2 of a 3-Part Series)

by Dave Dwelley

Introduction

An IEEE 802.3af Powered Ethernet connection provides both the familiar 10/100/1000MB/s data link and 13W worth of 48V DC power to a connected device. Such a device, known as a PD (for Powered Device), can be a digital Voice-Over-IP phone, a network wireless access point, a PDA charging station, an HVAC thermostat, or almost any small Ethernet-connected data device that would otherwise be powered by a wall transformer. A PD need not use the data link at all; something as simple as a cell phone battery charger or an illuminated exit sign could draw its power from an Ethernet connection.

This article is the second in a three-part series on Powered Ethernet. This issue covers the operation of the PD in detail. Part 1 appeared in the last issue of the *Linear Technology* magazine and covered the power details of the system, with a focus on the PSE (Power Sourcing Equipment) and its characteristics. Part 3 will discuss the nuances of detection and classification—the mechanism that the 802.3af standard uses to ensure that PDs receive power while legacy data-only devices remain unpowered.

Powered Ethernet Promises to Remove Warts

An excerpt from Part 1 of this series:

For years, data has passed over Ethernet CAT-5 networks, primarily to and from servers and workstations. The IEEE 802.3 group, the originator of the Ethernet standard, is currently at work on an extension to the standard, known as 802.3af, which will allow DC power to be delivered simultaneously over the same wires. This promises a whole new class of Ethernet devices, including IP telephones, wireless access points, and PDA charging stations, which do not require additional AC wiring or external power transformers ("wall warts").

Characteristics of a PD

Power arrives at the PD on a standard CAT-5 network cable via an RJ-45 connector. A CAT-5 wire contains four twisted pairs of 24-gauge wire (8 conductors in total). Two of the pairs—the "signal" pairs, at pin pairs (1, 2) and (3, 6) on the RJ-45 connector, shown in Figure 1—are used for the standard 10/100 Ethernet transmit and receive links. The two other pairs—the "spare" pairs, at pin pairs (4, 5) and (7, 8) are unused in 10/100 networks. 1000BASE-T networks use all four pairs. 48V appears on the cable as a difference in the common-mode voltages between the two signal pairs or the two spare pairs (but never both). The signal pairs are transformer-isolated as they enter the PD to strip the DC out of the data signal path; the power is taken from center taps on these transformers and passed to the PD input circuitry, as shown in Figure 2. The spare pairs may or may not be transformer isolated.

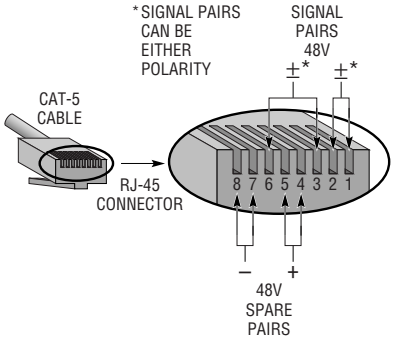


Figure 1. Signal and spare pairs on RJ-45 connector

To be considered an IEEE-802.3af PD, a device must meet several criteria. A PD must be able to accept power over either the signal pairs or the spare pairs, since a PSE is allowed to power either set. This is typically accomplished by diode ORing the two power inputs, as shown in Figure 3a. This circuit has the additional advantage of removing the signature from the unused set of pairs when the power is applied to the other set, a requirement of the IEEE spec. PDs are not allowed to draw power from both sets of pairs simultaneously. Diode bridges can be used to implement auto-polarity; this is useful since many CAT-5 cables are wired as crossover cables, so voltage polarity is likely to arrive reversed instead of forward. An alternate connection, shown in Figure 3b, uses single diodes and a third reverse biased diode to present an invalid signature when the polarity is reversed. This circuit will work with 802.3af systems, although it will not be powered if a crossover cable is used.

All PDs must present a characteristic 25kΩ signature impedance at the power inputs when probed with voltages between 2.8V and 10V. The signature impedance is allowed to

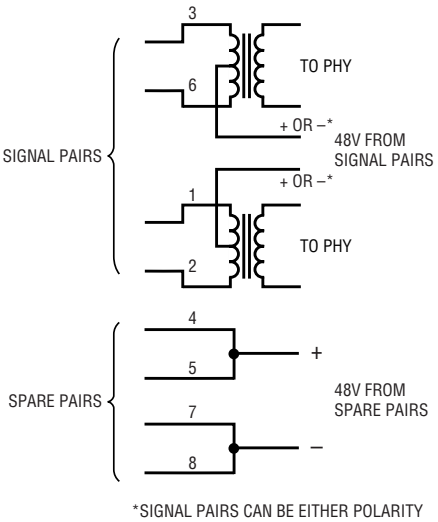


Figure 2. Deriving power from the cable

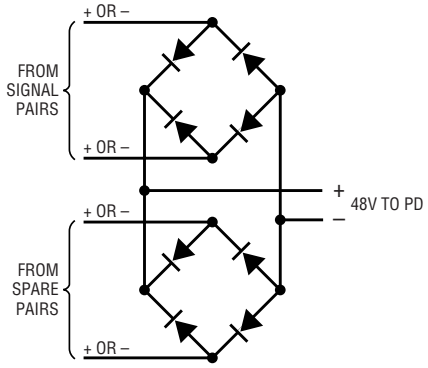


Figure 3a. Autopolarity input circuit

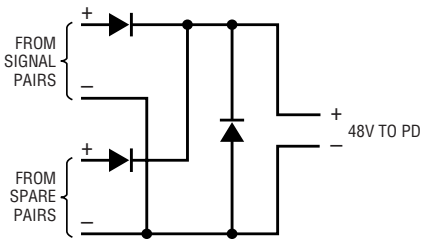


Figure 3b. Non-autopolarity input circuit

have up to three diodes in series, to allow for diode-based power steering and autopolarity circuits. This signature is an indication to the PSE, typically the Ethernet switch or hub, that the device on the end of the wire is, in fact, a PD, and won't be damaged if the PSE applies 48V to it. Older Ethernet devices, such as network interface cards and non-powered hubs, typically present common-mode impedances of around 150Ω, well away from the valid PD impedance.

A second, optional signature may be presented at the terminals when probed with between 15V and 20V. This "classification" signature indicates to the PSE the maximum power the PD will draw so the PSE can budget power if it chooses to. The classification signature appears as a constant current drawn by the PD at the input terminals. Table 1 shows the classes and their constant current signatures. Classes 1, 2 and 3 are used when the power is known. Class 0 is assigned if the PD chooses not to implement the classification signature. Class 0 means the PSE does not know how much power the PD may draw, although it's generally wise to budget Class 3 power for such a PD. Class 4 is reserved for future use.

Table 1. PD power classifications and signature currents

Class	PD Maximum Power	Nominal Classification Signature Current
0	0.44W–12.95W	< 5mA
1	0.44W–3.84W	10.5mA
2	3.84W–6.49W	18.5mA
3	6.49W–12.95W	28mA
4	Class 4 is currently reserved and should not be used	40mA

Once the PD has identified itself to the PSE, the PSE will apply a voltage between 44V and 57V to the wire. The PD now has several obligations. It should not draw significant load current until the terminal voltage rises above 30V (to avoid interfering with the classification signature), yet it must be fully operational by the time the line voltage reaches 42V. It can never draw more than 350mA or 12.95W continuously, whichever is less (brief surges to 400mA are allowed under some circumstances). It needs to operate with as much as 20Ω of wire in series with the input, which can cut the input voltage by as much as 8V during a 400mA current surge. This mandates adequate hysteresis between the turn-on and turn-off voltages to prevent *motorboating*—oscillating on and off—when the load is first applied and the input voltage is low. The PD must have an input capacitance below 180µF to keep the power-on current surge to a reasonable level; if this input capacitance is larger than 180µF, the PD must actively limit the inrush current to keep it under 350mA. Finally, the PD must maintain at least 10mA of current draw and must maintain an AC impedance of 33kΩ or less to avoid being disconnected.

LTC4257 PD Power Interface Controller

The LTC4257, shown in Figure 4, is designed to satisfy the specific demands that the IEEE standard places on a PD, allowing designers to focus on overall system design without worrying about compliance. The LTC4257 includes a trimmed 25k signature resistance on-board, and a full classification signature circuit, programmable to classes 0, 1, 2, 3 or 4 with a single external resistor. An on-chip power MOSFET keeps the PD circuitry disconnected from the line until the voltage rises above 40V. An inrush current limiting circuit keeps the line current below 400mA at all times, and thermal limiting protects the circuit from extreme fault conditions. The only task passed on to the rest of the PD circuitry is keeping the continuous power drain under 12.95W (or lower, if Class 1 or 2), something a switching regulator, such as the LT1871, does automatically. The regulator circuit must also maintain the required minimum 10mA current draw, a requirement usually met by the quiescent operating current of the system. *continued on page 27*

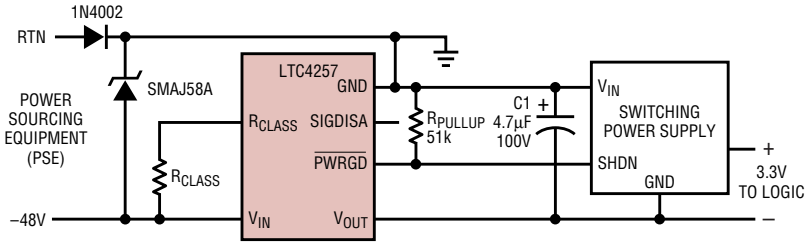


Figure 4. Typical PD application

2500V/µs Slew Rate Op Amps Process Large Signals with Low Distortion at High Frequencies

by Kris Lokere and Glen Brisebois

Introduction

The LT1818 and LT1819 are low distortion single and dual operational amplifiers that offer 400MHz gain bandwidth product and 2500V/µs slew rate. The parts operate with supplies from ±2V to ±6V and draw a typical supply current of only 9mA per amplifier.

The amplifiers can drive 100Ω loads with a low distortion of –85dBc relative to a 5MHz, $2V_{P-P}$ signal. In single 5V supply applications, the output swings to 0.8V from either supply rail with a 500Ω load (to 2.5V), and to 1.0V with a 100Ω load. The output current drive capability is typically 70mA. The low distortion and good output drive capability, combined with the 6nV/√Hz input voltage noise, make the LT1818/LT1819 an ideal choice for a wide variety of applications.

The LT1818 and LT1819 are available in space saving packages: the LT1818 single op amp in an SOT23-5; the LT1819 dual op amp in an 8-lead MSOP. Both parts are also available in an easy to use 8-lead SOIC. All parts are fully specified at ±5V and single 5V supplies, and are available in commercial and industrial temperature grades.

Table 1 summarizes the performance specifications of the LT1818 and LT1819.

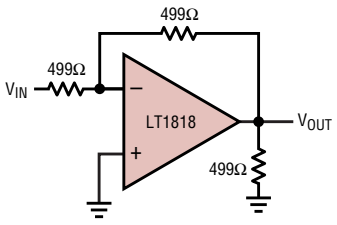


Figure 1. Test circuit for LT1818 (or competitor's part) configured in gain of –1.

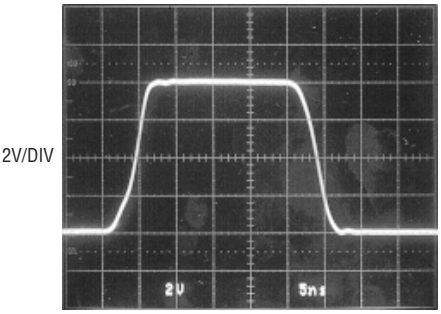


Figure 2a. The LT1818 responds to a 20MHz, ±4V input pulse with a fast enough slew rate to retain the shape of the pulse

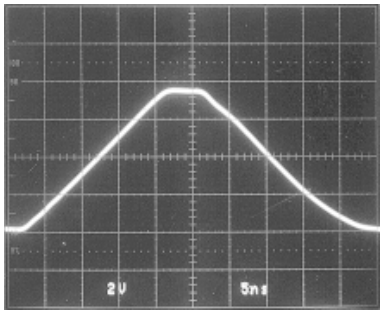


Figure 2b. Competitor's 625MHz op amp responds to the same input with inadequate slew rate to maintain pulse integrity

Fast Slew Rate Preserves High Bandwidth for Large Signals

The LT1818/LT1819 amplifiers exhibit an ultrafast slew rate of 2500V/µs in a gain of +1 and 1800V/µs in a gain of –1. The importance of a high slew rate is demonstrated by comparing the large signal dynamic response of amplifiers with similar bandwidths but differing slew rates. We compared the LT1818 to a competitor's amplifier, which has a wider, 625MHz bandwidth, but only a 400V/µs slew rate. Figure 1 shows a test circuit for a device configured in an inverting gain ($A_V = -1$). Figures 2a and 2b show the step response to a 20MHz, ±4V input pulse. The 3.5ns rise/fall time of the LT1818 (consistent with a 1800V/µs slew rate) preserves the 20MHz step very well. The lower slew rate amplifier, in contrast, is only barely fast enough to transmit the waveform,

Table 1: LT1818/LT1819 performance summary
(all specifications are typical with ±5V supplies and 25°C unless otherwise noted)

Parameter	Value
Gain Bandwidth Product	400MHz
Slew Rate	2500V/µs
Supply Current (per Amplifier)	9mA
Harmonic Distortion (5MHz, $2V_{P-P}$, R_L=100Ω)	–85dBc
Input Noise Voltage	6nV/√Hz
Input Noise Current	1.2pA/√Hz
Input Offset Voltage (Max)	1.5mV
Input Bias Current (Max)	±8µA
Input Common Mode Range	±4.2V
Output Voltage Swing (R_L=500Ω)	±4.1V
Settling Time (5V, ±0.1%)	9ns

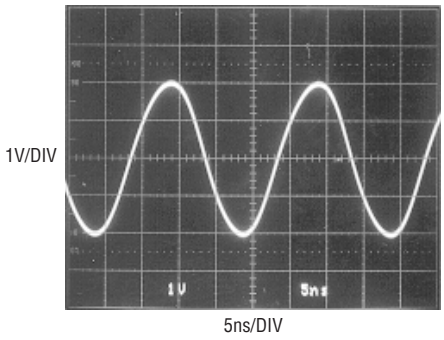


Figure 3a. LT1818 response to 50MHz, $4V_{P-P}$ sine wave maintains good fidelity.

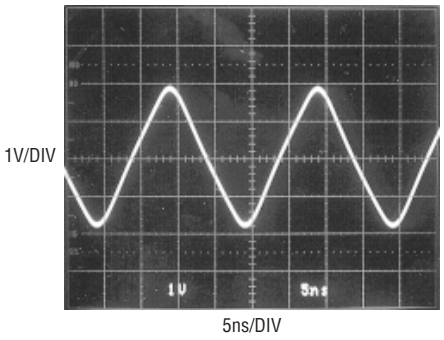


Figure 3b. Competitor's 625MHz response to the same sine wave is distorted.

turning it into a triangle wave. The difference in slew rate also has important ramifications for distortion of sine waves. Figures 3a and 3b show the response of both amplifiers to a 50MHz, $4V_{P-P}$ sine wave. The LT1818 transmits the waveform with minimal distortion, but the competitor's part turns the sine wave into a triangle wave, a result of the lower slew rate. This demonstrates that, to accurately process real world signals, slew rate is often the limiting parameter rather than bandwidth.

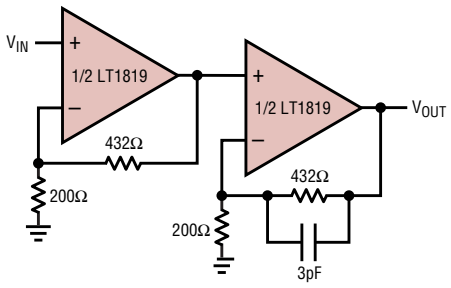


Figure 4. Dual op amp cascaded to form a gain of 10 (20dB).

The application shown in Figure 4 demonstrates the excellent high-frequency response of the LT1819 dual amplifier, and how two op amps can be combined to further increase bandwidth. The circuit shows the dual LT1819 op amp configured as two cascaded gain stages that together form a gain of 10 (= 20dB). The feedback capacitor on the second stage serves to cancel a pole formed by the feedback resistors and the input capacitance, to reduce peaking and ringing. The frequency-domain response (Figure 5) shows the –3dB frequency at 80MHz, which represents a gain-bandwidth product of 800MHz, consistent with two 400MHz amplifiers in series. Figure 6 shows the transient response to a small step. The 3.5ns rise/fall time is consistent with an 80MHz –3dB bandwidth. Figure 7 shows that the step response is only a little slower making a transition to a full $6V_{P-P}$, showing the merits of a high slew rate.

Low Distortion ADC Driver

Figure 8 illustrates the use of the LT1818 as a buffer for the LTC1744 14-Bit 50Msps ADC. The amplifier must provide low noise, low distortion as well as fast settling characteristics in order to recover quickly from the sampling loading effects of the ADC. The LTC1744 signal-to-noise ratio (SNR) of 73.5dB at $2V_{P-P}$ implies an input referred noise of $149\mu V_{RMS}$. The $6nV/\sqrt{Hz}$ input voltage noise of the LT1818, integrated over a 94MHz bandwidth (formed by the 51.1Ω, 18pF and the C_{IN} of the ADC) results in only $91\mu V_{RMS}$ of input noise. The contribution of the input referred current noise of the LT1818 depends on the source resistance of the circuit that drives the LT1818. For a 1k source resistance, the $1.2pA/\sqrt{Hz}$ input current noise results in $18\mu V_{RMS}$ over the same bandwidth. Both noise sources taken together still do not degrade the noise performance of the 14-bit ADC. Figure 9 shows the 4096 bin FFT of the converter output. This implies a full scale SNR of 76dB, just slightly better than the ADC's typical 73.5dB specification. More readily seen in the FFT is the SFDR of 78dB.

You can further improve the performance of the circuit by using the two amplifiers of the LT1819 to convert the single-ended input signal to a differential signal and drive both inputs of the LTC1744, as shown in Figure 10. An advantage of driving the ADC differentially is that the signal swing at each input can be reduced, which reduces the distortion of both the ADC and the amplifier. Typical performance is shown in the

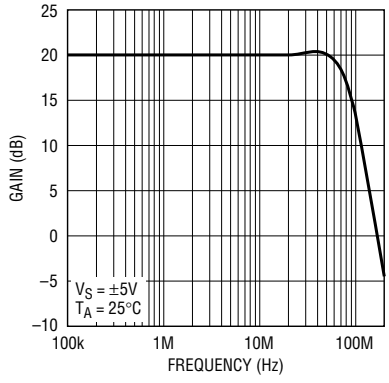


Figure 5. Frequency-domain response of 20dB gain block

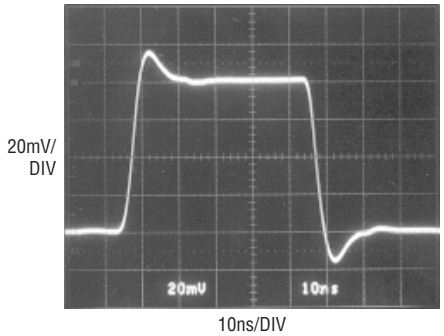


Figure 6. Small-signal transient response of 20dB gain block

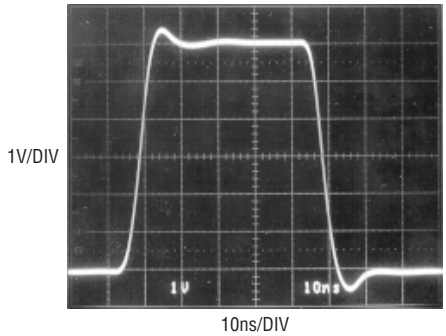


Figure 7. Large-signal transient response of 20dB gain block

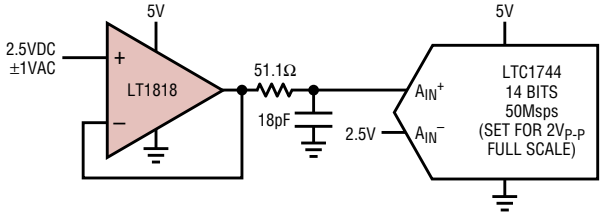


Figure 8. Single ended ADC driver

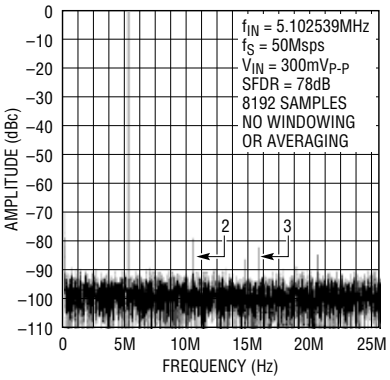


Figure 9. FFT of single ended ADC driver

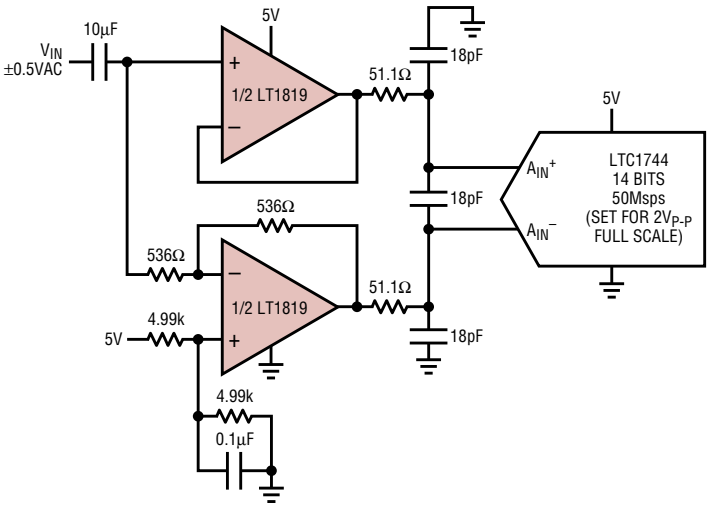


Figure 10. Single-to-differential ADC driver

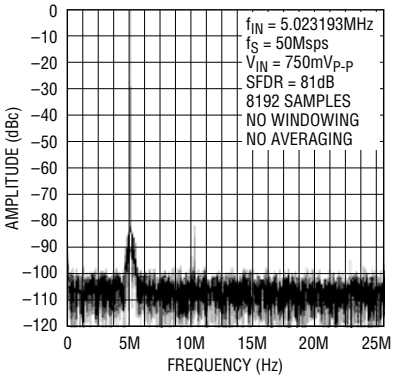


Figure 11. FFT of single-to-differential ADC driver

FFT of Figure 11, again consisting of 4096 bins derived from 8192 samples.

Fast Edge Generation to Measure Slew Rate

A 2500V/µs slew rate implies that the transition between ±2V occurs in 1.6ns. In order to accurately measure slew rates this fast, it is necessary to generate an input step that is faster than the device-under-test. Many off-the-shelf function generators fail in this regard, in which case custom-made circuitry may be necessary. The widely used HP8110A 100MHz Pulse Generator, for example, has a minimum rise/fall time of 1.8ns, which fails to provide a fast enough stimulus for this test. The older HP8082A Pulse Generator provides 1ns transitions, but its output amplitude is only 5V into 50Ω, which limits its flexibility to drive the amplifier on ±5V supplies.

The simple circuit of Figure 12 uses a high-speed inverter such as the NC7SZU04. Since the inverter has high gain, it sharpens the input edge of whatever pulse generator is used to drive it. The output is AC coupled to level shift the single supply inverter output to drive a split supply biased op amp. This inverter can provide rise and fall times as fast as 0.8ns, but the maximum supply voltage (and hence the maximum swing) is 5.5V, which is just short of the ±3V or ±4V desired for full range slew rate testing of the LT1818/LT1819. In addition, the 16mA output current drive of the inverter precludes a 50Ω termination, which limits the universal applicability of this circuit.

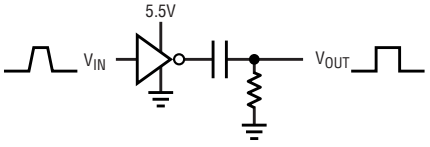


Figure 12. A simple inverter used to generate a sharp pulse—fast but too little signal swing and output drive

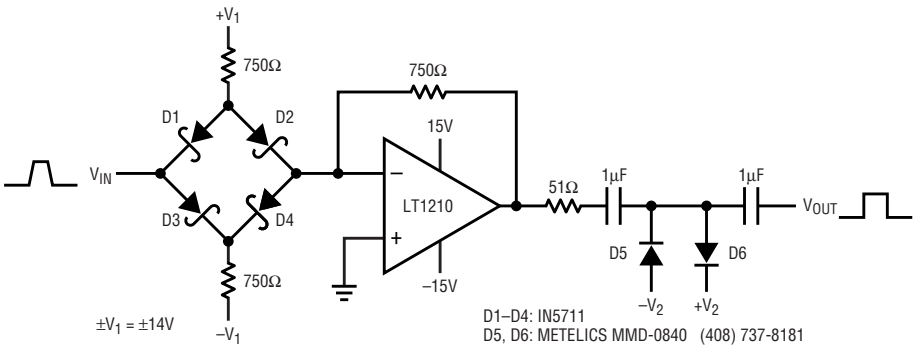


Figure 13. Improved pulse-sharpener circuit

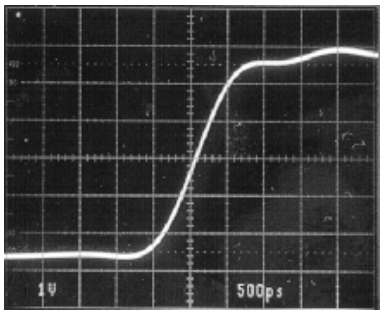


Figure 14. Output of pulse-sharpener circuit

Figure 13 shows a more involved, but very flexible and fast solution. The diode bridge D1-D4 switches the LT1210 current-feedback amplifier, which runs off ±15V supplies. This way, the input edge does not need to swing more than ±1V, and the current into the inverting node of the LT1210 switches very quickly. The already fast waveform at the output of the amplifier is then AC coupled into the D5–D6 Step Recovery Diodes (SRD).

An SRD is a two terminal p-i-n junction whose DC characteristics are similar to the usual p-n junction diode, but whose switching characteristics are quite different. The most distinguishing feature of the SRD is the very abrupt dependence of its junction impedance upon its internal charge storage. If a forward biased SRD is suddenly reverse-current biased, it will first appear as a very low impedance until the stored charge is depleted. Then the impedance will suddenly increase to its normal high reverse value, thereby stopping the flow of reverse current. This impedance transition generally takes only a few hundred picoseconds. The circuit in Figure 13 uses this SRD property as a pulse sharpener, generating a sub-one-nanosecond edge at the output. You can set the voltage levels of the output waveform by adjusting $\pm V_2$. Figure 14 shows a 5V, 0.8ns output waveform generated by this circuit.

Finally, an important consideration in these measurements is the bandwidth of the oscilloscope used. The photograph in Figure 14 is taken with a Tektronix TDS820 6GHz digitizing oscilloscope. For a detailed description of the effect of slower oscilloscopes on measuring fast edges, refer to Linear Technology Application Note 47.

LT1818 Circuit Design

A simplified schematic of the LT1818/LT1819 is shown in Figure 15. Both inputs are high impedance, classifying the amplifier as a voltage feedback topology. Complementary NPN and PNP emitter followers Q1-Q8 buffer each input and present the differential input signal across the internal resistor R1. The input common mode range extends to typically 0.8V from either supply, and is limited by a V_{BE} of Q10/Q14 plus a V_{SAT} of Q5/Q6. NPN and PNP current mirrors Q10–Q11 and Q14–Q15 mirror the current generated through R1 into the high impedance node. Cascode devices Q9 and Q13 raise the output impedance of the mirror, improving the open loop gain.

Resistor R1, the transconductances of Q5–Q8, and the compensation capacitor C1 set the 400MHz gain bandwidth product of the amplifier. The R_C, C_C network between the high impedance node and the output provides extra compensation when the output drives a capacitive load. This keeps the LT1818/LT1819 unity-gain stable with a C_{LOAD} up to 20pF. The amplifier can drive larger capacitive loads when configured in higher noise gains, or with an isolation resistor of 10Ω to 50 Ω in series with the load. The R_2, C_2 networks on the current mirrors provide a pole and zero at a frequency below the unity-gain frequency. This lowers the frequency where the open loop gain crosses 0dB, which improves the phase margin of the amplifier while maintaining a high open loop gain at lower frequencies.

The current generated across R1, divided by the capacitor C1, determines the slew rate. Note that this current, and hence the slew rate, are proportional to the magnitude of the input step. The input step equals the output step divided by the closed loop gain. The highest slew rates are there-

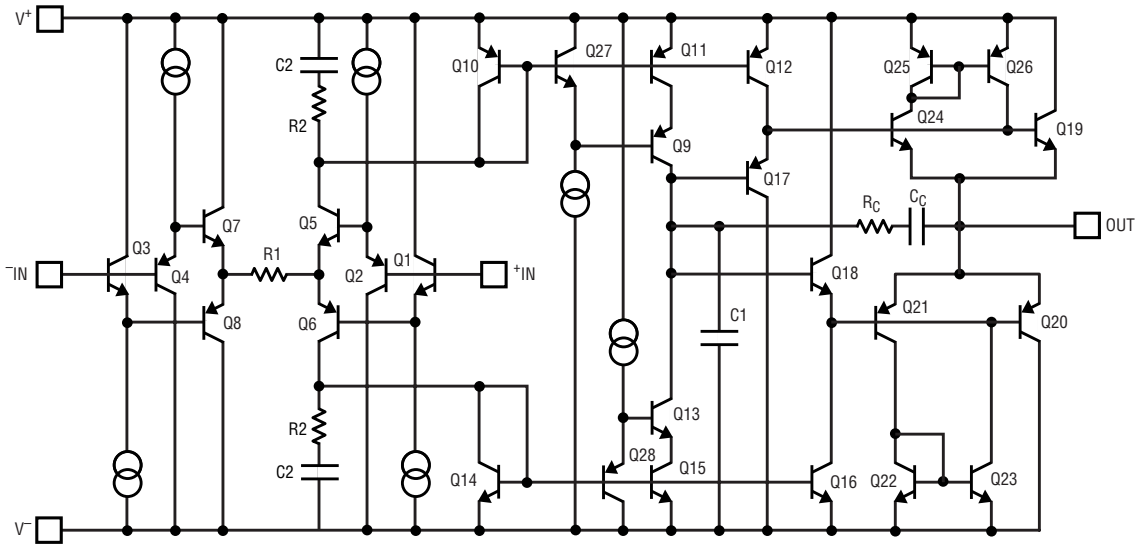


Figure 15. Simplified schematic of LT1818/LT1819 amplifier

fore obtained in the lowest gain configurations. The 2500V/µs slew rate specified on the data sheet is measured in a noninverting unity gain configuration. The 1800V/µs production tested slew rate is measured in an (inverting) gain of –1, which is equivalent to a noninverting gain of 2.

The internal current generated across the input resistor can be much higher than the quiescent supply current (up to 80mA). In normal transient closed loop operation this does not present a problem, since after a few nanoseconds the feedback brings the differential input signal back to zero. However, sustained (i.e. open loop) differential input voltages may result in excessive power dissipation and therefore this amplifier should not be used as a comparator.

The output stage buffers the high impedance node from the load by providing current gain. Emitter followers Q17–Q20 provide a current gain equal to $Beta_{NPN} \times Beta_{PNP}$, but the effective current gain is greatly enhanced by the dynamic base current compensation provided by Q24–Q26 and Q21–Q23. Q24 measures a fraction of the output current that flows through Q19, and mirror Q25–Q26 injects the appropriate current back into the base of Q19. This signal-dependent boost improves the linearity of the amplifier by reducing the amount of differential input signal required for a given output current. An additional advantage is that the output devices can be smaller, which requires less quiescent current for a given amplifier speed.

Conclusion

The ultrafast slew rate and high bandwidth allow the LT1818 and LT1819 op amps to process large signals at high frequencies with low distortion. Combined with the low noise and moderate supply current, these amplifiers are a good choice for receivers, filters, or drivers of cables and ADCs in high-speed communication or data acquisition systems.

LTC4412, continued from page 4

no load current is drawn from the batteries. The STAT pins provide information as to which input is supplying the load current. This concept can be applied to as many power inputs as are needed.

Multiple Battery Charging

Figure 6 shows an application circuit for automatically charging two batteries from a single charger. Whichever battery has the lower voltage receives the charging current until both battery voltages are equal then both will be charged. When both are charged simultaneously the higher capacity battery receives proportionally higher current from the charger. For Li-Ion batteries both batteries achieve the float voltage of the battery charger minus the forward regulation voltage of 20mV. This concept can apply to more than two batteries. The STAT pins provide information as to which batteries are being charged.

High Side Power Switch

Figure 7 illustrates an application circuit for a logic controlled high side power switch using the control input pin. When the CTL pin is a logical low the LTC4412 turns on the MOSFET. Because the SENSE pin is grounded the LTC4412's internal controller functions as an open-loop comparator and applies maximum gate drive voltage to the MOSFET. When the CTL pin is a logical high the LTC4412 turns off the MOSFET by pulling its gate voltage up to the supply input voltage, therefore denying power to the load. The MOSFET is connected with its source connected to the power source. This prevents the drain-source diode from supplying voltage to the load when the MOSFET is off.

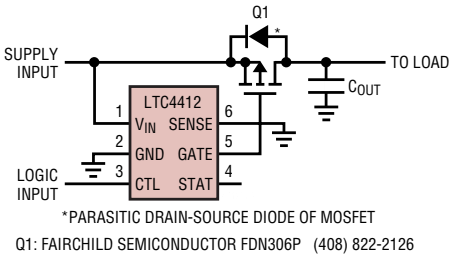


Figure 7. Logic controlled high side power switch

Conclusion

The LTC4412 provides a simple and efficient way to implement a low loss ideal diode controller that extends battery life and significantly reduces self-heating. The low external parts count translates directly to low overall system cost and its ThinSOT 6-pin package makes for compact design solutions. It's versatile enough to be used in a variety of diode OR-ing applications covering a wide range of supply voltages.

SOT-23 Digitally Controlled Amplifier Puts Programmable Gain Anywhere

by Max W. Hauser

Introduction

LTC6910-1 is programmable for eight gain magnitudes of 0, 1, 2, 5, 10, 20, 50, or 100 Volts/Volt—much like a classic oscilloscope amplifier plug-in or lab amplifier with a gain knob, but *much* smaller. This tiny DC-coupled, low-noise, self-contained amplifier, useful to low Megahertz frequencies, replaces expensive combinations of op amps and resistor arrays. The 8-lead TSOT-23 package needs no other analog components. The LTC6910-1 operates from single or dual supplies, 2.7V to 10.5V total, and generates its own ground reference for use with single supplies. A simple 3-bit CMOS digital input controls the gain.

The LTC6910-1 is an inverting voltage amplifier with a rail-to-rail output. At gains of unity and zero (digital inputs 001 and 000) it handles rail-to-rail input signals. At gains above unity (digital input 010 through 111), the input-referred noise decreases with increasing gain, as desired in a variable-gain amplifier for a wide range of input levels. When set for a gain of zero (digital input 000), the output remains active (tracking the analog-ground or AGND pin), but feedthrough from the signal input pin is low, typically –122dB at 20kHz and –100dB at 200kHz. Output noise in this zero-gain setting is typically 5.8μV_{RMS} in a 200kHz bandwidth, which is 116dB (19 equivalent bits) below the maximum signal output at a 10V power supply. The output will source or sink 10mA into a load, and is current-limited at approximately 30mA. Typical standing supply current is 2mA at 2.7V and 3mA at 10V total V_{SUPPLY}.

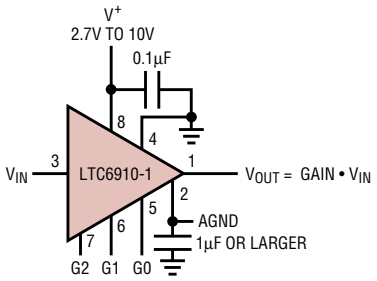


Figure 1. Single-supply programmable amplifier using LTC6910-1

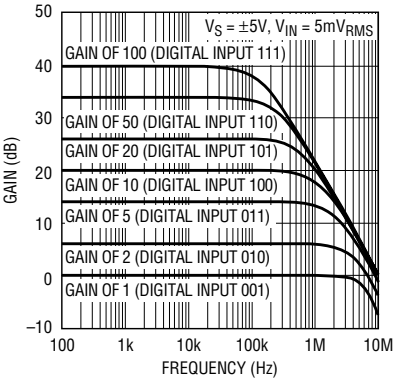


Figure 2. LTC6910-1 frequency response at non-zero gain settings

Easy to Use

The LTC6910-1 amplifier has only three analog signal pins: input, output, and an analog-ground reference (AGND), which can provide a half-supply reference for single-supply applications (Figure 1). The other pins are the power supply and the three digital input pins. These high-impedance CMOS digital inputs accept both rail-to-rail logic levels at any supply voltage, and 0V and 5V levels when the supply voltage is ±5V. Table 1 relates the 3-bit input code to the resulting voltage gain and other characteristics. (Other versions of the product are the LTC6910-2 with 0–64 binary gain code and the LTC6910-3 with 0–7 gain code.) Figure 2 shows the typical frequency response.

Circuit Description

Internally the LTC6910-1 includes an operational amplifier, switched

Table 1. LTC6910-1 gain settings and properties

G2	G1	G0	Nominal Voltage Gain		Maximum Input Signal (For Unclipped Output Signal) (V_{P-P})			Nominal Input Impedance (kΩ)
			Volts/Volt	(dB)	Dual 5V Supply	Single 5V Supply	Single 3V Supply	
0	0	0	0	–120	10	5	3	(Open)
0	0	1	–1	0	10	5	3	10
0	1	0	–2	6	5	2.5	1.5	5
0	1	1	–5	14	2	1	0.6	2
1	0	0	–10	20	1	0.5	0.3	1
1	0	1	–20	26	0.5	0.25	0.15	1
1	1	0	–50	34	0.2	0.1	0.06	1
1	1	1	–100	40	0.1	0.05	0.03	1

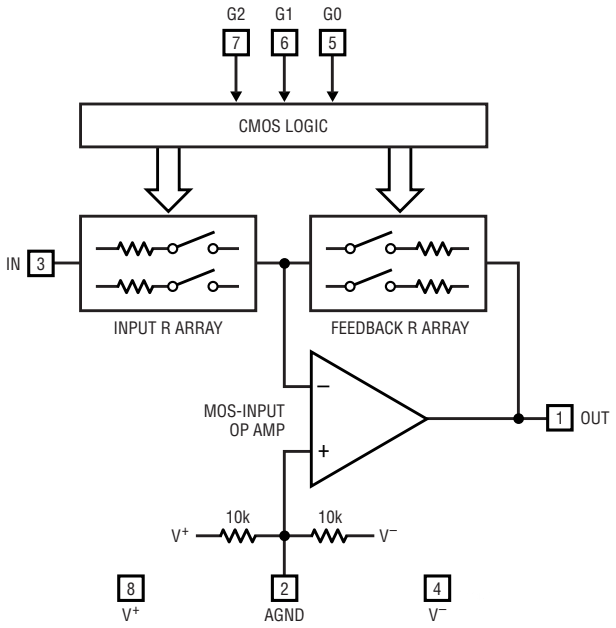


Figure 3. Block diagram of LTC6910-1

resistors, and CMOS decoding logic to drive the switches (Figure 3). The gain code is always monotonic: an increase in the 3-bit binary number (G2 G1 G0) increases the gain between the IN and OUT pins. For single-supply applications, an internal matched pair of 10kΩ resistors at the AGND pin generates a convenient half-supply reference voltage for input and output. The user can override this built-in analog ground reference by tying the AGND pin to a system reference voltage (within the AGND voltage range specified in the data sheet). The AGND pin presents a nominal impedance of 5kΩ due to the internal resistor pair. Digital inputs (G2 G1 G0) control the input and feedback resistances in the closed-loop amplifier.

In the design of the LTC6910-1, the lowest noise with gain variation would be achieved by varying the input R array in Figure 3. That, however, would impose a 100:1 input-resistance range for the closed-loop amplifier with a 100:1 gain range. To avoid such a wide variation of input resistance, logic in the LTC6910-1 trades off changing the input resistance and the feedback resistance (Table 2). This gain-control approach still produces near-minimal noise. When the gain setting is zero (digital input 000), switches disconnect the IN pin internally and short the feedback path in Figure 3 to reduce signal feedthrough and noise.

Table 2. Resistor values in LTC6910-1

Gain	R_{IN}	R_{FB}
0	∞	0
1	10k	10k
2	5k	10k
5	2k	10k
10	1k	10k
20	1k	20k
50	1k	50k
100	1k	100k

Bandwidth of the LTC6910-1 depends on gain setting. The lower gain settings of 1, 2, and 5V/V (digital inputs 001–011) exhibit –3dB corner frequencies respectively of 7, 5, and 2.5MHz at ±5V supply (Figure 2). The gain-control strategy described above causes the gain settings from 10 to 100 (digital inputs 100–111) to show a different high-frequency response, with a constant gain-bandwidth product of approximately 11MHz.

Figure 4 is a SINAD curve showing signal output more than 100dB above combined noise and distortion, with large-signal outputs and a ±5V supply.

Applications

Expanding an ADC's Dynamic Range

Figure 5 shows a compact data-acquisition system for wide-ranging input levels, which combines an LTC6910-1 programmable amplifier in an 8-lead TSOT-23 with an LTC1864 analog-to-digital converter

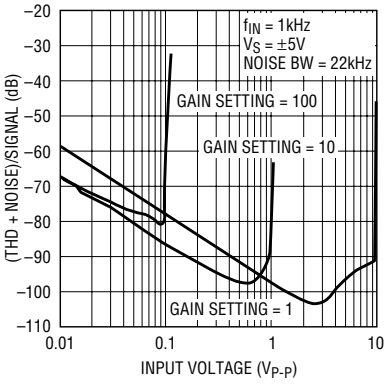


Figure 4. LTC6910-1 THD plus noise, referred to the signal output

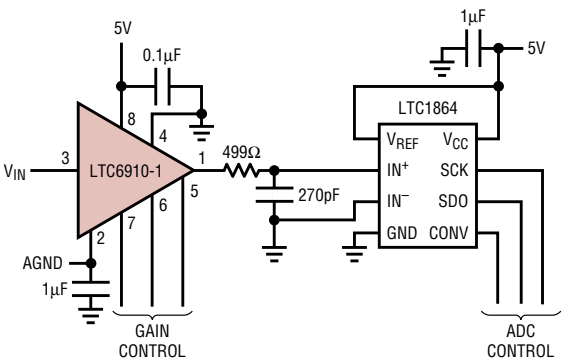


Figure 5. Expanding an ADC's dynamic range

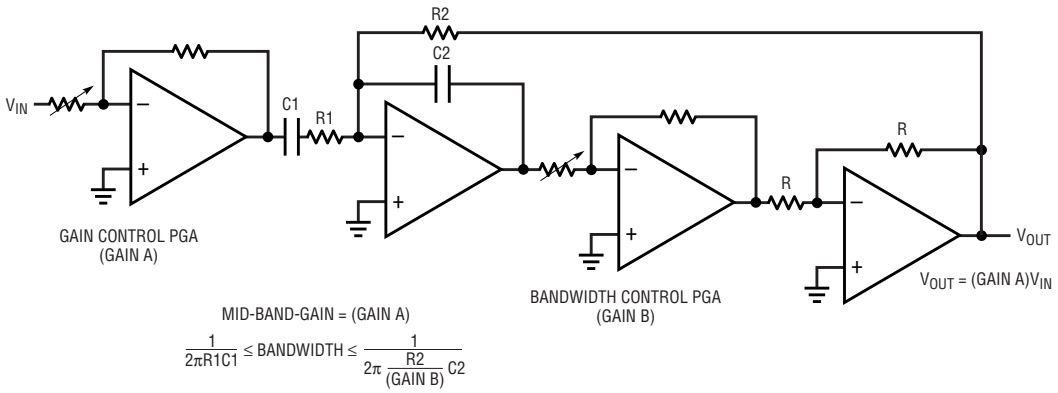


Figure 6. Low-noise AC amplifier with gain and bandwidth control

(ADC) in an 8-lead MSOP. The LTC1864 ADC has 16-bit resolution and a maximum sampling rate of 250ksps. The LTC6910-1 expands the ADC's input amplitude range by 40dB while operating from the same single 5V supply. The 499Ω resistor and 270pF capacitor couple cleanly between the LTC6910-1's output and the switched-capacitor input of the LTC1864.

The two ICs shown in Figure 5 have similar distortion performance, with total harmonic distortion (THD) levels about –90dB at 10kHz and –77dB at 100kHz. At a gain setting of 10 in the LTC6910-1 (digital input 100) and a 250ksps sampling rate in the LTC1864, a 100kHz input signal at 60% of full scale shows a THD of –75dB from the combination. 10kHz input signals under the same conditions produce measured THD values around –87dB. Noise effects (both random and quantization) in the ADC are divided by the gain of the amplifier and combined with the amplifier's noise when referred to V_{IN} in Figure 5. Because of this, the circuit can acquire a signal that is 40dB down from full scale of $5V_{P-P}$ with an SNR of over 70dB. Such performance from an ADC alone (110dB of useful dynamic range at 250ksps) would be prohibitively expensive today.

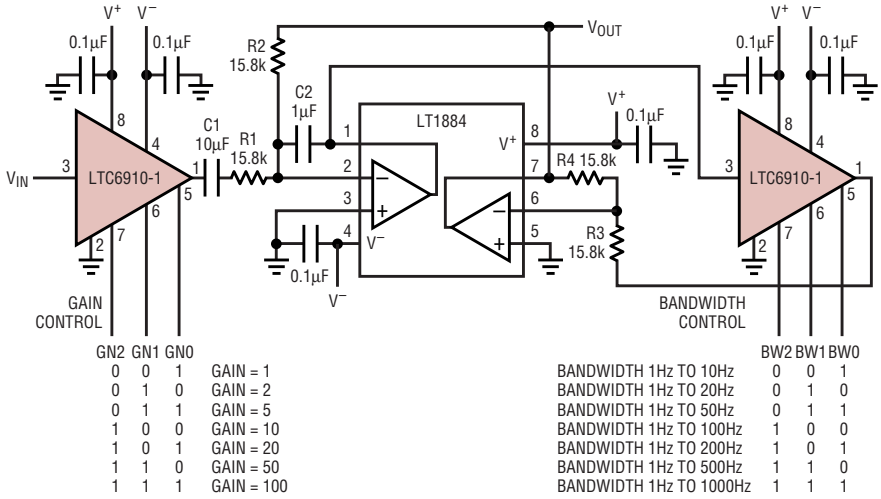


Figure 7. Practical low-noise AC amplifier with gain and bandwidth control

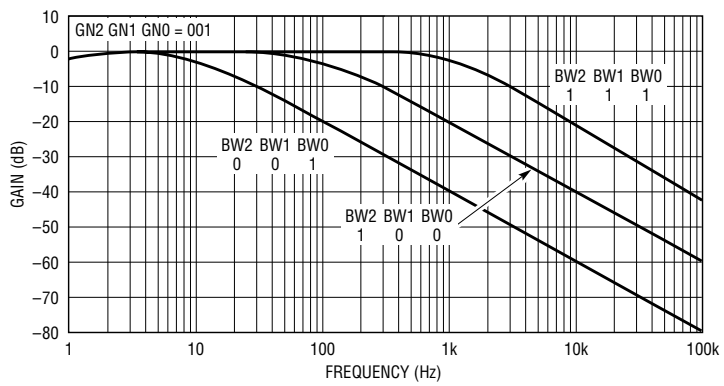


Figure 8. Measured frequency responses for Figure 7

Low Noise AC Amplifier with Programmable Gain and Bandwidth

Analog data acquisition can exploit band-limiting as well as gain, to suppress unwanted signals or noise. Tailoring an analog front end to both the level and bandwidth of each source maximizes SNR.

Figure 6 shows a block diagram and Figure 7 the practical circuit for a low-noise amplifier with gain and bandwidth independently programmable over 100:1 ranges. One LTC6910-1 controls the gain and another controls the bandwidth. An LT1884 dual op amp forms an integrating lowpass loop with capacitor C2 to set the programmable upper corner frequency. The LT1884 also supports rail-to-rail output swings over the total supply-voltage range of 2.7V to 10.5V. AC coupling through capacitor C1 establishes a fixed low

continued on page 24

Programmable Quad Supervisors Offer Unparalleled Flexibility for Multi-Voltage Monitoring Applications

by Bob Jurgilewicz

Introduction

Three new power supply supervisors improve system reliability by offering more accurate reset thresholds than other supervisors on the market. They also save design time, production costs and board space with easy-to-use, flexible interfaces and a low external parts count.

The LTC2900, LTC2901 and LTC2902 quad supervisors can simultaneously monitor four supply voltages with 1.5% threshold accuracy over temperature. Each part offers 16 user-selectable four-voltage combinations from the following: 5V, 3.3V, 3V, 2.5V, 1.8V, 1.5V, +ADJ and –ADJ. A simple external resistor divider performs single-pin programming, eliminating the need to qualify, source and stock different part numbers for different combinations of supply voltages. All three parts are configured for 5% power supply tolerance and the LTC2902 can also be programmed to work with power supplies at 7.5%, 10% and 12.5% tolerance. These new devices require no software, no calibration and no trimming. In some applications, they can be used with no external components, saving additional board space and cost. Available features include manual reset, watchdog functions, selectable supply tolerance and supply margining functions. The reset and watchdog times are also user adjustable via external capacitors.

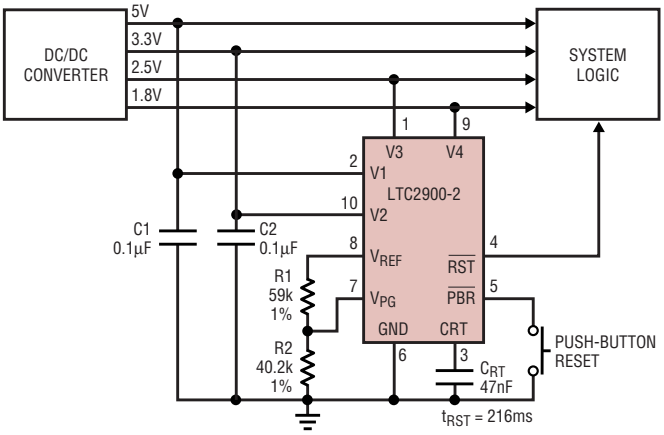


Figure 1. Typical application using the LTC2900-2 for 4-line voltage monitoring

These new devices require no software, no calibration and no trimming

The LTC2900, LTC2901 and LTC2902 supervisors offer micropower operation, small size, high accuracy and multiple reset output options. The extensive integrated functionality makes these devices easy to design into multi-voltage supervisory applications. Table 1 shows a feature summary for these devices. Figure 1 shows a fixed quad application with push-button reset using the LTC2900-2.

Table 1. LTC2900, LTC2901 and LTC2902 Feature Summary

Feature	LTC2900	LTC2901	LTC2902
Programmable Input Threshold Combinations	16	16	16
Threshold Accuracy	1.5%	1.5%	1.5%
"Open-drain" Reset LTC290x-1	●	●	●
Push-Pull Reset LTC290x-2	●	●	●
Adjustable Reset Time	●	●	●
Buffered Reference	●	●	●
Individual Comparator Outputs		●	●
Manual Reset	●		
Independent Adjustable Watchdog Circuitry		●	
Reset Disable			●
Monitored Supply Tolerance	Fixed 5%	Fixed 5%	User Selectable 5%, 7.5%, 10%, 12.5%
Package	10-lead MSOP	16-lead SSOP	16-lead SSOP

Safe Beginnings: Generating the Power-On Reset (POR)

Reliable operation in many systems requires knowledge of when certain power supplies have exceeded minimum thresholds and have remained stable for a specified period of time. One way to provide that knowledge is with a reliable Power-On Reset (POR) signal generated from a highly accurate voltage monitor.

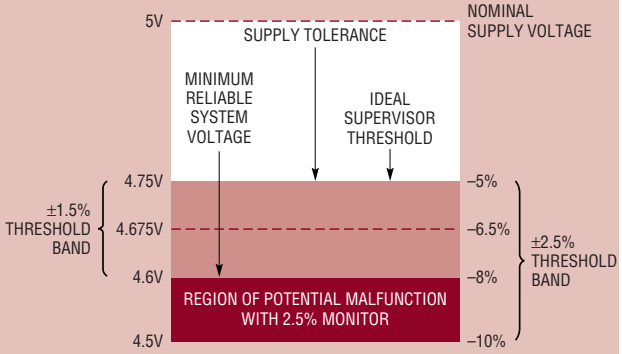
Why is Threshold Accuracy Important?

A system voltage margin specification must take three factors into account: power-supply tolerance, IC supply voltage tolerance and supervisor reset threshold accuracy. If a system is to work reliably, none of these can be left out of the design equation. The roles of the power-supply voltage tolerance and the IC supply voltage tolerance are fairly straightforward, but the role of supervisor accuracy in reliable system design is not as obvious. In the simplest terms, diminished accuracy corresponds to a system that must operate reliably over a wider voltage range, complicating the system design; whereas improved accuracy decreases the voltage margin required for reliable system operation, simplifying the system design.

Consider a 5V system with a ±5% power supply tolerance band (see the figure in this sidebar). System ICs powered by this supply must operate reliably within this band (and a little more, as explained below). The bottom of the supply tolerance band, at 4.75V (5V–5%), is the exact voltage at which a *perfectly accurate* supervisor would generate a reset. Such a perfectly accurate supervisor does not exist—the actual reset threshold may vary over a specified band (±1.5% for the LTC2900, LTC2901 and LTC2902 supervisors).

With this variation of reset threshold in mind, the nominal reset threshold of the supervisor is set *below* the minimum supply voltage; just enough so that the reset threshold band and the power supply tolerance bands do not overlap. If the two bands do overlap, the supervisor could generate a false or nuisance reset when the power supply is actually within its specified tolerance band (say, at 4.8V).

The LTC2900, LTC2901 and LTC2902 have ±1.5% reset threshold accuracy, so 5% thresholds are typically set to 6.5% below the nominal input voltage. For the 5V input, the typical threshold is 4.675V, or 75mV below the ideal threshold of 4.750V. The actual threshold is guaranteed to lie in the band between 4.750V and 4.600V over temperature. The powered system must work reliably down to the low end of the threshold band, or risk malfunction before a reset signal is properly issued. In our 5V example, using the 1.5% accurate supervisor, the system ICs must work down to 4.6V. The same system using a ±2.5% accurate supervisor must operate down to 4.5V, increasing the required system voltage margin, and the probability of system malfunction.



Improved undervoltage monitor threshold accuracy translates to improved system reliability

A typical device that requires a reliable POR signal is a microprocessor. The LTC2900, LTC2901 and LTC2902 can prevent a processor from executing instructions until all supply voltages have reached safe thresholds, regardless of the power supply turn-on characteristics. Furthermore, if any supply voltage falls back below a threshold with sufficient duration and magnitude, the reset command is reissued. Once the voltage has returned above the threshold and has remained there for a specified amount of time, the reset line is released.

In order to firmly establish the correct reset logic state, power must get to the reset drive circuitry early in the power-up phase. The LTC2900, LTC2901 and LTC2902 supervisors are powered automatically from the greater of the voltages on the V1 and V2 inputs. With V1 or V2 at 1V or greater, the reset output is specified to be a logic low of 0.3V (max) while sinking 100µA.

One Chip Covers All Supply Voltages: Single Pin Programming

The LTC2900, LTC2901 and LTC2902 ICs give designers the freedom to specify one chip for all supervisory applications, even though the nominal supply voltages may not be finalized. The desired input voltage combination is selected by placing a simple resistive divider between the reference pin (V_{REF}) and ground (GND) and connecting the tap point to the programming pin (V_{PG}), as shown in Figure 2. The programming process occurs during power-up and is transparent to the user. Table 2 specifies the recommended 1% resistor values for programming the available input combinations. The last column in

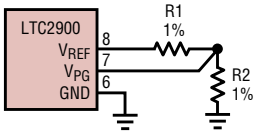


Figure 2. Programming the voltage monitoring modes (see table 2 for R1 and R2 values)

Table 2. Voltage Threshold Programming

Mode	V1 (V)	V2 (V)	V3 (V)	V4 (V)	R1 (kΩ)	R2 (kΩ)	V_{PG}/V_{REF}
0	5.0	3.3	ADJ	ADJ	Open	Short	0.000
1	5.0	3.3	ADJ	–ADJ	93.1	9.53	0.094
2	3.3	2.5	ADJ	ADJ	86.6	16.2	0.156
3	3.3	2.5	ADJ	–ADJ	78.7	22.1	0.219
4	3.3	2.5	1.5	ADJ	71.5	28.0	0.281
5	5.0	3.3	2.5	ADJ	66.5	34.8	0.344
6	5.0	3.3	2.5	1.8	59.0	40.2	0.406
7	5.0	3.3	2.5	1.5	53.6	47.5	0.469
8	5.0	3.0	2.5	ADJ	47.5	53.6	0.531
9	5.0	3.0	ADJ	ADJ	40.2	59.0	0.594
10	3.3	2.5	1.8	1.5	34.8	66.5	0.656
11	3.3	2.5	1.8	ADJ	28.0	71.5	0.719
12	3.3	2.5	1.8	–ADJ	22.1	78.7	0.781
13	5.0	3.3	1.8	–ADJ	16.2	86.6	0.844
14	5.0	3.3	1.8	ADJ	9.53	93.1	0.906
15	5.0	3.0	1.8	ADJ	Short	Open	1.000

Table 2 specifies optimum V_{PG}/V_{REF} ratios (±0.01) to be used when programming with a ratiometric DAC.

Monitor Any Positive or Negative Voltage: Configuring the Adjustable Inputs

Voltages not explicitly listed in Table 2 can be monitored using the positive adjustable (ADJ) and negative adjustable (–ADJ) inputs. The positive adjustable threshold available on the V3 or V4 input is set to 0.5V. For the majority of positive adjustable applications, the tap point on an external resistive divider (R3, R4) placed between the positive voltage being sensed and ground is connected to the high impedance input on V3 or V4. Figure 3 demonstrates a generic setup for the positive adjustable application.

The negative adjustable threshold available on the V4 input is tied to ground. In negative adjustable applications, the tap point on an external resistive divider (R3, R4) placed between the negative voltage being sensed and V_{REF}, is connected to the high impedance input on V4. The voltage on the V_{REF} pin (1.210V nominal) provides the necessary and accurate level shift required to operate near ground. The V_{REF} pin can source and sink up to 1mA of current over the full temperature range –40°C to 85°C. Figure 4 shows a generic setup for the negative adjustable application.

It is also possible to monitor voltages between ground and +0.5V using the positive adjustable inputs. Similar to the offset technique in the negative adjustable application, tie a resistor from V_{REF} to the V3 or V4 input, and an appropriate resistor to the monitored voltage.

Quality System Design: Consider Threshold Accuracy and Noise Sensitivity

System reliability depends on power supply reset thresholds that remain accurate over temperature and power supply variations (see sidebar). All LTC2900, LTC2901 and LTC2902 supervisor inputs have the same relative threshold accuracy: ±1.5% of the nominal input voltage over temperature (see Figure 5).

In any supervisory application, supply noise riding on the monitored DC voltage can cause spurious resets, particularly when the monitored voltage is already near the reset threshold.

One commonly used, but problematic, solution to this problem is the addition of hysteresis to the input comparator. The amount of hysteresis is usually specified as a percentage of the trip threshold, and typically needs to be added to the advertised accuracy of the part in order to determine the true accuracy on the trip threshold. This technique degrades accuracy, and therefore is

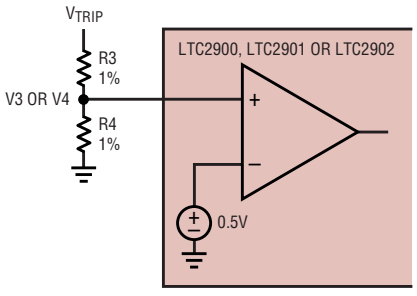


Figure 3. Setting the positive adjustable trip point, $V_{TRIP} = 0.5V(1 + R3/R4)$

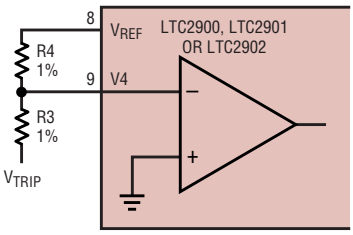


Figure 4. Setting the negative adjustable trip point ($V_{TRIP} = -V_{REF}(R3/R4)$)

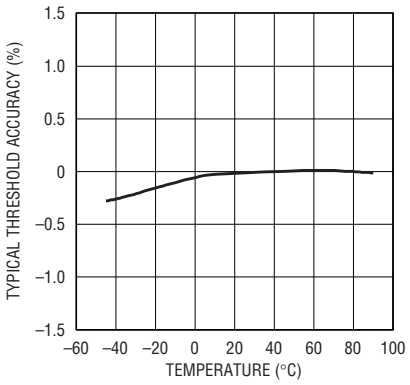


Figure 5. Typical threshold accuracy vs temperature (LTC2900, LTC2901 and LTC2902)

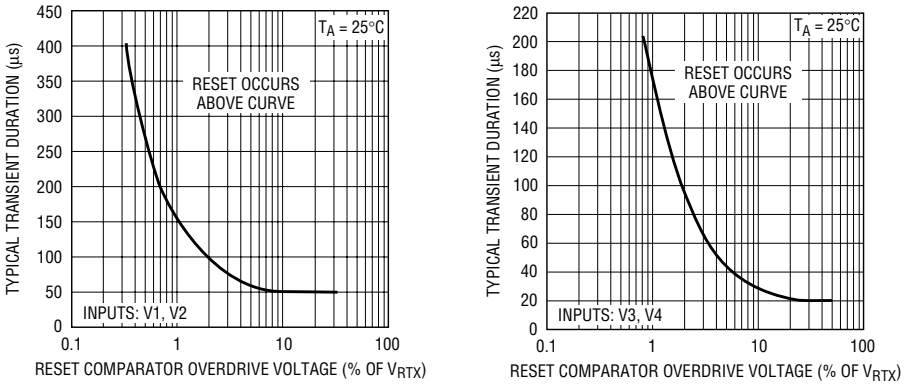


Figure 6. Typical transient duration versus overdrive required to trip comparator

not used on the LTC2900, LTC2901 and LTC2902 supervisors.

Instead, two forms of noise filtering are employed to minimize spurious resets while maintaining system accuracy.

The first line of defense used to minimize the effect of noise is a proprietary tailoring of the comparator transient response. Transient events receive a form of electronic integration in the comparator and must be of sufficient magnitude and duration to cause the comparator to switch. Figure 6 illustrates the typical transient duration versus comparator overdrive (as a percentage of the trip threshold V_{RTx}) required to trip the comparators.

The second filtering method, which is under user control (see next section), is the adjustment of the reset time-out period (t_{RST}) or reset "delay time". A capacitor (C_{RT}) attached between the CRT pin and ground sets the reset time-out period. When any supply drops below its threshold, the reset line is brought low. The reset time-out counter starts once all inputs are back above threshold. The counter is cleared whenever any input drops back below threshold. A noisy input with frequency components of sufficient magnitude above $f = 1/t_{RST}$ effectively holds the reset line low, preventing oscillatory behavior on the reset line.

Although all four supply monitor comparators have built-in glitch filtering, bypass capacitors on V1 and V2 are recommended because the greater of V1 or V2 is also the V_{CC} for the chip (a 0.1µF ceramic capacitor is satisfactory in most applications). Filter capacitors on the V3 and V4 inputs are allowed and recommended in extremely noisy situations.

User Adjustable Reset Time-Out Period

The reset time-out period (t_{RST}) is adjustable in order to accommodate a variety of applications. The period is adjusted by connecting a capacitor, C_{RT}, between the CRT pin and ground. The value of this capacitor is determined from:

$$C_{RT} = t_{RST} \bullet 217 \bullet 10^{-9}$$

with C_{RT} in Farads and t_{RST} in seconds. Maximum reset timeout is limited by the largest available low-leakage capacitor. The accuracy of the time-out period is affected by capacitor leakage and capacitor tolerance. To maintain timing accuracy, capacitor leakage must be well below the 2µA nominal charging current.

Reset Output Options and Individual Comparator Outputs

The reset output line is available in two styles, open-drain (LTC2900-1, LTC2901-1 and LTC2902-1) and push pull (LTC2900-2, LTC2901-2 and LTC2902-2). The open-drain output actually contains a weak pull-up current source to the V2 input, so an external pull-up resistor is only required when the output needs to pull to a higher voltage and/or when the reset output needs a fast rise time. The open-drain output allows for wired-OR connections and can be useful when more than one signal needs to pull down on the reset line. The non-delayed individual comparator outputs available on the LTC2901 and LTC2902 also have open-drain outputs with identical pull-up characteristics. When externally pulling up to voltages higher than V2, an internal network is automatically enabled to protect the weak pull-up circuitry from reverse currents.

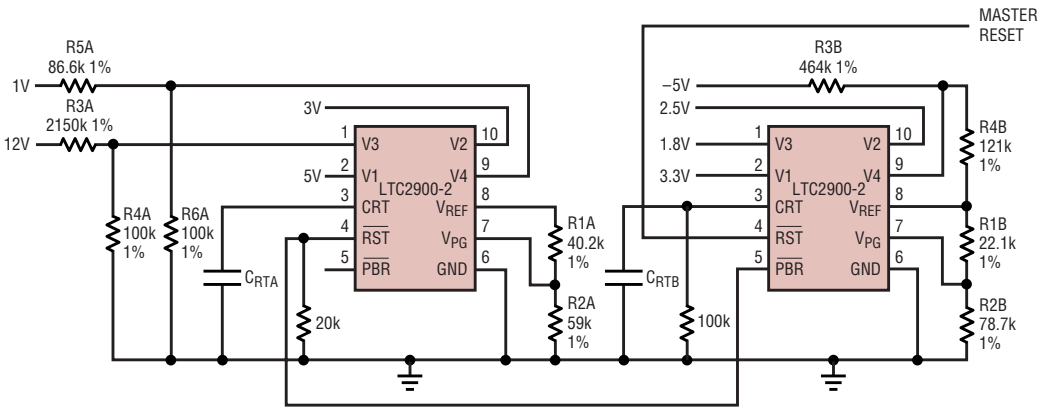


Figure 7. Two supervisors cascaded to monitor eight voltages

The push-pull reset output has a much stronger active pull-up capability, also to the V2 input, resulting in a faster, low voltage drop pull-up characteristic. Wired-OR connections and/or external pull-ups are not recommended with the push-pull reset output option.

Ensuring Reset Valid for V_{CC} down to 0V (LTC2900-2, LTC2901-2 and LTC2902-2)

Some applications require the reset output ($\overline{RST}$) to be valid with V_{CC} down to 0V. The LTC2900-2, LTC2901-2 and LTC2902-2 are designed to handle this requirement with the addition of an external resistor from $\overline{RST}$ to ground. The resistor will provide a path for stray charge and/or leakage currents, preventing the $\overline{RST}$ output from floating to undetermined voltages when connected to high impedance (such as CMOS logic inputs). The resistor value should be small enough to provide effective pull-down without excessively loading the active pull-up circuitry. Too large a value may not pull-down well enough. A 100k resistor from $\overline{RST}$ to ground is satisfactory for most applications.

Manual Reset Feature on the LTC2900

The manual reset or push-button reset pin ($\overline{PBR}$) on the LTC2900 is used to issue a forced reset, typically with a normally-open pushbutton switch attached between $\overline{PBR}$ and ground. The $\overline{PBR}$ pin is pulled to V_{CC} with an internal current source of 10µA (typical). The switch is debounced through the reset circuitry using the delay provided by the C_{RT} timing capacitor. A logic low on this pin will pull $\overline{RST}$ low. When the $\overline{PBR}$ pin returns high, $\overline{RST}$ will return high after the reset time-out period has elapsed, assuming all four voltage inputs are above their thresholds. The $\overline{PBR}$ pin may also be driven by a logic signal. The input-high threshold on the $\overline{PBR}$ pin is 1.6V (max), allowing the pin to be driven by low-voltage logic. Figure 7 demonstrates a supervisory cascade using two LTC2900-2 ICs to monitor 8 voltages. The reset output of the first supervisor is tied to the $\overline{PBR}$ input of the second which holds the master reset low while the voltages on the first supervisor are below threshold. When all eight voltages are above threshold, the master reset is released after the delay provided by the second reset timing capacitor (C_{RTB}).

Independent Watchdog Features on the LTC2901

The LTC2901 contains independent watchdog circuitry consisting of a watchdog input (WDI), a watchdog output ($\overline{WDO}$) and a timing pin (CWT) that allows for a user adjustable watchdog time-out period. An undervoltage condition on any supervisor input causes $\overline{RST}$ to go low which clears the watchdog timer and brings $\overline{WDO}$ high. The watchdog timer is started when $\overline{RST}$ pulls high. Subsequent rising or falling edges received on the WDI pin will clear the watchdog timer. If an edge is not received within the watchdog time-out period, $\overline{WDO}$ will go low. $\overline{WDO}$ will remain low and the watchdog timer will remain cleared until another edge is received on the WDI pin or another undervoltage condition occurs.

The watchdog function is typically used to monitor a processor's activity. Consider a system that is no longer executing the correct code, thereby failing to issue an edge to the WDI pin. If the watchdog output is tied to a non-maskable interrupt (NMI), a watchdog timeout will cause the processor to vector to a new program location, which may enable a variety of recovery actions. For example, a motor could be disabled, an interlock could be engaged, critical data could be written to NVRAM, etc.

The watchdog time-out period (t_{WD}) can be optimized for software execution. A capacitor (C_{WT}) connected between the CWT pin and ground sets the watchdog time-out period. The capacitor value is determined from:

$$C_{WT} = t_{WD} \bullet 50 \bullet 10^{-9}$$

with C_{WT} in Farads and t_{WD} in seconds. Maximum timeout is limited by the largest available low-leakage capacitor. The accuracy of the time-out period is affected by capacitor leakage and capacitor tolerance. To maintain timing accuracy, capacitor leakage must be well below the 2µA nominal charging current.

The watchdog circuit can also be used as a clock or frequency monitor by applying a periodic logic signal to the WDI input. If the input signal is

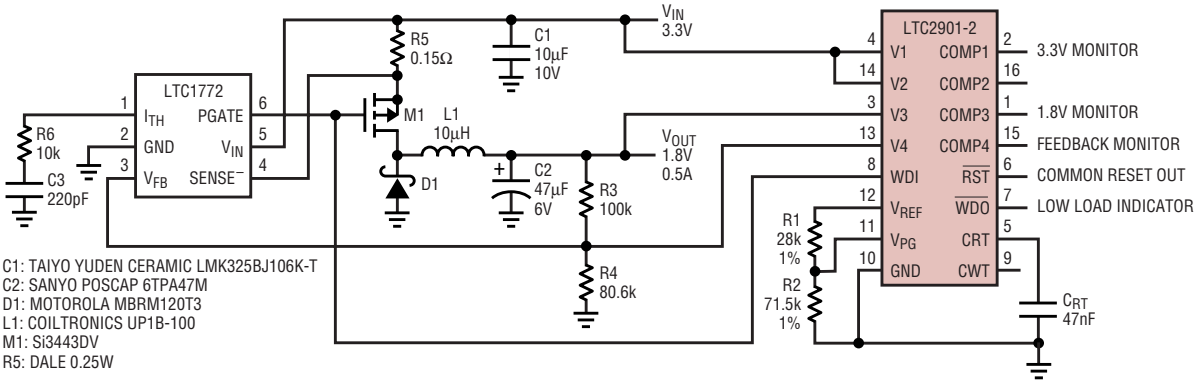


Figure 8. Use the LTC2901-2 to monitor the input, output, feedback voltage and low load conditions on a DC/DC controller. In this case, the controller is an LT1772 used in a 3.3V input to 1.8V output application.

inactive for an amount of time longer than the watchdog time-out period, the $\overline{WDO}$ line falls, indicating a loss of the periodic input. Figure 8 demonstrates how the LTC2901 can be used to monitor a switching regulator's activity. In this application, the 3.3V input, 1.8V output and feedback voltage to the LTC1772 regulator are supervised. Furthermore, if the load goes open circuit, the LTC1772 switches into Burst Mode® operation, reducing the duty cycle at the gate of M1. The pulse spacing exceeds the watchdog time-out period, and the watchdog output falls indicating the low-load condition.

Power Supply Margin Testing with the LTC2902

In high reliability system manufacturing and test, it is desirable to verify the correct operation of electrical components at or below the rated power supply tolerance. The LTC2902 is designed to complement such testing in two ways. First, the reset disable pin ($\overline{RDIS}$) can be pulled low which forces the $\overline{RST}$ output high. With $\overline{RDIS}$ low, moving supply voltages below threshold does not invoke the reset command during margining tests. The individual comparator outputs operate normally with $\overline{RDIS}$ high or low, allowing for individual supply monitoring.

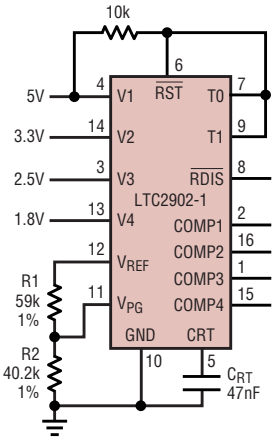


Figure 9. Quad supply monitor with asymmetric hysteresis

The second way allows the user to provide more supply headroom by lowering the trip thresholds. Using the digital tolerance programming inputs (T0, T1), the global supply tolerance can be set to 5%, 7.5%, 10%, or 12.5% (Table 3).

When using the positive or negative adjustable inputs in conjunction with tolerance programming, external resistors need only to be sized once, based on a 5% tolerance threshold. Once the external resistor dividers are set using the 5% tolerance thresholds, the thresholds for the other tolerance modes (7.5%, 10%, 12.5%) are automatically correct because the reference voltage (V_{REF}) is scaled accordingly. Figure 9 shows how the LTC2902 can be configured for asymmetric hysteresis, having 5% tolerance when supplies are rising and 12.5% tolerance after all supplies have safely crossed their 5% thresholds.

Table 3. LTC2902 Tolerance Programming

T0	T1	Tolerance	V_{REF}
Low	Low	5%	1.210V
Low	High	7.5%	1.178V
High	Low	10%	1.146V
High	High	12.5%	1.113V

Conclusion

One part can now satisfy most present and future supervisory needs. The LTC2900, LTC2901 and LTC2902 micropower quad supervisors provide the versatility, accuracy and reliability required in multi-voltage monitoring applications. Input supply combinations are programmable including positive and/or negative adjustable thresholds. The comparators are 1.5% accurate over temperature and feature built-in noise rejection. Reset logic is correct for V_{CC} down to 1V, and is available with open-drain or push-pull outputs. Reset and watchdog times are user adjustable with external capacitors. Power supply margining features include real-time supply tolerance selection and an on-demand reset disable pin.

LTC6910-1, continued from page 18

frequency corner of 1Hz, which can be adjusted by changing C1. Alternatively, shorting C1 makes the amplifier DC-coupled. (When DC is not needed, however, the AC coupling suppresses low frequency noise and all amplifier offset voltages other than the low internally-trimmed LT1884 offset in the integrating amplifier, which is the second amplifier in Figure 6. If desired, another coupling capacitor in series with the input can relax the requirements on input DC level as well.)

Measured frequency responses (Figure 8) demonstrate bandwidth settings of 10Hz, 100Hz, and 1kHz (digital BW inputs of 001, 100, and 111, respectively) and unity gain in each case. By scaling C2, this circuit can serve other frequency ranges, such as a maximum of 10kHz with 0.1µF using LT1884 (gain-bandwidth product around 1MHz). Output signal-to-noise ratio measured with $10mV_{P-P}$ input, gain of 100, and 100Hz bandwidth is 76dB; for $100mV_{P-P}$ input, gain of 10, and 1000Hz bandwidth it is 64dB.

Conclusion

With a printed circuit footprint of only about $11mm^2$, the easy-to-use LTC6910-1 provides two decades of programmable DC or AC voltage gain. It can preamplify, drive loads, and introduce gain flexibility into spaces so small that, as one engineer put it, "your boss doesn't even need to know it's there."

Acknowledgements

Mark Thoren and Derek Redmayne collaborated on the ADC application and Philip Karantzalis contributed the AC amplifier.

Tiny 1.25MHz Monolithic Boost Regulator Has 1.5A Switch and Wide Input Voltage Range

by Keith Szolusha

Introduction

The LT1961 is a monolithic, current-mode, boost converter with a very high switching frequency and an on-board monolithic, high-current power switch. Because the power switch is included in the tiny MSOP 8-pin exposed leadframe package, layout and board space shrink dramatically for most designs. The high 1.25MHz switching frequency further reduces the size requirement for the surrounding inductors and capacitors, by allowing the use of chip inductors and low profile capacitors and inductors. It operates within a 3V to 25V input voltage range and can be synchronized up to 2MHz. The built in 0.2Ω, 35V switch allows up to 1.5A switch current at high efficiency. In battery-powered applications the extremely low 6µA shutdown current maintains high efficiency and long battery life. The shutdown pin also provides an undervoltage lockout option to limit battery source current when low on charge.

The current-mode topology of the IC allows for fast transient response and simple loop compensation techniques that can take advantage of a variety of ceramic output capacitors to cover a wide range of output voltages. Ceramic capacitors have the advantage of smaller size and they can handle high RMS ripple current, the overriding requirement in sizing the output capacitor for boost and flyback topologies.

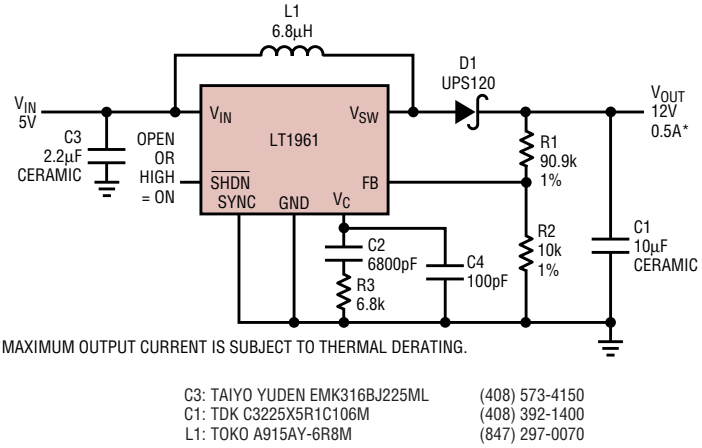


Figure 1. 5V input, 12V output boost converter with ceramic input and output capacitors

A High Efficiency 12V Boost Converter with all Ceramic Capacitors

Figure 1 shows a typical application for the LT1961; a 12V boost converter using only ceramic capacitors. This circuit provides a regulated 12V output from a typical input voltage of 5V, but can also be powered from any input voltage between 3V and 12V. The maximum load current changes as a function of input voltage. Efficiency for the circuit is as high as 87% for a 5V input, as shown in Figure 2. Figure 3 shows the extremely low $60mV_{P-P}$ output voltage ripple at 500mA load. Low-ESR ceramic capacitors and high switching frequency help reduce the peak-to-peak output voltage ripple, even in the normally noisy boost configuration.

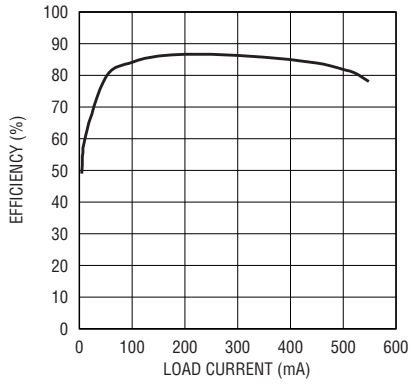


Figure 2. Efficiency of the circuit shown in Figure 1 is as high 87%.

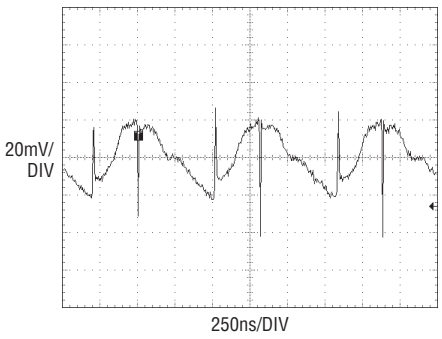


Figure 3. At 500mA load current, the output ripple voltage of Figure 1's circuit is an extremely low 60mV peak-to-peak.

Low Profile 3.0mm SEPIC Has Wide Input Voltage Range

Although the LT1961 is configured as a boost, or step-up, converter, its internal low-side, asynchronous, 1.5A, 35V switch is versatile enough to be used in other applications such as a SEPIC or flyback. SEPIC solutions typically use the basic single-output flyback topology and a transformer with its two windings capacitively coupled together to generate a fixed output voltage from an input voltage that can be either above, equal to, or below the output voltage. However, much of the advantage of the LT1961's high frequency and correspondingly small external components is lost by

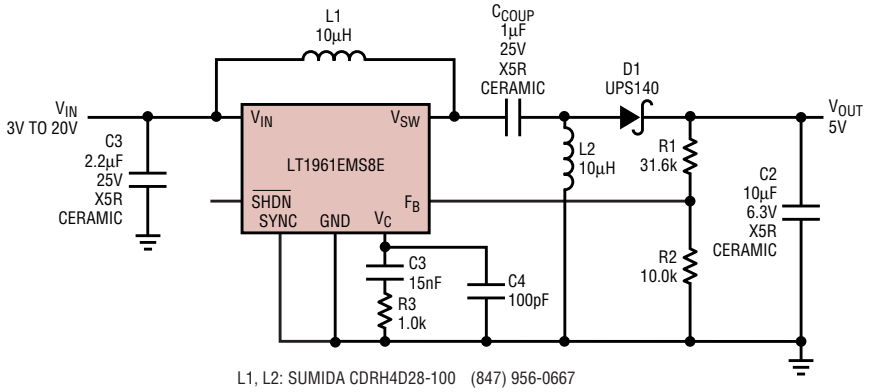


Figure 4. 3V–20V input, 5V output SEPIC saves space by using two low profile inductors and all ceramic capacitors.

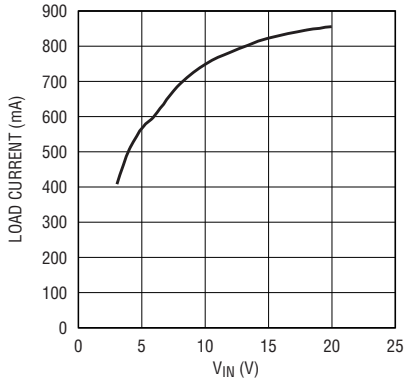


Figure 5. Maximum load current of the low profile SEPIC shown in Figure 4 increases with input voltage.

using a transformer, which is typically tall and occupies a large amount of board space. Instead, Figure 4 shows a way to use two separate inductors to create a low profile SEPIC solution with less than 3.0mm height—desirable for many of today's handheld and portable computer applications. The coupling capacitor replaces the transformer core as the low-impedance path for energy to move from the primary to the secondary side. The coupling capacitor charges up to a steady state voltage—equal to the input voltage—and has enough capacitance to maintain its charge within 5% during switch on and off-times while high ripple current passes back and forth between the primary and secondary sides.

The circuit shown in Figure 4 is a 3V–20V input to 5V output low profile SEPIC featuring the LT1961 with less than 3.0mm height and all ceramic capacitors. This is a tiny, low cost and low profile solution with a wide input voltage range. The maximum load current depends on the input voltage (see Figure 5). The two 10µH inductors limit the ripple. However, each inductor can be sized independently to increase the output current capability. Figure 6 shows that typical efficiency is over 70% and improves as the input voltage approaches the output voltage (5V). In this configuration, the two inductor currents are summed in the switch during the switch on-time and then through the catch diode and the output during the switch off-time. This effectively doubles the switch and catch diode losses compared to the typical boost application. At high input voltages, the duty cycle is low and the catch diode conducts current for a greater proportion of the overall time. At low input voltages, the duty cycle is high and the switch conducts current for a greater proportion of the overall time. The low switch V_{ceSAT} relative to the forward voltage of the catch diode is the reason for the increase in converter efficiency at lower input voltages.

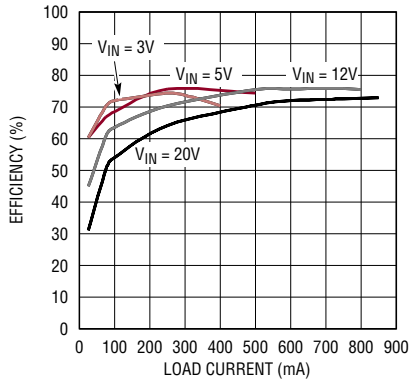


Figure 6. Efficiency of the low profile SEPIC shown in Figure 4 is as high as 76% and increases as the input voltage approaches the output voltage.

Dual Polarity Output SEPIC

Figure 7 is a 5V to 9V input to ±12V dual polarity output converter. As discussed above, the low-side boost converter switch is ideal for flyback converters that usually use a transformer to couple energy from the primary (input) side to the secondary (output) side. For dual polarity output flyback converters, this transformer has at least three windings coupled together on the same core, one for the primary side, and one for each out-

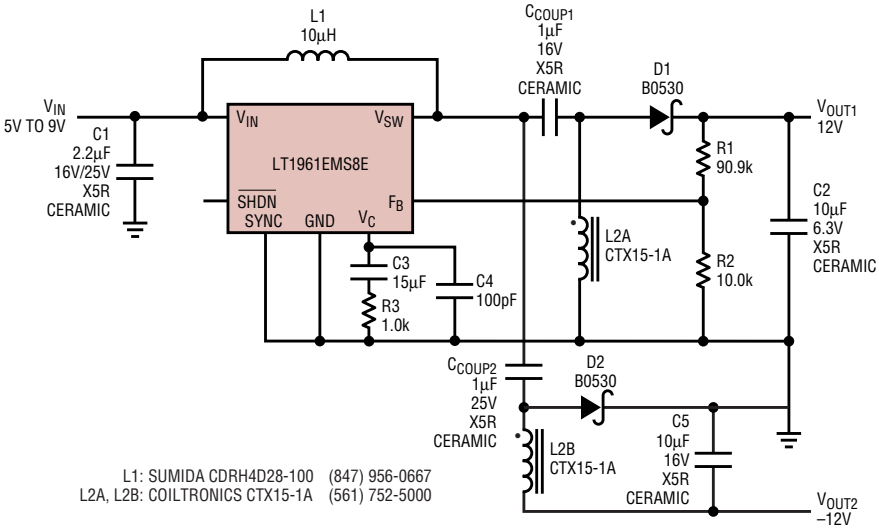


Figure 7. Dual polarity output SEPIC for 5V–9V input to ±12V output. This circuit uses one low profile inductor and one 1:1 off-the-shelf transformer for the two outputs.

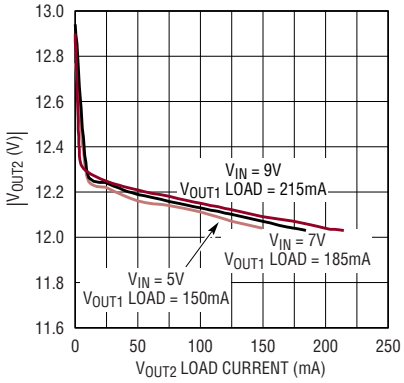


Figure 8. Cross-regulation of Figure 7's circuit with fixed V_{OUT1} load current and varying V_{OUT2} load current.

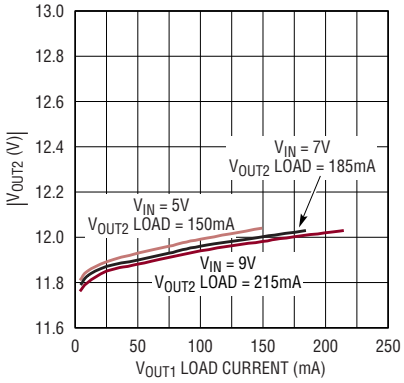


Figure 9. Cross-regulation of Figure 7's circuit with fixed V_{OUT2} load current and varying V_{OUT1} load current.

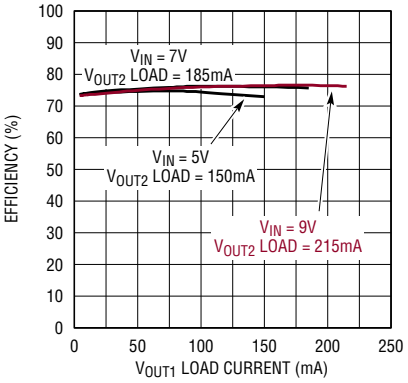


Figure 10. Efficiency of the circuit shown in Figure 7 is typically 75%.

put. Such a transformer, at the power level required (1.5A total parallel current and 3.3µH to 22µH per winding), negates most of the space savings provided by the high frequency LT1961. The solution is to capacitively couple energy from the input to the output transformer like the single output of the low-profile SEPIC using two separate inductors. This not only gets the job done, but reduces the height of the inductive components and provides layout flexibility. 1:1 transformers with only two windings are more readily available and much smaller than transformers with at least three windings.

Cross-regulation is excellent in this converter as shown in Figures 8 and 9. With only a single feedback pin, the positive output voltage always maintains regulation, but the negative output voltage (V_{OUT2}) regulation changes as a function of the difference in the load currents of the two outputs. As one output becomes heavily loaded and other lightly loaded, cross-regulation can become slightly compromised due to differences in losses in the catch diodes and inductors. Figure 8 shows that extremely light loads on V_{OUT2} can result in a loss of regulation, so a preload may be required. However, Figure 9 shows that V_{OUT1} can go to zero load current without a loss in regulation on V_{OUT2}. The overall converter efficiency remains high for a flyback or SEPIC-type design as shown in Figure 10. The maximum load current on each output varies as a function of the load on the other output. Figure 11 shows the maximum matched load current (the same load current on both outputs). If one load current is decreased, the other can be increased without exceeding current limit.

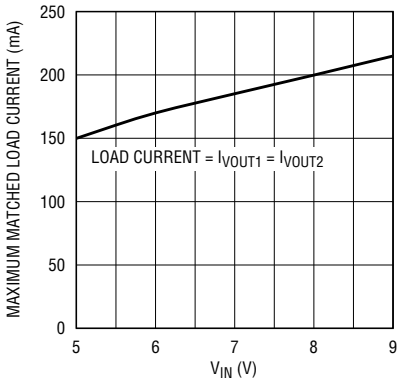


Figure 11. Maximum individual output load current (with equal loads on V_{OUT1} and V_{OUT2}) for the circuit of Figure 7, at various input voltages.

Conclusion

The LT1961 is a tiny, monolithic, 1.5A boost converter with a wide input voltage range that can be used in many applications. Its high switch frequency and onboard switch help minimize circuit size and cost.

LTC4257, continued from page 10

Two additional features add flexibility to LTC4257 designs. An open-drain $\overline{\text{PWRGD}}$ output indicates that the voltage drop across the internal power MOSFET has dropped below 1.5V, indicating that any input capacitance has charged, the output has reached its final value, and it is safe to turn on the system. This helps systems that draw the maximum input power stay below the inrush limits at turn on. A SIG_DISA input allows the PD to disable the 25k signature resistance if desired, allowing it to opt not to receive power from the PSE if it is getting it from another source, such as a wall transformer.

Conclusion

The LTC4257 contains virtually all of the circuitry needed to connect a powered device to an IEEE 802.3af Power Over Ethernet network. Signature, classification, power switching, inrush, and fault protection are all included, thus simplifying the required circuitry between the input transformers and the PD voltage regulator. The LTC4257 accomplishes all of this in a space-saving 8-pin SO or DFN package with only one external component, a resistor to program the class current (not needed for class 0).

Part 3 of this series will cover the details of detection and classification from the PSE end of the power network.

Secondary Side Synchronous Post Regulator Provides Precision Regulation and High Efficiency for Multiple Output Isolated Power Supplies

by Charlie Y. Zhao, Wei Chen and Chiawei Liao

Introduction

Many telecom, server and other applications require an isolated power supply with multiple output voltages, but maintaining tight regulation for all of the output voltages can be a power supply designer's headache. Traditionally, a linear regulator is used for each auxiliary output, but efficiency of a linear regulator can be very low, limiting its usage to low output current applications. One alternative to the linear regulator is to use a buck converter as a post regulator. This method can yield better efficiency, but the power supply needs a larger output inductor and capacitor if the post regulator cascades the main output; or it needs an additional rectifier, inductor and capacitor before the post regulator if multiple secondary windings are used. The additional power conversion stage and components increase conduction losses. Another option is to use a magnetic amplifier post regulator. The efficiency of a magnetic amplifier post regulator can be high, especially for low or medium current applications, but is usually low in high current applications. Furthermore, its complex assembly and poor regulation at light load make it less than a perfect solution. A better alternative is a post regulator design that uses the new LT3710.

The LT3710 controller brings simplicity, high efficiency and precision regulation to multiple output isolated power supply applications. The LT3710 is a special synchronous step-down switching regulator controller with dual N-Channel MOSFET drivers. It is used as a high efficiency secondary side synchronous post regulator controller to generate a tightly regulated auxiliary output directly from the rectified transformer secondary winding voltage. This scheme minimizes the size of inductor and output capacitors at the main output stage. The LT3710 is a constant frequency voltage mode controller with programmable current limit protection and up to 500KHz switching frequency. With leading edge modulation, it operates well with a main output control loop that uses either current mode control or voltage mode control.

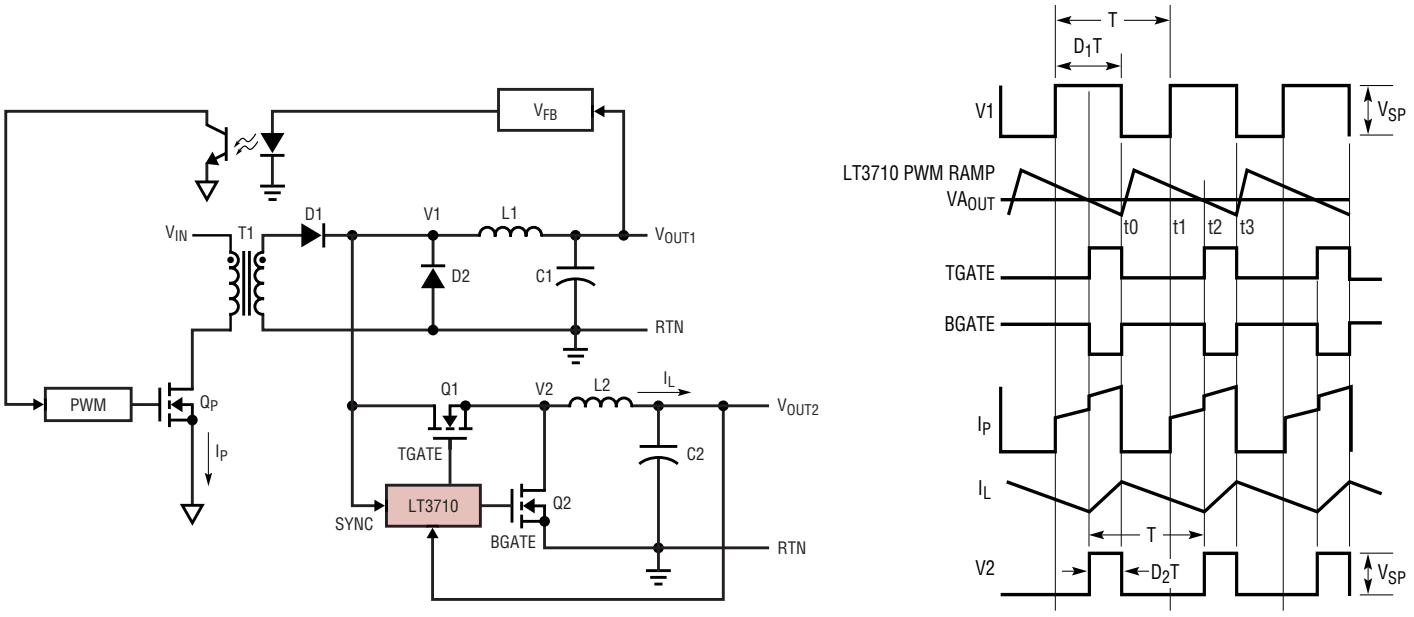


Figure 1. Simplified application schematic and key waveforms

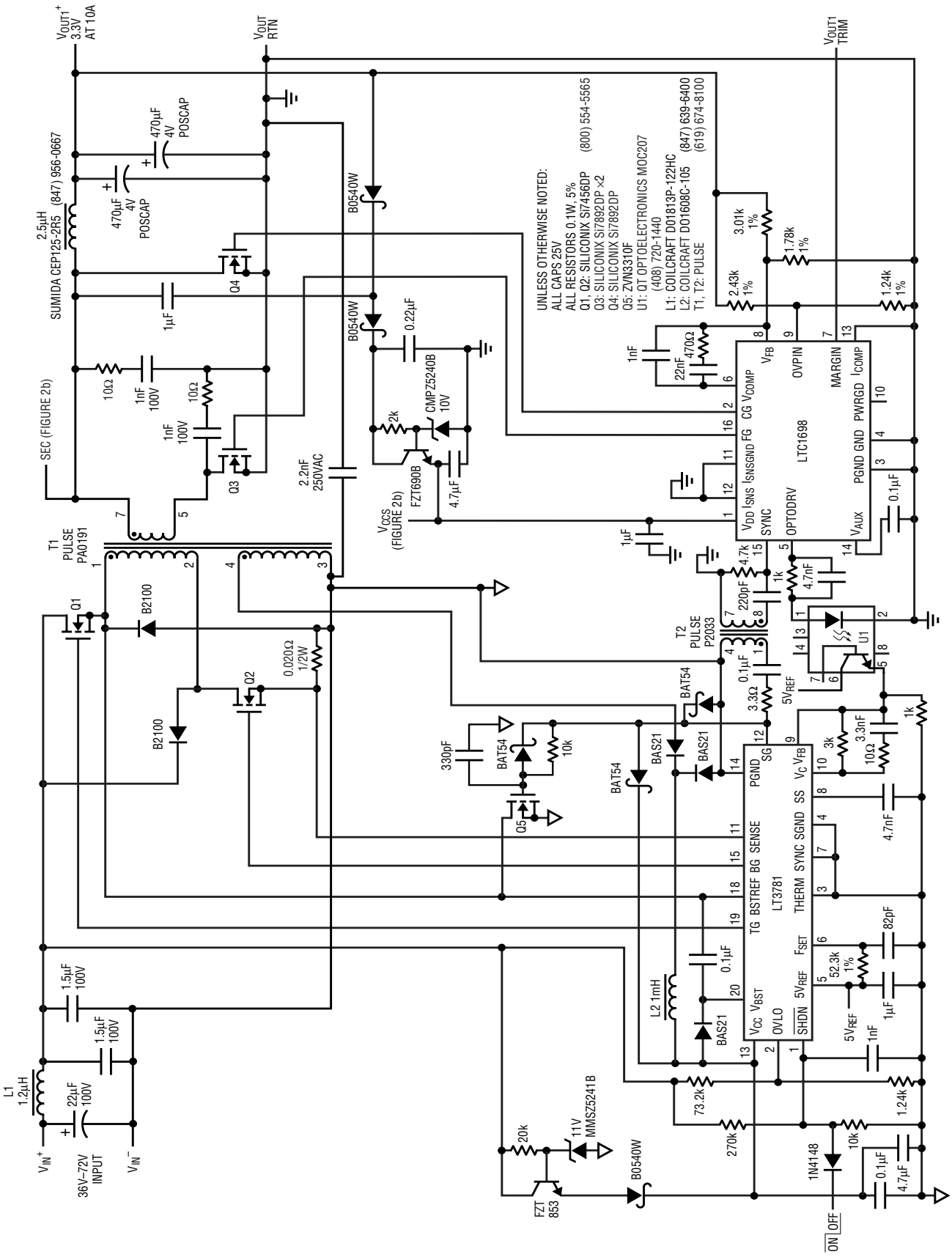


Figure 2a. 36V–72V DC to 3.3V/10A and 1.8V/10A dual output isolated power supply

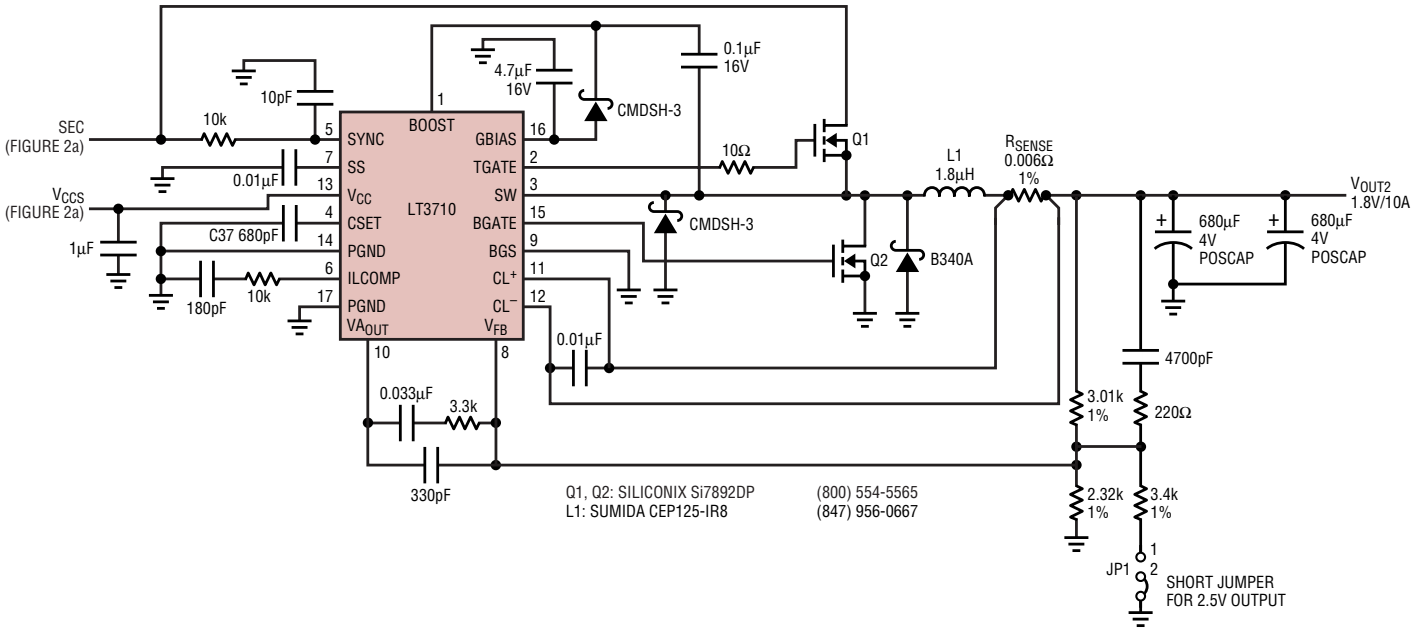


Figure 2b. (continued) 36V–72V DC to 3.3V/10A and 1.8V/10A dual output isolated power supply

LT3710 Post Regulator Operation

The LT3710's basic functional blocks include a voltage amplifier for feedback regulation, a ramp generator synchronized to the secondary side switching pulse, a PWM comparator with leading edge modulation, a current limit amplifier and high speed MOSFET drivers.

Figure 1 shows a simplified LT3710 application circuit and key waveforms. The main output power stage is a forward converter. The LT3710 regulates the auxiliary output V_{OUT2}. The LT3710 circuit looks like a synchronous buck converter except that the input is a pulsed voltage rectified from the power transformer secondary winding.

In normal operation, a switching cycle begins at t_0, the falling edge of the rectified transformer secondary voltage V_1. An internal ramp is triggered to start a new PWM switching cycle, turning off the top MOSFET Q1 (control switch) and turning on the bottom MOSFET Q2 (synchronous switch). From t_0 to t_1, the control switches of both the main converter (Q_P) and the LT3710 circuit (Q1) are "off." At t_1, the rectified transformer secondary voltage V_1 goes high. During the period (t_1 to t_2), the control switch of the main converter is "on" but the control switch of the LT3710 circuit remains "off." The primary switch current I_P equals the reflected main output inductor current, I_{L1}/N, where N is the transformer primary to secondary turns ratio. From t_0 to t_2, the switch node voltage V_2 remains near zero and the auxiliary inductor current I_L is flows into C_{OUT2} and the load across V_{OUT2}. This state lasts until the PWM ramp signal intersects the voltage error amplifier output, V_{AOUT}, at t_2. The top MOSFET Q1 turns on and the bottom MOSFET Q2 turns off. The switch node voltage V_2 is pulled up to the same voltage as V_1 and charges the auxiliary inductor. During the period t_2 to t_3, the control switches of both the main converter and the LT3710 circuit are "on." The primary switch current I_P is the sum of the reflected main output inductor

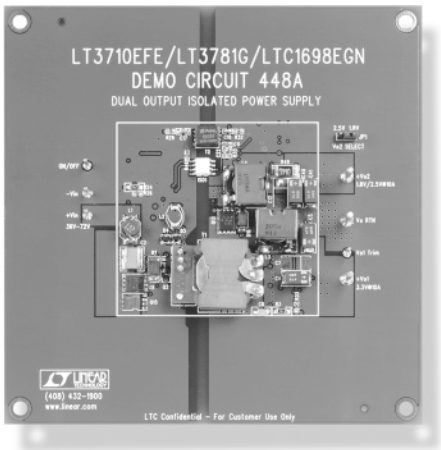


Figure 3. 36V–72V DC to 3.3V/10A and 1.8V/10A dual output isolated power supply

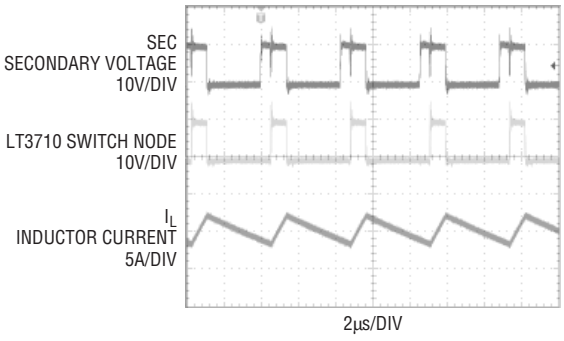


Figure 4. Post regulator input voltage, switch node and inductor current waveforms for 48V input to 3.3V/10A and 1.8V/10A outputs

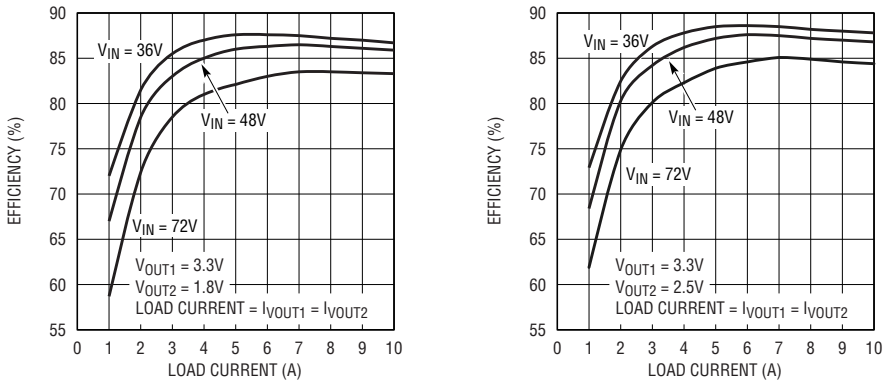


Figure 5. Efficiency vs load current for the circuit in Figure 2

current and the auxiliary output inductor current $(I_{L1} + I_L)/N$ during this stage. This state ends at t_3, when the rectified transformer secondary voltage V_1 becomes zero, and the next switching cycle begins.

There is a step change in the primary switch current at t_2 when the control switch of the LT3710 circuit turns on. Leading edge modulation prevents loop instability even if peak current mode control is used on the primary side.

The synchronization threshold of the LT3710 is about 2.5V. The falling edge of the rectified transformer secondary must pass through this threshold each cycle. To ensure proper synchronization, the LT3710 internal oscillator frequency should be set lower than the system switching frequency.

The auxiliary output V_{OUT2} can range from 0.8V to near the main output voltage V_{OUT1}. The voltage V_{OUT2} can be determined by $D_2 \bullet V_{SP}$, where V_{SP} is the amplitude of the secondary voltage (V_{IN}/N) and D_2 is the duty cycle of the switch node voltage V_2.

Dual Output Isolated 2-Switch Forward Power Supply

Figure 2 shows an application using the LT3710—in this case a dual output high efficiency, isolated DC/DC power supply with 36V to 72V input range and 3.3V/10A and 1.8V/10A outputs. The basic power stage topology is a 2-switch forward converter with synchronous rectification. The primary side controller uses an LT3781, a current mode 2-switch forward controller with built-in MOSFET drivers. On the secondary side, an LTC1698 synchronous rectifier controller provides the voltage feedback for the main 3.3V output, as well as the gate drive for the synchronous MOSFETs. The error amplifier output of the main 3.3V circuit is fed into the optocoupler and then relayed to LT3781 on the primary side to complete the main 3.3V regulation. The auxiliary 1.8V output is precisely regulated by the LT3710 circuit.

Current limiting is also provided by the LT3710 circuit. The current limit can be programmed by the value of the external sensing resistor R_{SENSE} (see Figure 2b), to $70mV/R_{SENSE}$. If current limiting is not required,

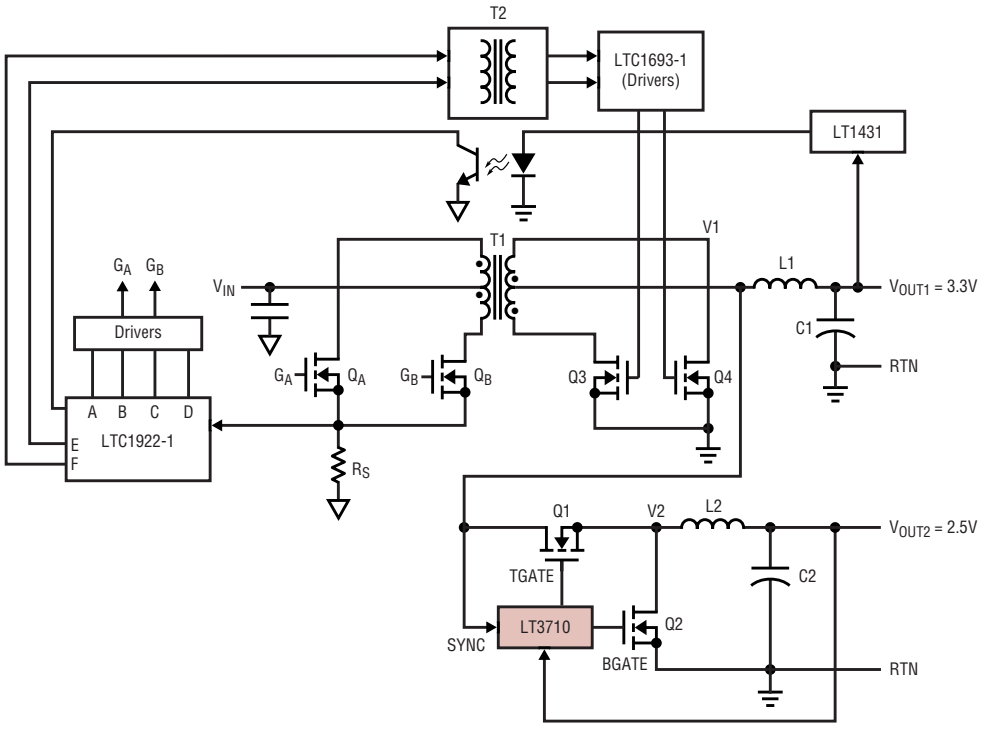


Figure 6. Simplified schematic of a push-pull converter using the LT3710

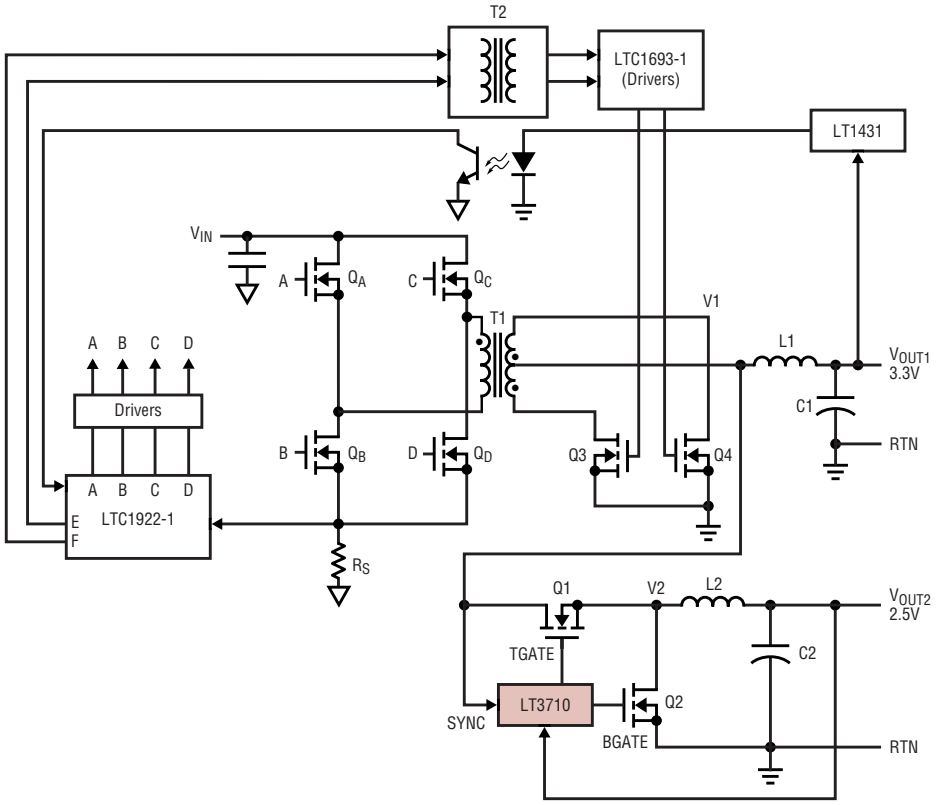


Figure 7. Simplified schematic of a full-bridge converter using the LT3710

ground the current sensing pins CL^+ and CL^-.

A Pulse Engineering planar transformer acts as the power transformer. This transformer is constructed on a PQ20 core with nine turns of primary windings, two turns of secondary windings and seven turns of auxiliary windings for the LT3781 bias supply. Because the maximum secondary winding voltage V_{SP} is about 16V, 30V MOSFETs are chosen with the consideration that the secondary voltage overshoot is typically 20% to 30% of V_{SP}. In this design Si7892DP N-channel MOSFETs were selected for low $R_{DS(ON)}$, a 30V V_{DSS} rating and a compact and thermally enhanced PowerPAK™ SO-8 package.

This circuit provides 1500V input-to-output isolation at switching frequency of 230KHz. Additional features include primary side on/off control, ±5% secondary side trimming on the 3.3V output, input overvoltage protection, undervoltage lockout and board thermal shutdown. The entire circuit is mounted on a standard half brick size PC board with about a half inch height. Figure 3 shows a top side picture of the board.

Figure 4 shows the LT3710 post regulator input voltage, switch node voltage and inductor current waveforms with 48V input to 3.3V/10A and 1.8V/10A outputs. The efficiency curve of this circuit is shown in Figure 5. With a 48V input and full loads on both main and auxiliary outputs, measured total efficiency is about 86%.

Other Isolated Topologies Using the LT3710

Application of the LT3710 is not limited to forward converter topologies. It can also be used with other buck derived single-ended or dual-ended isolated topologies, such as push-pull, half-bridge and full-bridge converters. Figure 6 shows a simplified circuit of push-pull converter using the LT3710. The primary side controller is an LTC1922-1 synchronous phase modulated controller. The secondary side uses the LT1431, a programmable reference, to feed back the output signal and drive an opto-coupler. The secondary MOSFETs can be driven by an LTC1693-1, which contains two high speed dual N-channel MOSFET drivers. The LT3710 regulates the auxiliary output. Note that the LT3710 circuit works at twice the switching frequency of the main output push-pull converter because of the double-ended secondary structure. The higher switching frequency means the inductor L2 and output capacitor C2 can be smaller. Figure 7 shows a full bridge application with the LT3710.

Conclusion

The LT3710 is a high efficiency secondary side synchronous post regulator controller. It is designed to generate a tightly regulated auxiliary output in multiple output isolated power supplies. The LT3710 provides a simple, high efficiency and space saving post regulator solution, especially for low voltage/high current applications.

PowerPAK is a trademark of Vishay Siliconix

A 14-Bit ADC that is Both Fast and Low Noise

by Richard Reay and Dave Thomas

Introduction

The LTC1744 is an exception to the rule that an ADC must tradeoff low noise performance for high sampling rates. The LTC1744 is a 14-bit ADC that has excellent dynamics and linearity at sampling rates up to 50Msps, making it ideal for communications, scanners and high-speed data acquisition. Pin selectable input ranges of $2V_{P-P}$ and $3.2V_{P-P}$ along with a resistor programmable mode allow the LTC1744's input range to be optimized for a wide variety of applications. Its low jitter of 0.3ps allows undersampling of IF frequencies of up to 70MHz and beyond with excellent noise performance.

The LTC1743 is a pin compatible 12-bit part.

LTC1744 Features

- 50Msps sample rate
- 77dB SNR and 87dB SFDR at 5MHz input
- 150MHz full power bandwidth sampling
- $2V_{P-P}$ to $3.2V_{P-P}$ input range
- 0.5V to 5V digital output range
- 48-pin TSSOP package

Flexible, Yet Easy to Use

The LTC1744 is a complete solution with an on-chip sample and hold, a 14-bit pipelined ADC and a 30ppm programmable reference, as shown in block diagram in Figure 1. The wide-band sample and hold circuit can sample analog inputs beyond the Nyquist rate up to its 150MHz bandwidth. There is a low impedance, 2.5V reference output provided (V_{CM}) that can be used to set the common mode voltage of the analog inputs. The on-chip programmable reference can be set for a $2V_{P-P}$ or $3.2V_{P-P}$ input range, or any range in between by using two external resistors.

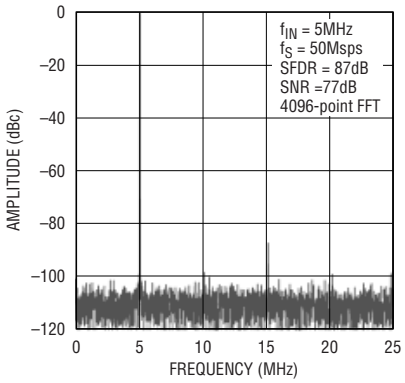


Figure 2. FFT with a 5MHz input signal

At 77dB SNR, the LTC1744 has the lowest noise of any ADC at this speed. The distortion performance of the LTC1744 is exceptional, with typical values of 87dB SFDR for a 5MHz input signal, and 73dB SFDR for a 70MHz input signal. Figure 2 shows a 4096-point FFT plot of the LTC1744 with a 5MHz input signal.

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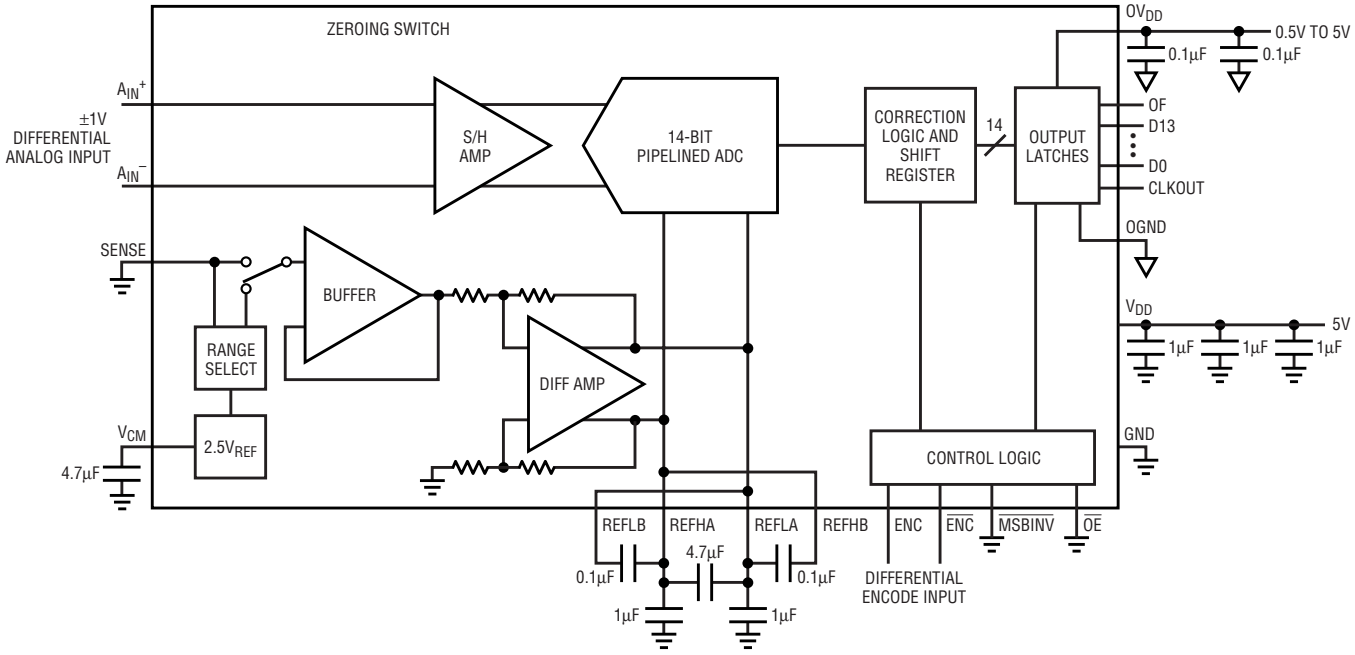
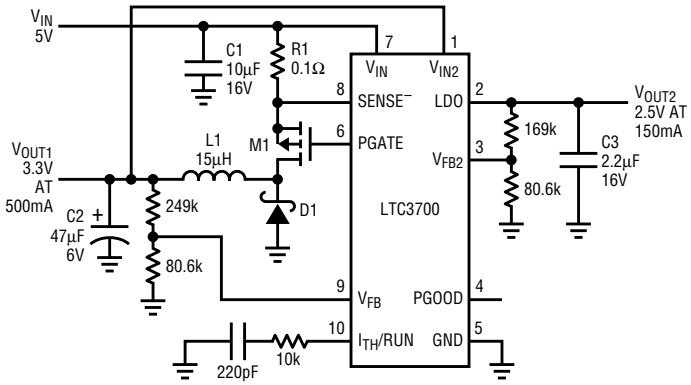


Figure 1. Block diagram

Replace Two ICs with a Combination High Efficiency Buck Controller Plus Low Noise LDO

by Mark Vitunic



C1: TAIYO YUDEN EMK325BJ106MNT (408) 573-4150
C2: SANYO POSCAP 6TPA47M (619) 661-6835
C3: MURATA GRM42-6X7R225K016AL (770) 436-1300
D1: MOTOROLA MBRS130LT3 (800) 441-2447
L1: COILTRONICS UP1B150 (561) 752-5000
M1: SILICONIX Si3443DV (800) 554-5565
R1: DALE 0.25W (605) 665-9301

Figure 1. 5V input to dual output: a 3.3V/500mA high efficiency output and a 2.5V/150mA low noise output

Need a second low-noise voltage output alongside your DC/DC converter, but don't have the room for another IC? The LTC3700 offers a simple solution by combining a constant frequency current mode step-down DC/DC controller with a 150mA low dropout (LDO) regulator in a tiny 10-pin MSOP.

The buck controller section of the LTC3700 offers many of the features expected in a high-performance switcher: high efficiency (up to 94%), wide V_{IN} range (2.65V to 9.8V), high constant frequency operation (550kHz), and current mode control for excellent AC and DC load and line regulation. The buck is configured for Burst Mode® operation, which reduces switching losses at light load, thereby enhancing efficiency. In dropout, the external P-channel MOSFET is turned on continuously (100% duty cycle), extending the usable voltage range of a battery source.

The LDO output is powered by an internal P-channel MOSFET pass device with an on resistance of approximately 1.5Ω (with V_{IN2} = 4.2V). The LDO has a separate input supply pin, which offers the versatility of powering the LDO from the buck regulator's input supply, its own independent input supply or the buck controller's output. The LDO is protected by both current limit and thermal shutdown circuits.

The LTC3700 provides ±2.5% output voltage accuracy for both the buck and LDO. The buck consumes only 210µA of quiescent current in normal operation with the LDO consuming an additional 50µA. In shutdown, a mere 10µA (combined) is consumed. A common "Power Good" output monitors both supplies.

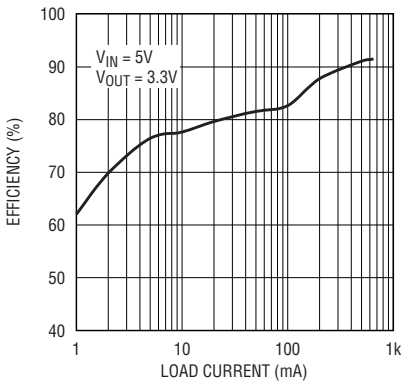


Figure 2. Efficiency of the 3.3V output for the circuit in Figure 1

5V Input Supply to 3.3V/500mA High Efficiency Output and 2.5V/150mA Low Noise Output

Figure 1 shows a dual regulated output voltage design running off of a single 5V input supply. The input to the LDO, V_{IN2}, could connect directly to V_{IN}, but better efficiency is obtained by running if off the 3.3V buck output.

Figure 2 shows the buck efficiency vs load current. Since the LDO's input supply is connected to the buck output, input current to the LDO adds to the load current seen by the buck. With both outputs running at maximum current, 500mA (buck) and 150mA (LDO) for 650mA total, the measured buck efficiency was 91.4%.

A Simple Solution to Low Noise, Isolated Power Conversion

by Tom Sheehan

Introduction

The LT3439 is a DC transformer driver tailored for applications that require an efficient, low noise isolated step-up or step-down power supply, such as noise sensitive medical instruments and precision measurement equipment. The LT3439 includes a proprietary technique for reducing conducted and radiated electromagnetic interference (EMI) that shortens the design cycle time and saves costs.

To maximize efficiency in power supplies, switch transitions are designed to occur as quickly as possible. Most EMI produced by a power supply is caused by the high speed slewing of currents and voltages. The result is input and output ripple that contains numerous harmonics of the switching frequency. Also, fast edges couple through circuit parasitics to nearby signal lines causing sensitive circuitry performance to be corrupted. Typically, mechanical shielding and careful layout is required to control the effects of EMI, but this can be an expensive and time consuming effort involving multiple PCB layout iterations.

The LT3439 gives the user the ability to reduce the EMI at the source of the noise. Switch current and voltage slew rates are programmable with a single resistor. Reducing the switch transition times can yield a large improvement in EMI with only a minor reduction in efficiency. Expensive shielding and filtering are not required and system performance is less sensitive to circuit layout. Also, the noise performance of the final system can be adjusted and tested by changing only one resistor.

Circuit Operation

The LT3439 DC transformer driver has two 1A internal switches which drive each end of a center tapped transformer. The two switches are turned on out of phase at 50% duty cycles. The input voltage is applied across the primary side of the transformer. The voltage on the secondary side is simply the input voltage times the turns ratio. Rectifiers on the secondary side generate the DC output voltage. The output capacitor is for hold up and filtering. If required, an additional inductor and capacitor can be added to reduce the output noise even further.

Control of the voltage and current slew rate is maintained via two control loops. One loop controls the output switch dV/dt and the other loop controls the output switch dI/dt. Output slew control is achieved by comparing the two currents generated by these slewing events to a current set by the external resistor R_{SL}.

The frequency of the internal oscillator can be set from 20kHz to 250kHz with an external resistor and capacitor, R_T and C_T. Each output switch is driven at half the frequency of the oscillator. The SYNC pin can be used to synchronize the switching to an external clock. A $\overline{SHDN}$ pin can be used to place the part into shutdown mode where the part draws less than

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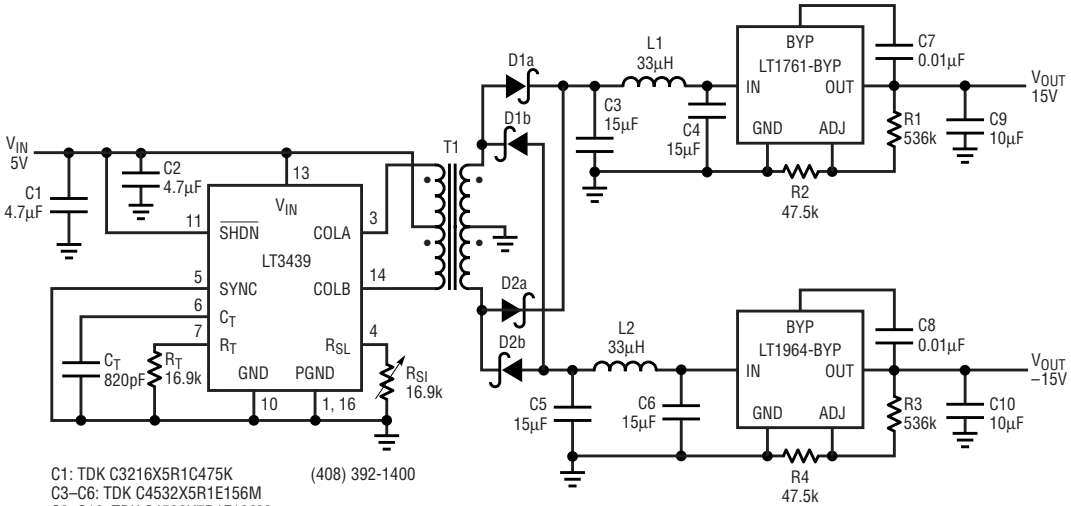

C1: TDK C3216X5R1C475K (408) 392-1400
C3–C6: TDK C4532X5R1E156M
C9, C10: TDK C4532X7R1E106M
D1, D2: ON SEMI BAS40 (602) 244-6600
T1: COILTRONICS CTX02-13664 (561) 752-5000
L1, L2: COILCRAFT DO1608C-333 (847) 639-6400

Figure 1. Dual output isolated step-up converter has well-controlled EMI

Bootstrapped Power Supply Permits Single Rail Amplifier Output Swing to Ground (and Below)

by Jim Williams

Many single supply powered applications require amplifier output swings within millivolt or even sub-millivolt levels of ground. Amplifier output saturation limitations normally preclude such operation. Figure 1's power supply bootstrapping scheme achieves the desired characteristics with minimal component addition.

A1, a chopper stabilized amplifier, has a clock output. This output switches Q1, providing drive to the diode-capacitor charge pump. The charge pump output feeds A1's V^- terminal, pulling it below zero, permitting output swing to (and below) ground. If desired, the negative output excursion can be limited by either clamp option shown.

Reliable start-up of this bootstrapped power supply scheme is a valid concern, warranting investigation. In Figure D2, the amplifier's V^- pin (Trace C) initially rises at supply turn-on (Trace A) but heads negative when amplifier clocking (Trace B) commences at about midscreen.

The circuit provides a simple way to obtain output swing to zero volts, permitting a true "live at zero" output.

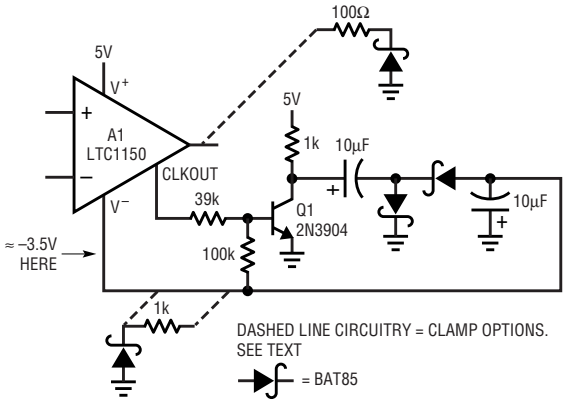

Figure 1. Single rail powered amplifier has true zero volt output swing. A1's clock output switches Q1, driving diode-capacitor charge pump. A1's V^- pin assumes negative voltage, permitting zero (and below) volt output swing.

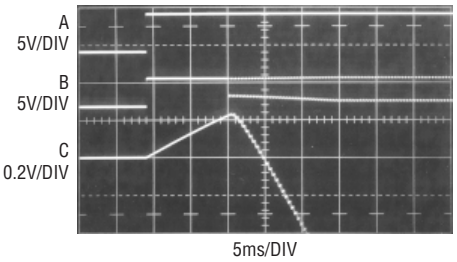

Figure 2. Amplifier bootstrapped supply start-up. Amplifier V^- pin (trace C) initially rises positive at 5V supply (trace A) turn-on. When amplifier internal clock starts (trace B, 5th vertical division), charge pump activates, pulling V^- pin negative.

LTC3439, continued from page 35

20µA. The $\overline{SHDN}$ pin can easily be configured to provide a supply undervoltage lockout (UVLO) function.

Protection features include current limiting, which facilitates startup into a high capacitance load; and cross conduction prevention circuitry, which keeps the two switches from being on simultaneously.

The LT3439 is available in a thermally enhanced 16-pin TSSOP with exposed underside metal.

Low Noise Step-up Converter Produces ±15V at 100mA from a 5V Input

Figure 1 shows a design that provides regulated ±15V at 100mA outputs from a 5V±5% input. Output ripple is less than 150µV or 0.001% of V_{OUT} measured at full load. Efficiency of the supply is approximately 71% measured at full load.

The LT1964-BYP and the LT1761-BYP linear regulators regulate the output to within 0.1% of nominal over the full line and load range.

Conclusion

The LT3439 DC Transformer Driver greatly simplifies the design of efficient low noise isolated power supplies. By reducing a major source of the EMI with voltage and current slew control, designs using the LT3439 avoid expensive shielding and filtering requirements and save the cost and time incurred by multiple iterative layouts.

For more information on parts featured in this issue, see http://www.linear.com/go/ltmag

New Device Cameos

Versatile Amplifiers and Comparators Now in Tiny Packages

Linear Technology is now producing a variety of its industry standard amplifiers and comparators in the tiny DFN package. The DFN package is a dual in-line, fine-pitch, lead-less package that measures only 3mm on a side and is only 0.8mm thick—it occupies the same amount of board space as a leaded SOT-23 but has eight connection pads for added functionality.

Some of the devices now available in a DFN include...

- micro-power, rail-to-rail amplifiers including the LT1490 and LT1638 dual, and the LT1636 and LT1637 single amplifiers. The new package, combined with the micropower operation, makes these parts easy to fit into handheld battery-powered applications.
- the versatile LTC1540/41/42 family of nanopower comparator, op amp and voltage reference combinations.
- precision devices that, in the new smaller package, can take advantage of proximity to the sensor to improve system performance. These include the precision, 3µV offset, zero-drift LTC2051 op amp and the low-noise, 1.9nV/√Hz, LT6203 dual amplifiers.
- 80MHz op amps: the rail-to-rail LT1801, the 200V/µs LT1813, and the 750V/µs LT1816 dual amps.
- the LT1396 dual current feedback amplifier for wideband applications and cable buffering.
- the high speed, 4.5ns propagation delay, LT1720 voltage comparator which can toggle at 70MHz.

Samples of these tiny DFN-packaged devices are provided on a carrier board for easy hook-up evaluation.

Authors can be contacted at (408) 432-1900

LTC4300-2 Provides Capacitance Buffering, Level Translation, and Data and Clock Hot Swapping 2-Wire Bus Systems

The LTC4300-2 allows I/O card insertion into a live backplane without corruption of the data and clock lines (SDA and SCL) for I²C™ and SMBus systems. In a typical application, the LTC4300-2 resides on the edge of a peripheral card where two of its pins, SDAOUT and SCLOUT, are connected respectively to the data and clock busses on the card. When the card is plugged into a live backplane two other pins, SDAIN and SCLIN, are connected to the data and clock busses on the backplane. Control circuitry provides a glitch-free connection by preventing the backplane busses from being connected to the card busses until data transactions on both sides are complete.

When the LTC4300-2's connection circuitry is activated, SDAIN is connected to SDAOUT, and SCLIN is connected to SCLOUT. Clock stretching, arbitration, synchronization, and data acknowledge always work, regardless of how devices in the system are tied to the LTC4300-2. Another key feature of the connection circuitry is that, while it links the backplane and card busses together, it still maintains electrical isolation between them, thus providing capacitance buffering for both sides.

The LTC4300-2 also features independent power supply inputs for the backplane and card, enabling level translation between 3.3V and 5V systems. Both the backplane and card may be powered with supply voltages ranging from 2.7V to 5.5V, with no constraints on which supply voltage is higher. Other features of the part include: rise time accelerator circuitry, which provides pull-up current during rising edges to help heavily loaded systems meet rise time requirements; the ability to disable the accelerator circuitry for lightly loaded systems; and pre-charge circuitry, which initializes the data and clock busses to 1V before card insertion in order to minimize the charge required by the LTC4300-2's parasitic capacitance. The LTC4300-2 is available in a small 8-pin MSOP package.

I²C is a trademark of Philips Electronics N.V.

LT1910 Provides Protected High-Side MOSFET Drive With Fault Status Indication

The LT1910 is a protected high-side MOSFET driver with a FAULT flag. High-side switching in hostile environments, such as industrial control, avionics and automotive applications, requires a rugged N-channel MOSFET driver. The LT1910 operates over a wide supply range of 8V to 48V and it can survive supply transients from –15V to 60V without damage.

The LT1910 has a charge pump that fully enhances an external N-channel MOSFET switch with no external components. By connecting a drain current sense resistor across a comparator, the LT1910 detects MOSFET current exceeding V_{SENSE}/R_{SENSE}. Upon overcurrent, the LT1910 immediately switches the MOSFET off and sets an open-collector FAULT status pin low. After a programmed time delay, the MOSFET is automatically restarted. The FAULT flag is reset only if the switch restarts successfully. Latch-off current limiting protection can also be implemented with the LT1910.

The LT1910 is specified over the –40° to 85° temperature range. It is available in an 8-lead plastic SO.

For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

LTC4210 Provides Active Current Limiting Protection with Circuit Breaker Timer

The LTC4210 is a positive Hot Swap™ controller with a fast current limit loop and a circuit breaker timer. The current limit loop protection allows each card in a bus cage be allocated with a fixed supply current budget. When a catastrophic board failure occurs, such as a component latching-up, the offending board robs current from the bus supply, the supply voltage drops and the adjacent cards reservoirs of capacitance dump current. This interaction can cause adjacent cards to reset and possibly cripple a high reliability system if the bad board's supply is not immediately limited.

The LTC4210 has a fast amplifier that monitors the voltage across an external R_{SENSE} resistor connected between the V_{CC} and SENSE pins. If a load surge causes the sense resistor voltage to exceed the circuit breaker trip voltage, V_{CB} of 50mV, the amplifier abruptly lowers the gate voltage to regulate the pass transistor. This limits the sense pin at V_{CB} and the load current is constant at 50mV/R_{SENSE}. The circuit breaker timer is activated during the current limiting period. An external C_{TIMER} capacitor connected between the TIMER pin to ground sets the timeout duration for circuit breaking. This timeout duration should be within the pass transistor safe-operating-area, SOA. At time-out, the pass transistor is shutdown with GATE pull to ground. After a brief load surge, the amplifier stops limiting and the charge pump pulls up the GATE with a 10µA current source.

A multi-mode timer sequences the LTC4210, with the duration set by C_{TIMER}. The initial timing cycle provides enough time for a solid connection to be made to the backplane and for the power supply to settle at the board plug-in. The ON pin of the LTC4210 must be taken high for the initial timing cycle to be activated. The start-up cycle begins after the initial timing cycle with the charge pump ramping up the GATE with a 10µA current source.

The LTC4210 operates from 2.7V to 16.5V and is available in low profile 6-pin ThinSOT™ package. It is specified for both commercial and industrial temperature ranges. This part is available in two configurations: the LTC4210-1 for automatic retry on an overcurrent fault and the LTC4210-2 for latch-off on an overcurrent fault.

LTC1744, continued from page 33

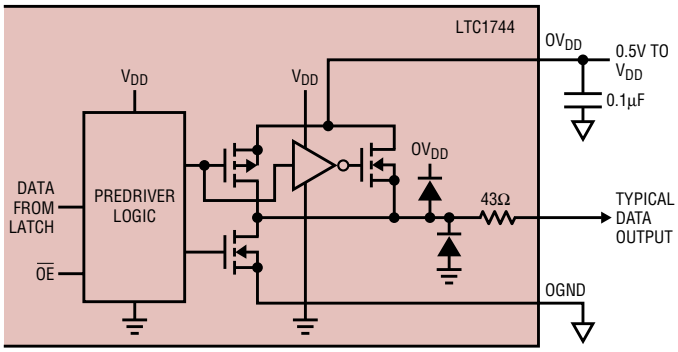

Figure 3. Equivalent circuit for a digital output buffer

Programmable On-Chip Reference

When using high-speed ADCs, there is a tradeoff between using a small input range for clean distortion performance and a larger input range for low noise. The LTC1744 gives the user the flexibility to choose the optimal input range for the application. There are two built-in input ranges that can be selected using the SENSE pin. With SENSE tied to V_{DD}, the input range is $3.2V_{P-P}$, and with SENSE tied to GND, the input range is $2V_{P-P}$. If another input range is desired, SENSE can be driven with an external reference or by a resistor divider from the on-chip 2.5V reference to generate any input range between $2V_{P-P}$ and $3.2V_{P-P}$.

Easy Interface to 5V, 3V or LVDS Systems

The LTC1744 offers flexible digital output range making it versatile and easy to use. Figure 3 shows an equivalent circuit for one of the digital output buffers. Each buffer is powered by the OV_{DD} and OGND pins, which are isolated from the ADC power and ground. The OV_{DD} supply can be set from 0.5 to 5V, allowing direct interface to any CMOS logic family, TTL or LVDS. In high speed ADCs, coupling from the digital outputs to the analog input can degrade the noise performance. Reducing the output swing minimizes this effect.

Conclusion

The LTC1744 is a flexible 14-bit 50Msps ADC that offers industry-leading low noise performance and features that make it both versatile and easy-to-use.

For more information on parts featured in this issue, see http://www.linear.com/go/ltmag

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