LINEAR TECHNOLOGY

IN THIS ISSUE...

Photoflash Capacitor Chargers Fit into Tight Spots

by Albert Wu

Introduction

Take a walk through any electronics retailer and you will notice an obvious trend: Cameras are being added to PDAs, cell phones and other portable devices. This is due, of course, to shrinking electronics required for digital imaging. Even as imaging electronics shrink, the imaging pixel count grows. The corresponding increase in image quality demands a corresponding improvement in photoflash technology. LED-based photoflash units are certainly compact enough to fit in the smallest devices, but LED units cannot meet the light output and spectral quality required of one megapixel or higher sensors. A xenon-bulb based flash unit offers better performance, but traditionally takes more space. Now there is a way to fit a xenon-bulb photoflash unit into the tightest spaces. The solution is to use one of Linear Technology's LT®3468 photoflash capacitor chargers.

The LT3468 series is available in a 5-Lead ThinSOT™ package. All output voltage detection is implemented inside the part, substantially reducing external parts count to a mere four components. A new patented control technique allows the use of ultra-small transformers while maintaining high efficiency. Imaging devices using these parts can save significant space while still achieving well controlled battery current, fast charge times and high efficiency.

Overview

A typical application for the LT3468 is shown in Figure 1a. The high level of

DANGER HIGH VOLTAGE—OPERATION BY HIGH VOLTAGE TRAINED PERSONNEL ONLY

C1: 4.7µF, X5R OR X7R, 10V
T1: TDK PART# LDT565630T-001, L_{PRI} = 6µH, N = 10.4
D1: VISHAY GSD2004S DUAL DIODE CONNECTED IN SERIES
D2: ZETEX ZHCS400 OR EQUIVALENT
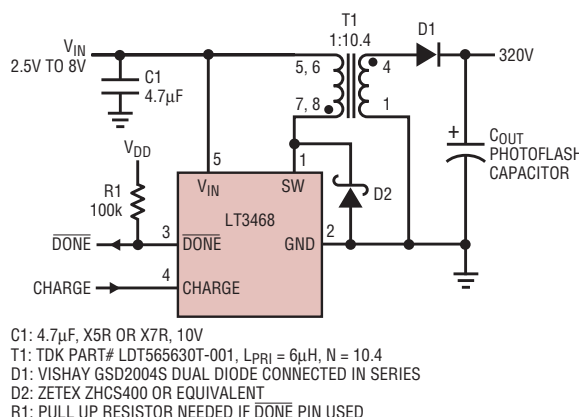R1: PULL UP RESISTOR NEEDED IF $\overline{DONE}$ PIN USED

Figure 1a. Compact, 320V photoflash capacitor charging circuit needs no zener

Issue Highlights

This issue's cover article presents the new LT3468 and LT3468-1, two **photoflash capacitor chargers** that make it possible to fit a xenon-bulb photoflash unit into the tightest spots. Until now, the smallest digital imaging devices, like those found in cell phones and PDAs had to make due with relatively low-performance LED-type flash units.

Featured Devices

Below is a summary of the other devices featured in this issue.

Power over Ethernet

This magazine recently ran a three-part series of articles about **Power over Ethernet (PoE)**. At the time, the PoE standard (IEEE 802.3af) had not yet been finalized, but it is now. The follow-up article in this issue ties up some of the loose ends left by the then not-yet-finalized 802.3af standard, and discusses the *power off* part of the standard in more detail. (Page 17)

Programmable Oscillators

The LTC®6903 and LTC6904 are **programmable oscillators** that provide a smaller, more reliable and vastly more versatile clocking solution than the venerable crystal oscillator. In a small MS8 package, the LTC6903 and LTC6904 use less board space than almost all crystal oscillators. (Page 7)

Power Supply Regulators and Controllers

The LTC3407 is a tiny, 10-lead, **dual, synchronous, step-down, current mode, DC/DC regulator** intended for low power applications. It operates within a 2.5V to 5.5V input voltage range and has a fixed 1.5MHz switching frequency, making it possible to use tiny capacitors and inductors that are under 1.2mm in height. (Page 19)

The LTC3205 **multi-display LED controller** improves efficiency in Li-Ion powered devices by powering up in *direct-connect* mode rather than step up mode. The LTC3205 has enough LED pins and sufficient strength to power a 4-LED main display, a 2-LED sub display and a 3-LED RED, GREEN and BLUE "happy-light." (Page 22)

The LT3433 **high-voltage monolithic DC/DC converter** incorporates two switch elements, allowing for a unique topology that accommodates both step-down and step-up conversion using a single inductor. The LT3433 is primarily intended for use in step-down applications that have transient low voltage input requirements, such as 12V automotive applications that must support a cold-crank condition, where the battery-rail can briefly drop down to 4V. (Page 24)

Hot Swap, Hot Plug, Power Supply Monitoring and Margining

A fundamental problem plaguing most power supply supervisory ICs is the inability to establish the correct logic state at the reset node with low input supply voltages. The LTC2903 **precision quad supply monitor** virtually eliminates this floating reset node problem. (Page 14)

The LTC4212 is a **Hot Swap controller** that allows safe board insertion and removal from a live backplane. It features a supply range of 2.5V to 16.5V, programmable soft-start with inrush current limiting, automatic retry or latched mode operation, a high side drive for an external N-channel MOSFET and dual level overcurrent fault protection. The LTC4212 can monitor any number of supplies on the board. (Page 10)

The LT4220 **dual supply Hot Swap controller** operates over any combination of split supplies ranging from ±2.7V to ±16.5V. It allows a circuit board to be safely inserted or removed from a live backplane without glitching the power supplies while controlling load currents from milliamps to amps. The LT4220 also coordinates voltage tracking of the split supplies. (Page 28)

The LTC2920-1 is a **power supply margining controller** packaged in a 5-lead SOT23. The LTC2920-2 is a dual power supply margining controller packaged in an 8-lead MSOP. Both parts provide easy and accurate way to accomplish on-board power supply margining with a minimum of design time and board space. (Page 31)

Design Ideas and Cameos

Starting on page 33 are three new Design Ideas, and at the back are four New Device Cameos. Visit www.linear.com for complete device specifications and applications information. *LT*

Figure 1b. Charge times

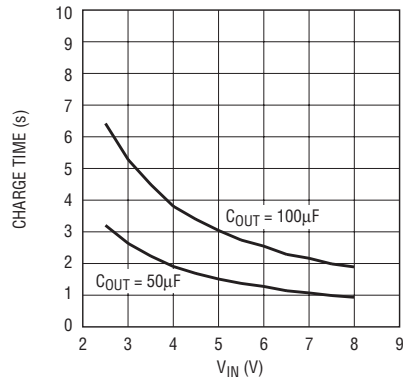**Figure 1c. The LT3468 makes it possible to fit an entire photoflash charging circuit into 80mm²**

integration inside the part results in a very simple circuit that takes little valuable board space. Figure 1c shows an entire charging circuit fitting into 80mm². The tallest component on

the board is the transformer, which is only 3mm in height. Despite the tiny components, charge time is excellent due to the high power, integrated low resistance NPN power switch.
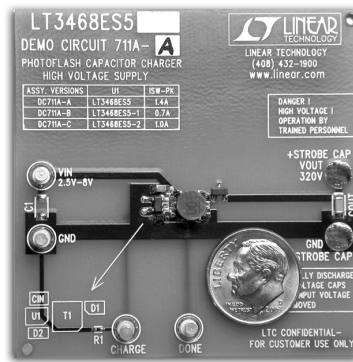
The LT3468-1 is a lower current version of the LT3468. Figure 2a shows a typical application circuit while Figure 2b shows the charge time. The input current for the LT3468-1 is typically 250mA, while that of the LT3468 is about 550mA.

Operation

To better understand the operation of the part, refer to Figure 3 for the following overview. Note that the only difference between the LT3468 and the LT3468-1 is the switch current limit (1.4A for the LT3468, 0.7A for the LT3468-1). A low-to-high transition on the CHARGE pin initiates the part. An edge triggered one-shot triggered by the CHARGE pin puts the various latches inside the part into the proper state.

DANGER HIGH VOLTAGE—OPERATION BY HIGH VOLTAGE TRAINED PERSONNEL ONLY

C1: 4.7µF, X5R OR X7R, 10V
T1: TDK PART# LDT565630T-002, L_{PRI} = 14.5µH, N = 10.2
D1: VISHAY GSD2004S DUAL DIODE CONNECTED IN SERIES
D2: ZETEX ZHCS400 OR EQUIVALENT
R1: PULL UP RESISTOR NEEDED IF $\overline{DONE}$ PIN USED
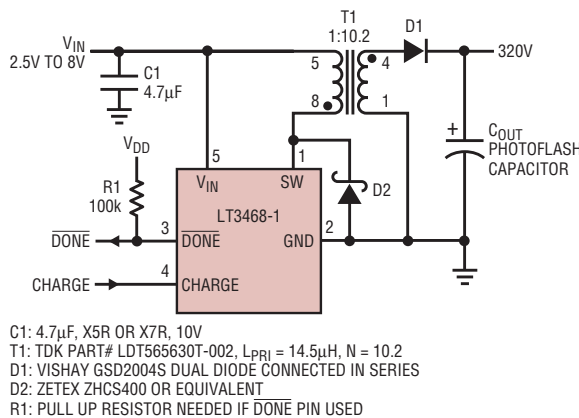
Figure 2a. LT3468-1 photoflash circuit uses tiny 3mm tall transformer

Figure 2b. Charge time

	LT3468	LT3468-1	LT3420	LT3420-1
Peak SW Current (A)	1.4	0.7	1.4	1.0
Secondary Current at SW Turn On (mA)	0		40	20
Average Input Current (mA) (V_{IN} = 3.3V, V_{OUT} = 300V)	550	250	840	500
Minimum Battery Voltage (V)	2.5		1.8	
Integrated Output Detection?	Yes		No	
Automatic Refresh?	No		Yes	
Common Battery Combinations	1–2 Li-ion cell 4 AA cells 4 NIMH cells		1–2 Li-ion cell 2–4 AA cells 2–4 NIMH cells	
Package	TSOT-5L		MSOP-10L	
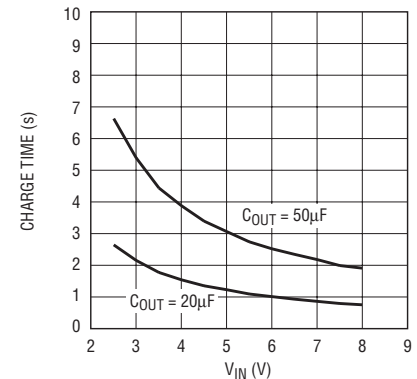
Table 1. Comparison chart for Linear Technology's photoflash charger parts
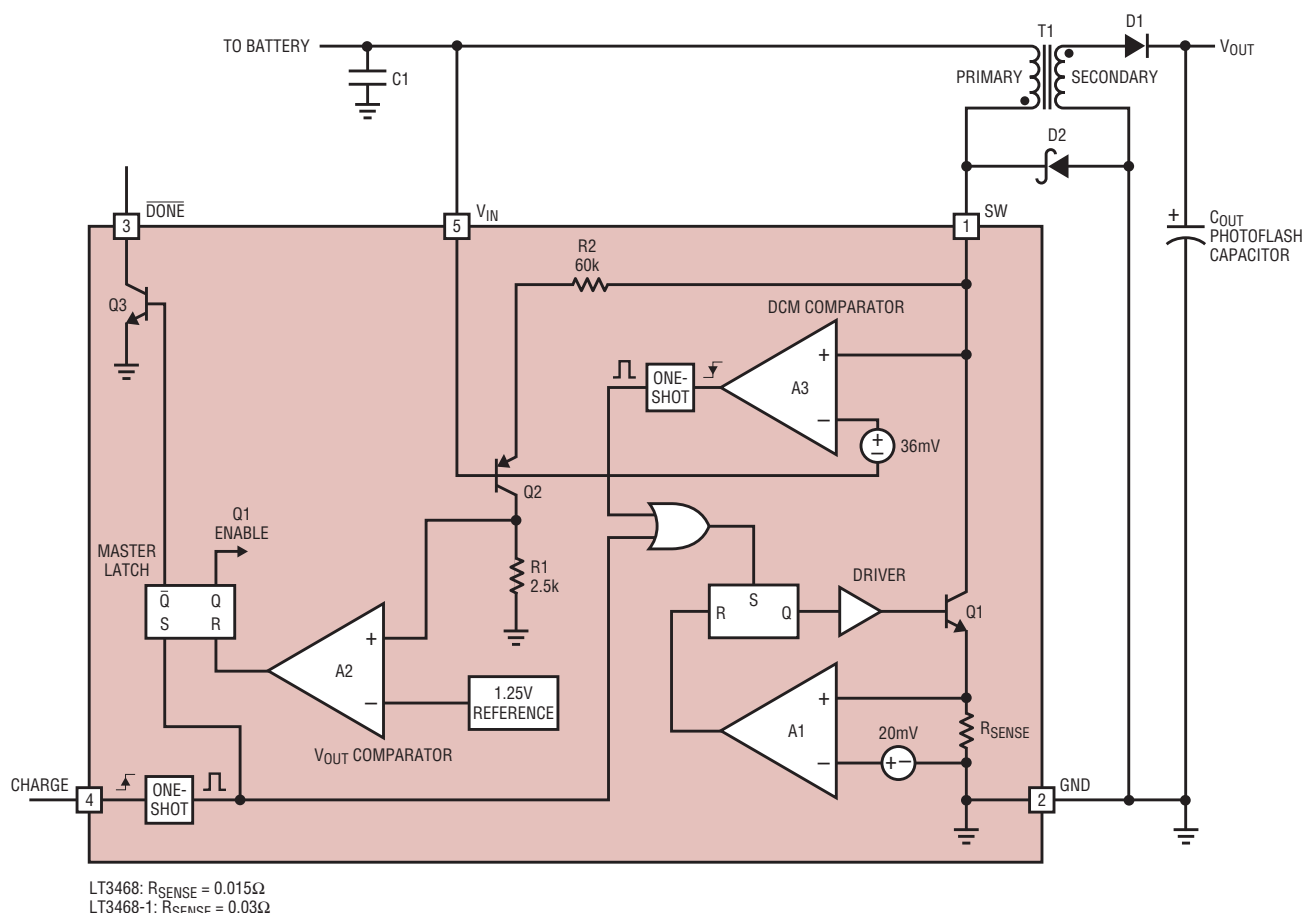
Figure 3. Block diagram of the LT3468

LT3468: R_{SENSE} = 0.015Ω
LT3468-1: R_{SENSE} = 0.03Ω

The part begins charging by turning on the power NPN transistor Q1. With Q1 on, the current in the primary of the flyback transformer increases. When it reaches the current limit, Q1 is turned off and the secondary of the transformer delivers current to the photoflash capacitor via diode D1. During this time, the voltage on the SW pin is proportional to the output voltage. Since the SW pin is higher than V_{IN} by an amount roughly equal to (V_{OUT} + 2 • V_D)/N, the output of the DCM Comparator is high. In this equation, V_{OUT} is the photoflash capacitor voltage, V_D is the rectifying diode forward drop, and N is the turns ratio of the transformer.

Once the current in the secondary of the transformer decays to zero, the voltage on the SW pin collapses to V_{IN}, or lower. As a result, the output of the DCM comparator goes low, which triggers the one-shot. This leads to Q1 turning on again and the cycle repeats.

Output voltage detection is accom-

Figure 4a. LT3468 switching waveform at 100V output

Figure 4b. LT3468 switching waveform at 300V output

Figure 4c. LT3468-1 switching waveform at 100V output

Figure 4d. LT3468-1 switching waveform at 300V output

plished via comparator A2. When the SW pin is 31.5V higher than V_{IN} on any cycle, the output of A2 goes high. This resets the master latch and the part stops delivering power to the photoflash capacitor. Power delivery can only restart by taking the CHARGE pin low and then high.
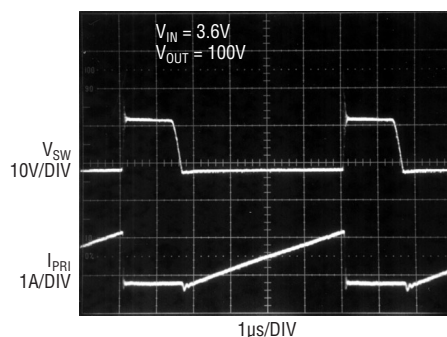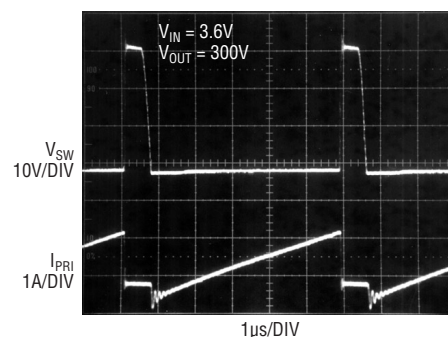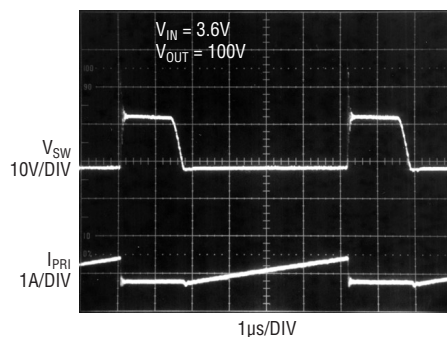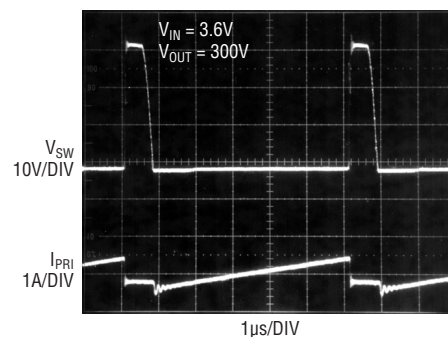
Note that the flux in the flyback transformer is brought to zero on each switching cycle. This is generally referred to as boundary mode since the transformer is operated in between continuous conduction mode and discontinuous conduction mode (CCM and DCM respectively). When the CHARGE pin is forced low at anytime, the LT3468 ceases power delivery and goes into shutdown mode, thus reducing quiescent current to less than 1µA. Figure 4 shows some typical switching waveforms for the LT3468 and LT3468-1.

Which Part to Use?

The LT3468 and LT3468-1 round out Linear Technology's photoflash capacitor charger line to four chargers that can suit just about any photoflash need: the LT3468, LT3468-1, LT3420, and the LT3420-1. Table 1 shows the major functional differences between these four parts.

Choosing a device is a matter of balancing the inherent trade-off between average input current and charge time.

For a given photoflash capacitor size, the device which results in the highest average input current offers the fastest charge time. The limit on how much current the photoflash charger can draw is usually set by the batteries, and how much load they can handle. The LT3420 offers the fastest charge times of the chargers discussed here.

The following equations predict the charge times (T) in seconds for the four parts:

LT3468:

$$T = \frac{C_{OUT} \cdot \left(V_{OUT(FINAL)}^2 - V_{OUT(INIT)}^2 \right)}{0.65 \cdot V_{IN}},$$

LT3468-1:

$$T = \frac{C_{OUT} \cdot \left(V_{OUT(FINAL)}^2 - V_{OUT(INIT)}^2 \right)}{0.32 \cdot V_{IN}},$$

LT3420:

$$T = \frac{C_{OUT} \cdot \left(V_{OUT(FINAL)}^2 - V_{OUT(INIT)}^2 \right)}{1.2 \cdot V_{IN}},$$

LT3420-1:

$$T = \frac{C_{OUT} \cdot \left(V_{OUT(FINAL)}^2 - V_{OUT(INIT)}^2 \right)}{0.55 \cdot V_{IN}},$$

where C_{OUT} is the value of the photoflash capacitor in Farads, $V_{OUT\text{-}FINAL}$ is the target output voltage, $V_{OUT\text{-}INIT}$ is

the initial output voltage, and V_{IN} is the battery or input voltage to which the flyback transformer is connected.

These equations are developed for specific transformers, namely the TDK LDT565630T-001 for the LT3468, the TDK LDT565630T-002 for the LT3468-1, the TDK SRW10EPC-U01H003 for the LT3420 and the Kijima Musen SBL-5.6S-2 for the LT3420-1. If other transformers are used, the constant in the denominator of each the above equations changes slightly because of differing transformer efficiencies.

Generally speaking, the LT3468 is used for photoflash capacitors in the 80µF to 160µF range commonly found in mid- to high-end digital cameras. The LT3468-1 is used for photoflash capacitors in the 10µF–80µF range, which are likely to be required in ultra small digital cameras and cell phone-based cameras. For designs required to operate from 2AA cells, the LT3420 and LT3420-1 are the right choice, as they are designed to operate on a battery voltage down to 1.8V.

Output Voltage Detection

A major benefit of the LT3468 and LT3468-1 is the complete integration of output voltage detection inside the part. The output voltage is sensed via the flyback transformer as described in the operation section above. The

For Use With	Transformer Name	Size (mm) (W × L × H)	L_{PRI} (µH)	L_{PRI}-Leakage (nH)	N	R_{PRI} (mΩ)	R_{SEC} (Ω)	Vendor
LT3468 LT3468-1	SBL-5.6-1 SBL-5.6S-1	5.6 × 8.5 × 4.0 5.6 × 8.5 × 3.0	10 24	200 Max 400 Max	10.2 10.2	103 305	26 55	Kijima Musen Hong Kong Office 852-2489-8266 (ph) kijimahk@netvigator.com (email)
LT3468 LT3468-1	LDT565630T-001 LDT565630T-002	5.8 × 5.8 × 3.0 5.8 × 5.8 × 3.0	6 14.5	200 Max 500 Max	10.4 10.2	100 Max 240 Max	10 Max 16.5 Max	TDK Chicago Sales Office (847) 803-6100 (ph) www.components.tdk.com
LT3468/LT3468-1 LT3468-1	T-15-089 T-15-083	6.4 × 7.7 × 4.0 8.0 × 8.9 × 2.0	12 20	400 Max 500 Max	10.2 10.26	211 Max 75 Max	27 Max 35 Max	Tokyo Coil Engineering Japan Office 0426-56-6336(ph) www.tokyo-coil.co.jp

Table 2. Pre-designed transformers and typical specifications (unless otherwise noted)

Table 3a. Performance comparison of LT3468 and two microprocessor-controlled photoflash charging units from actual digital cameras

	LT3468	µP-Controlled Flyback #1	µP-Controlled Flyback #2
Charge Time (seconds) (V_{IN} = 3V, V_{OUT} charged from 50V to 320V, 120µF photoflash capacitor)	6.3	13.6	7.5
Average Input Current (mA)	500	430	750

Table 3b. Normalized performance comparison of LT3468 and two microprocessor-controlled photoflash charging units from actual digital cameras

	LT3468	µP-Controlled Flyback #1	µP-Controlled Flyback #2
Normalized Charge Time (seconds) (V_{IN} = 3V, V_{OUT} charged from 50V to 320V, 120µF photoflash capacitor)	6.3	11.7	11.2
Average Input Current (mA) Normalized to 500mA	500		

output voltage is thus set by the turns ratio, N, of the transformer. Choose N with the following equation:

$$N = (V_{OUT} + 2)/31.5,$$ where V_{OUT} is the desired output voltage.

Because most of the output detection circuitry, other than the transformer, is integrated inside the IC, the accuracy of the output detection can be very good. The 31.5V comparator voltage is precision trimmed and is specified at ±1.6% over the full operating temperature range. To find the worst case deviation on the output voltage, simply add this deviation to the worst case deviation in the turns ratio N of the transformer. Typical guaranteed deviations of N are in the 2%–3% range, although there is likely much room for improvement here. Consult your transformer vendor for more information. Figure 5 shows a histogram of the V_{OUT} distribution for a sample (~100 units) of LT3468 prototype boards. As you can see, the distribution is tight in a range of ±5V, which is equivalent to a tolerance under ±1.5%

Pre-Designed Transformers

Linear Technology Corporation has worked with several transformer manufacturers to produce transformer designs that are optimized for the LT3468 and LT3468-1. In most applications, these transformers, shown in Table 2, will suffice. Of particular interest are the ultra small transformers now available—as small as 5.8mm × 5.8mm × 3.0mm—which still achieve excellent efficiency and charge time.

Comparison of the LT3468 and LT3468-1 to Discrete Photoflash Chargers

There are numerous benefits to using the LT3468 series of parts—best seen when the LT3468 series is compared to the current method used by many digital camera manufacturers. Figure 6 shows a typical microprocessor-controlled flyback photoflash capacitor charger. Due to cost and microprocessor limitations, no sensing of primary current is done. In this case, only the output voltage is sensed in order to halt charging at the appropriate time. The microprocessor must control the gate of the NFET with appropriate ON and OFF times. The OFF times must be large enough so that the current in the primary of the transformer always stays in control. Since no direct sensing of the current is used, the OFF time must be conservative so that the flux in the transformer is always reset to zero each cycle. Thus, the flyback converter is operated heavily in the discontinuous mode region. This has several unwelcome consequences, including high peak currents in the primary of the transformer and the discrete NFET. The high peak currents are difficult to filter out and cause volt-
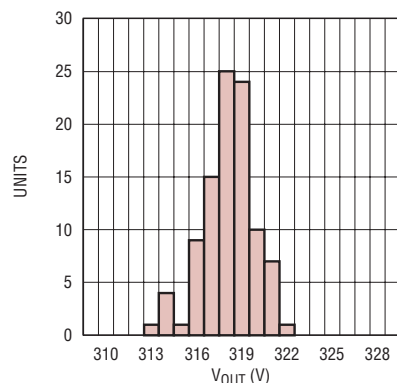

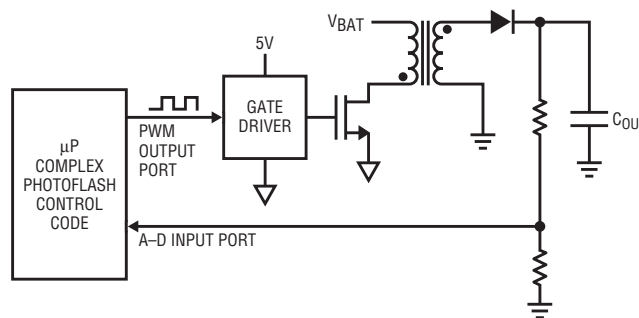Figure 5. Output voltage histogram of ~100 LT3468 prototype boards.

Figure 6. Typical microprocessor-controlled flyback photoflash capacitor charger. Due to cost and microprocessor limitations, no sensing of primary current is done—only the output voltage is sensed in order to halt charging at the appropriate time.

Digital Programmable Oscillator Is Smaller, Sturdier and More Versatile than Crystal Oscillators

by Albert Huntington

Introduction

Open just about any electronic gadget these days, and you will find a crystal oscillator driving a microcontroller, providing a timebase or clocking any number of discrete time circuits. Crystal oscillators provide a reasonably priced, and highly stable time base. They are relatively easy to use, and are available in increasingly smaller packages. Thus, the venerable crystal oscillator has become the defacto timebase solution. Designers often do not even consider asking if it is the best solution to a problem, when, in fact, crystal oscillators are not without their drawbacks. They can be power hungry, inflexible, board space hogging, and above all, *shock sensitive* components.

Enter the LTC6903 and LTC6904. These programmable oscillators provide a smaller, more reliable and vastly more versatile clocking solution. In a small MS8 package, the LTC6903 and LTC6904 use less board space than almost all crystal oscillators. Whereas crystal oscillators contain a quartz crystal and are sensitive to mechanical shock, the LTC6903 and LTC6904 are a fully electronic devices, and relatively insensitive to vibration and mechanical shock. While crystal oscillators output a set frequency, the LTC6903 and LTC6904 are fully programmable between 1kHz and 68MHz. The frequency is set by a 16-bit control word via a serial port and is typically accurate to within 1.1%, with a resolution of 0.1% or better.

Device Description

The LTC6903 and LTC6904 are resistor controlled oscillators, similar to the popular LTC1799. These new oscillators offer an integrated serial resistor DAC and a set of digital frequency dividers, as shown in Figure 1.

The LTC6903 takes commands via an SPI-compatible 3-wire serial port, and the LTC6904 communicates through an I^2C-compatible 2-wire serial port. The serial port bit maps are shown in Figure 2. Ten DAC bits control the resistor DAC, four OCT bits control the output dividers, and 2 MODE bits control the outputs. The LTC6904 can respond to one of two different serial port addresses (set by the state its ADR pin).

The resistor DAC ranges linearly in value from R to 2R, where R is trimmed to give the oscillator a frequency range of 34MHz to 68MHz:

$$f = \frac{68\text{MHz} \bullet R}{R_{DAC}}, \text{ where } R \leq R_{DAC} \leq 2R$$

The oscillator frequency is inversely proportional to the resistance of the DAC. At frequencies just above 34MHz, the step size is 16.6kHz. At frequencies immediately below 68MHz, the step size is 66.4kHz. The step size ranges between 0.05% and 0.1% of the frequency. The output frequency divider divides the internal oscillator frequency by 2^N, where N ranges from 0 to 15. N is calculated from the OCT bits of the control word, and is simply the complement of those bits. Higher values of N (lower values of OCT) yield lower output frequencies. The combination of the OCT and DAC bits into a single 14-bit control word provides a simple and consistent interface where higher control codes always result in
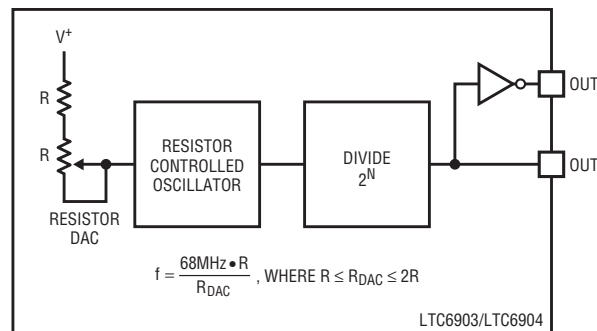
Figure 1. LTC6903 and LTC6904 conceptual block diagram. The LTC6903 and LTC6904 consist of a resistor controlled oscillator coupled to a serial port controlled resistor DAC and output divider.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
OCT3	OCT2	OCT1	OCT0	DAC9	DAC8	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0	MODE1	MODE0
4-Bit Control Divider 2^N				10-Bit Control DAC										2-Bit Control OUT and $\overline{\text{OUT}}$	

Figure 2. LTC6903 and LTC6904 serial port bitmap. OCT[3:0] controls the octave, DAC[9:0] controls the frequency setting within an octave, and MODE[1:0] sets the active output.

Table 1. Choosing the OCT code

Minimum Frequency	Maximum Frequency	OCT Code
34.05MHz	68.03MHz	15
17.02MHz	34.01MHz	14
8.511MHz	17.01MHz	13
4.256MHz	8.503MHz	12
2.128MHz	4.252MHz	11
1.064MHz	2.126MHz	10
532kHz	1063kHz	9
266kHz	531.4kHz	8
133kHz	265.7kHz	7
66.5kHz	132.9kHz	6
33.25kHz	66.43kHz	5
16.62kHz	33.22kHz	4
8.312kHz	16.61kHz	3
4.156kHz	8.304kHz	2
2.078kHz	4.152kHz	1
1.039kHz	2.076kHz	0

higher frequencies. Across all control codes, the LTC6903/LTC6904 is guaranteed to be completely monotonic.

The output pins are controlled by the output control bits MODE1 and MODE0. Either of the outputs can be disabled through these bits. When both outputs are disabled through the mode control bits, the internal oscillator is also disabled. The OE pin can also be used to asynchronously disable either output without shutting down the oscillator entirely.
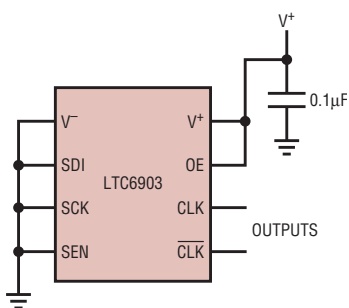

Figure 3. LTC6903 minimal circuit. The LTC6903 and LTC6904 have a simple external interface—the only required external component is a bypass capacitor.

Applications Example

A Minimal Circuit

The LTC6903 and LTC6904 require no external components other than a small power supply bypass capacitor. For best performance, this capacitor should have low series resistance and be mounted directly adjacent to the power supply pins. The minimal circuit shown in Figure 3 results in an oscillator frequency of 1.039kHz upon power-up. The LTC6903/LTC6904 incorporates power on reset circuitry which sets the control code to all zeros when power is first applied. Other frequencies may be set through the serial port.

Calculating the Frequency Code

In order to set a frequency, an OCT code and a DAC code must be calculated. The OCT code may be chosen from Table 1 or it may be calculated as:

$$OCT = 3.322 \log \frac{f}{1039}, \qquad (1)$$

where f is the desired frequency in Hertz.

When using the equation, it is necessary to round the OCT code *down* (truncate) to the nearest integer.

The DAC code is:

$$DAC = 2048 - \frac{2078(Hz) \cdot 2^{10+OCT}}{f},$$

where f is the desired frequency in Hertz and OCT is the previously determined OCT code.

Round the DAC code to the nearest integer value, up or down. The frequency may be calculated from the OCT and DAC settings through the formula:

$$f = 2^{OCT} \cdot \frac{2078}{\left(2 - \dfrac{DAC}{1024}\right)} \qquad (2)$$

For instance, to set a frequency of 1.00MHz, first chose the OCT code from Table 1 or calculate OCT from equation [1] above.

$$OCT = 3.322 \log \frac{1 \cdot 10^6}{1039} = 9.91$$

Round down (truncate) for an OCT code of 9. Next, calculate the DAC code:

$$DAC = 2048 - \frac{2078(Hz) \cdot 2^{10+9}}{1 \cdot 10^6} = 958.53$$

Rounding to the nearest integer, the DAC code is 959.

Verify the calculations by plugging the result back into the formula [2] for frequency:

$$f = 2^9 \cdot \frac{2078}{\left(2 - \dfrac{959}{1024}\right)} = 1.00 \times 10^6$$

In order to determine the 16-bit control word for the LTC6903/LTC6904, values for the mode control bits, MODE0 and MODE1, must be chosen. To enable both outputs, set both MODE0 and MODE1 to "0".

The control word is composed of the OCT, DAC and MODE control bits:

$OCT \cdot 2^{12} + DAC \cdot 2^2 + MODE,$

or,

$9 \cdot 2^{12} + 959 \cdot 2^2 + 0 = 40,700,$

or in binary,

1001111011111100.

Figure 4 shows that frequency resolution over the entire range of the control word is roughly proportional to the set frequency.

Writing the Control Code

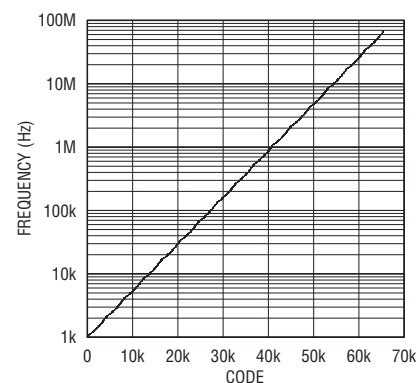The LTC6903 can be configured through its SPI-compatible serial port. Similarly, the LTC6904 can be

Figure 4. Frequency vs control code. The LTC6903 and LTC6904 achieve 0.1% resolution across all specified frequencies with a smooth, monotonic transfer function.

OCT = 9				DAC = 959										MODE=0	
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	1	1	1	0	1	1	1	1	1	1	0	0

Figure 5. Setting the frequency to 1MHz and choosing a mode after calculating OCT and DIV codes. The codes must be translated into a binary number and written to the LTC6903 or LTC6904 through its serial port.

addressed through its I²C-compatible 2-wire serial port. Both serial ports are set up so that the serial transfer is accomplished in 8-bit chunks, the MSB being transferred first. Therefore, writing just a single byte to the serial port will result in the most significant byte being changed. Additionally, the bytes are written to the registers as they are received, so a pause between writing the first and second bytes may temporarily result in an unintended frequency output.

Driving Loads

The LTC6903 and LTC6904 output drivers present a low output impedance of 45Ω, and are capable of driving substantial resistive and capacitive loads of as much as 1kΩ and 100pF at frequencies up to 1MHz. At higher frequencies, two effects must be taken into account. First, the impedance presented by the capacitive load becomes a substantial factor in the shape of the output waveform. At the maximum operating frequency of 68MHz, in order to achieve full swing, an output load of 5pF or less is recommended. Second, the current drawn through the output drivers at high frequencies becomes excessive with capacitive loads. This results in greatly increased power

dissipation, and will contribute to frequency inaccuracy at frequencies above about 1MHz. Under a 5V power supply, the output drivers each draw 1.7mA at 68MHz for every 5pF of load. This is simply a calculation of the energy necessary to charge and discharge the output load capacitance to 5V at 68MHz, following the formula:

$$I_S = C_{LOAD} \bullet V_{SUPPLY} \bullet F_{CLK}$$

The recommended 5pF load is equivalent to two HC CMOS logic inputs, and is substantially less than the 12pF–15pF of a standard oscilloscope probe. It is also recommended that the connection to the output of the LTC6903/LTC6904 be kept shorter than 5cm in order to reduce ringing and reflections from transmission line effects.

Jitter

Crystal oscillators traditionally excel in frequency accuracy with low jitter. The LTC6903 and LTC6904 do not reach the level of a crystal oscillator by those measures, but it is comparable enough to make it a good choice in most applications, especially when size, cost and durability are important.

Frequency accuracy is trimmed in at <0.75% at 1kHz under nominal power

supply and temperature conditions. DAC variation over frequency settings adds an additional 0.35%, while temperature variation across 0°C–70°C adds 0.9%, for a total variation of 2% over temperature and setting. Power supply variations, mostly at the upper end of the supply range, account for an additional 0.25% inaccuracy, leading to 2.25% over all conditions.

Due to the large number of dividers used when operating at low frequencies, the LTC6903 is able to provide typical peak-to-peak jitter of less than 0.1% at frequencies up to 500kHz, and less than 0.4% at frequencies up to 8.5MHz. At 68MHz, jitter increases to just under 3% because the averaging effects of the dividers are absent. These specs are acceptable in all but the most demanding precision timing applications.

A Tunable Lowpass Filter

The LTC6903 and LTC6904 are uniquely well suited to interface with switched capacitor devices such as filters and data converters. The tunable lowpass filter of Figure 6 is a typical example. Using the LTC6903 in combination with an LTC1569-7 tunable filter, it is possible to generate a lowpass frequency response anywhere from 94Hz to 300kHz with a 0.1% resolution, using a circuit consisting of only two small integrated circuits and no external components other than two 10% resistors and power supply bypass capacitors.

By tuning the LTC6903 over a frequency range of 3kHz to 9.5MHz at 5V power supply using the equations presented earlier, a corner frequency of between 94Hz and 300kHz may be set. The current draw of the combined circuits is typically 10mA, the majority of which is in the LTC1569-7 tunable lowpass filter.
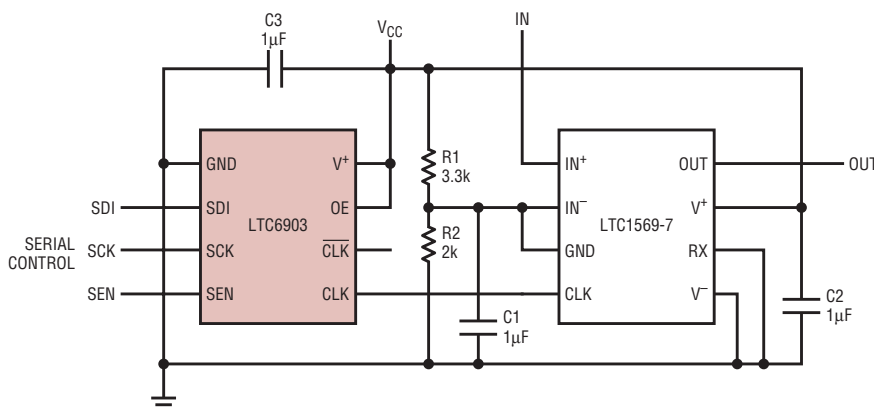

Figure 6. This simple circuit can generate a lowpass frequency response anywhere from 100Hz to 200kHz with a 0.1% resolution.

Hot Swap Controller with Power-Up Timeout Function Simplifies Hot Swapping Boards with Multiple Power Supplies

Introduction

by Anthony Ng and YK Sim

The LTC4212 is a Hot Swap controller that allows safe board insertion and removal from a live backplane. It features a supply range of 2.5V to 16.5V, programmable soft-start with inrush current limiting, automatic retry or latched mode operation, a high side drive for an external N-channel MOSFET and dual level overcurrent fault protection.

Unlike many Hot Swap controllers, the LTC4212 does not monitor the load side of the MOSFET directly. Instead, the LTC4212 interfaces with external power supply monitor ICs or directly with the PGOOD pin of a switching regulator. This permits the LTC4212 to monitor any number of supplies on the board. It has a power-up timeout function that disconnects a card from the backplane supply when the monitored supplies do not power-up within the programmable timeout period and a glitch filter to reject short term glitches in the monitored supplies after normal power-up.

Figure 1 shows a typical application, which uses the LTC1727-2.5V to monitor the outputs of two LDOs (LT1963) and the 5V output at the source (load) of the external N-channel MOSFET.

Power-Up Timeout Function

The LTC4212 has a power-up timeout function, implemented via 3 pins: PGI, PGT and PGF. The PGI (or Power Good Input) pin is a high impedance input pin that is normally connected to the $\overline{RST}$ or COMPn pins of a supply monitor IC such as the LTC1727, or to the PGOOD pin of one or more DC/DC converters. Since the $\overline{RST}$, COMPn and PGOOD pins are typically open drain pins, the LTC4212 can monitor any number of supplies by just connecting the open drain pins together. The PGI pin requires a pull-up resistor (R4 in Figure 1) when monitoring open drain pins.

Power Good Timer

An external capacitor (C_{PGT}) connected from the PGT (Power Good Timer) pin to ground sets the power-up timeout period, at the end of which the LTC4212 samples the PGI pin. The timeout period is 1.81s/µF and is accurate to within ±10% assuming ideal capacitors. The power good timer charges and discharges C_{PGT} between 0.65V and 0.95V using 5µA current sources for 14 cycles to generate the timeout period. If the PGI pin is less than 1.236V when sampled, PGT trips the Electronic Circuit Breaker (ECB). This causes the GATE pin to be pulled immediately to ground to disconnect the board from the backplane supply and the $\overline{FAULT}$ pin goes low to indicate that the ECB was tripped.

Power Good Glitch Filter

Another external capacitor (C_{PGF}) connected from the PGF (Power Good Filter) pin to ground sets the duration of the glitch filter for the PGI pin. After normal power-up, the glitch filter is enabled to reject any short-term pulses at the PGI pin. C_{PGF} is charged by a 5µA pullup current source as long as the PGI pin is low. When a monitored supply drops out of regulation, the PGI pin goes low and V_{PGF} starts to ramp
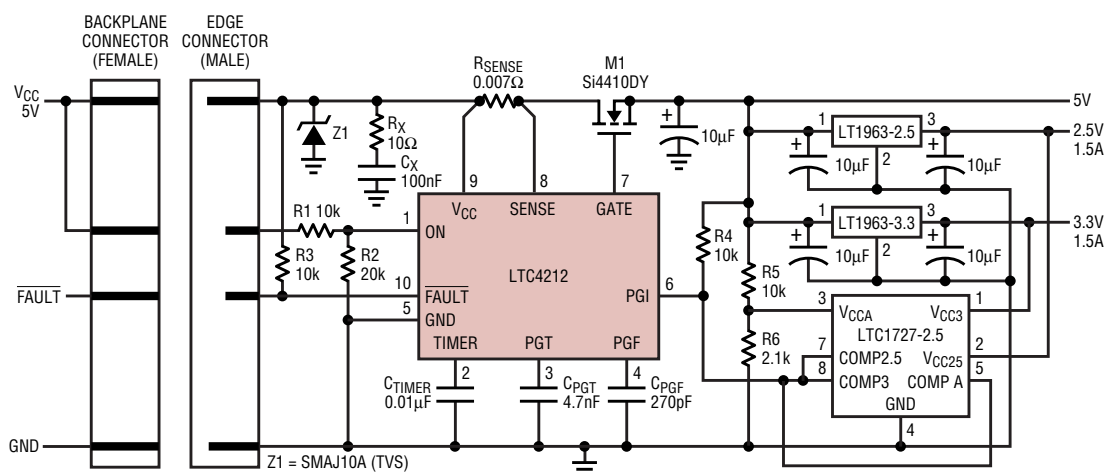

Figure 1. Hot Swap controller with power-up timeout and glitch filtering

up. When it rises above 1.236V, the glitch filter trips the ECB. The GATE pin is immediately pulled to ground and the $\overline{\text{FAULT}}$ pin goes low.

Electronic Circuit Breaker

The Electronic Circuit Breaker (ECB) can be tripped by an overcurrent fault, a power good timeout fault or by a glitch filter fault. When the ECB trips, the GATE pin is pulled down to ground immediately to disconnect the board from the backplane supply. The $\overline{\text{FAULT}}$ pin is pulled low whenever the ECB trips. In order to reconnect the board, the ON pin must be taken low for at least 120µs to reset the ECB or the V_{CC} must be below 2.2V for more than 30µs.

Overcurrent Protection

The load current is sensed by monitoring the voltage across an external sense resistor (R_{SENSE} in Figure 1). During power-up, a soft-start circuit limits the load current to $50mV/R_{SENSE}$. After normal power-up, 2 comparators, FASTCOMP and SLOWCOMP, monitor the load current. FASTCOMP trips the ECB if the load current exceeds $150mV/R_{SENSE}$ for 500ns and protects the external MOSFET and load against fast and large overcurrent conditions. SLOW-COMP trips the ECB if the load current exceeds $50mV/R_{SENSE}$ for more then 18µs.

Typical Application

Figure 1 shows LTC1727-2.5 triple supply monitor providing three comparators to monitor the voltage at the V_{CCA}, V_{CC3} and V_{CC25} pins. Each comparator responds to a 10% overdrive in 50µs and exhibits a response time that decreases with overdrive. With a 1% overdrive, the response slows to 150µs. The maximum trip point of each comparator is –5% for V_{CC3} and V_{CC25} and varies with R5 and R6 for V_{CCA}. Setting R5 to 11.8k and R6 to 3.01k sets the trip-point for the V_{CCA} comparator to 4.75V or 5V–5%. When any of the three monitored supplies are below –5% for about 60µs, the corresponding open drain output COMP3, COMP25 or COMPA is pulled
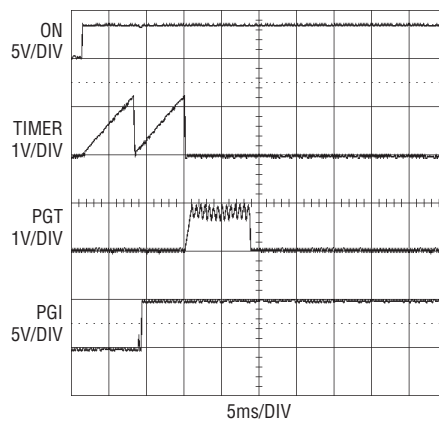

Figure 2. Normal power-up sequence (no load)

low. In Figure 1, all three open drain outputs are shorted to the PGI pin of the LTC4212 and share a single pull-up resistor, R4.

The LT1963-2.5 and LT1963-3.3 are fast transient response LDO regulators that can supply 1.5A of output current at voltages of 2.5V (+3%, –3.5%) and 3.3V (±3%) respectively. A minimum output capacitor of 10µF (ESR of 3Ω of less) is needed to prevent oscillations, and larger capacitors may be required to limit ripple or improve transient response with large transient loads.
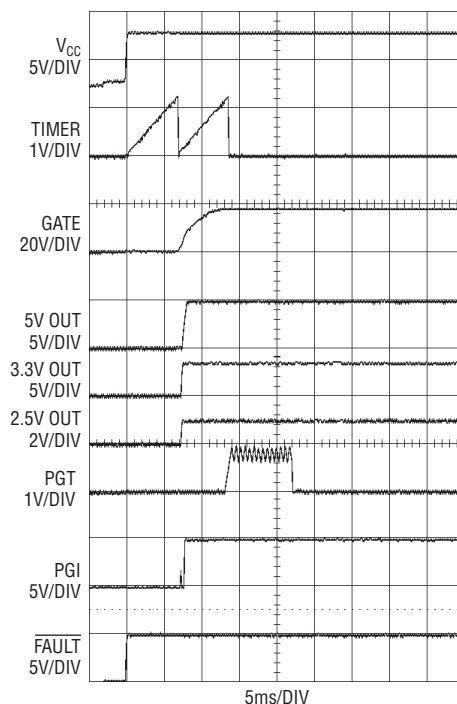

Figure 3. Power-up with load

Normal Power-Up Sequence

Figure 2 shows a normal power-up sequence with unloaded 2.5V, 3.3V and 5V outputs. When V_{CC} rises above 2.2V and the ON pin is greater than 1.316V, the LTC4212 starts the 1st timing cycle. A 2µA current source charges an external capacitor (C_{TIMER}) connected from the TIMER pin to ground. When V_{TIMER} rises avbove 1.236V, the TIMER pin is pulled immediately to ground and C_{TIMER} is discharged. The second timing cycle is started and FASTCOMP is enabled.

During the second timing cycle, a soft-start circuit in the LTC4212 servos the GATE pin to regulate the inrush current at $50mV/R_{SENSE}$. The 2µA current source is re-enabled to charge C_{TIMER}. From the start of the 2nd cycle, the GATE rises to its final value in around 7ms. The outputs of the linear regulators rise up in 1ms. At the end of the second timing cycle (when V_{TIMER} rises above 1.236V again), the soft-start circuit is disabled and a 10µA current source continues to pull-up the GATE pin. At the same time, SLOWCOMP is enabled, the TIMER pin is pulled back to ground and the LTC4212 starts the power good timer. At timeout, the PGI pin is sampled. In Figure 2, PGI goes high (>1.236V) well before timeout and the board remains powered up as is normal. Since the PGI pin is only sampled at timeout, any transients at the PGI pin during supply ramping are ignored.

Figure 3 shows a normal power-up sequence with the 2.5V and 3.3V outputs loaded with 1A.

Power-Up with Fault Sequence

Figure 4 shows power-up with a short at the 5V board supply output, V_{CCA}. During the 2nd timing cycle, the gate voltage ramps up initially to the point where the FET just turns on. After that it flattens out due to action of the soft-start circuit to limit the load current to $50mV/R_{SENSE}$ or roughly 7A. The V_{CC} backplane supply dips 0.5V due to the 7A flowing in the interconnection to the 5V, 10A limited supply. At the end of the 2nd cycle, the soft-start circuit is replaced with a 10µA pull-up current
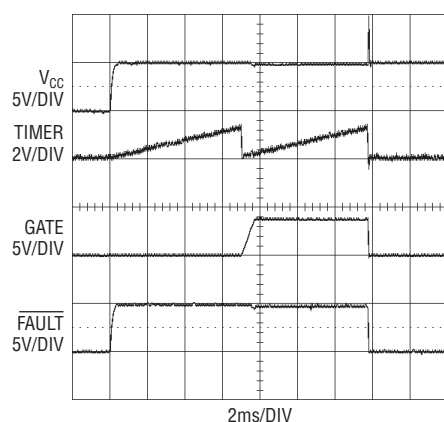
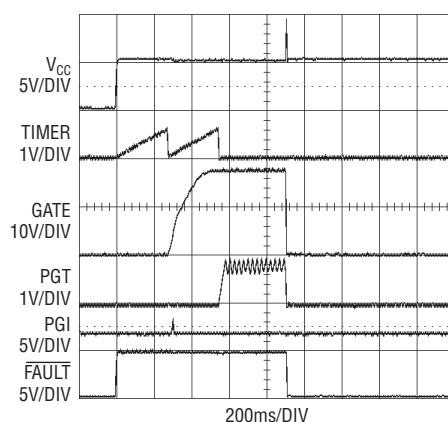**Figure 4. Power-up with the 5V output shorted to GND**

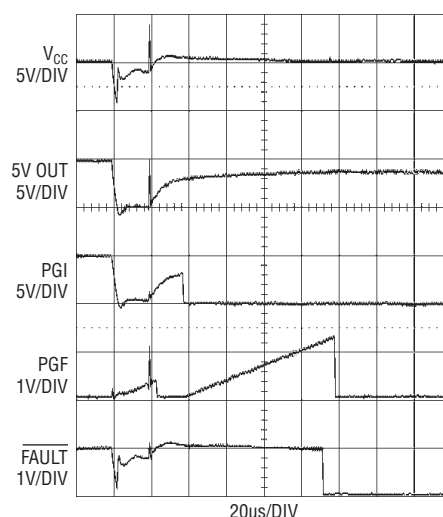**Figure 5. Power-up with the 3.3V output shorted to GND**

Figure 6. Glitch filter operation

source. This ramps the gate of the FET up and the load current rises until the SLOWCOMP trips the ECB. The gate voltage pulls down in 1µs to 2µs when the fast pulldown circuit is activated. Stray inductance causes the V_{CC} supply to spike when the load current is terminated. The power good timer and glitch filter are disabled when the ECB has been tripped.

If any of the LDO outputs are shorted to ground, the short circuit protection in the LDO reduces the fault current and the board does not latch off after the second timing cycle. As shown in Figure 5, the power good timer samples the PGI pin at timeout and trips the ECB since PGI is low. The GATE pin is pulled to ground immediately to disconnect the board from the backplane supply.

Figure 6 shows the response of the glitch filter to a 20µs overload at the 5V output after normal power-up. The comparators in the LTC1727-2.5 take PGI low whenever the 5V supply or any of the LDO outputs drop below their lower thresholds. The glitch filter capacitor (C_{PGF}) is charged by a 5µA pull-up current source whenever PGI goes low. The first PGF ramp is due to the 20µs overload but V_{PGF} does not ramp above 1.236V. The second pulse is a result of the time it takes the 5V linear regulator to recover from the over load and is long enough for V_{PGF} to ramp above 1.236V, causing the glitch filter to trip the ECB. The GATE pin is pulled immediately to ground to disconnect the board from the backplane supply. If the PGF pin is tied to ground, the PGF pin remains permanently below 1.236V and the glitch filter is effectively disabled. Tying PGF to ground causes the LTC4212 to ignore a low PGI state after normal power-up.

Interfacing with the $\overline{RST}$ Pin

The PGI pin of the LTC4212 can be connected to the $\overline{RST}$ pin instead of the COMPx pins of the LTC1727-2.5. The $\overline{RST}$ pin is delayed by 200ms compared to the COMPn pins and C_{PGT} must be adjusted to include the 200ms delay for the board to power-up normally. In addition, any transients on the monitored supplies that exceed the response time of the comparators in the LTC1727-2.5 will cause $\overline{RST}$ to go low for at least 200ms. This causes the glitch filter to trip the ECB.

Auto-Retry Application

Figure 7 shows an application that automatically tries to power-up the board after the ECB has been tripped due to a shorted load supply output. This circuit uses the LTC1326-2.5 supply monitor chip and ties its $\overline{RST}$ output
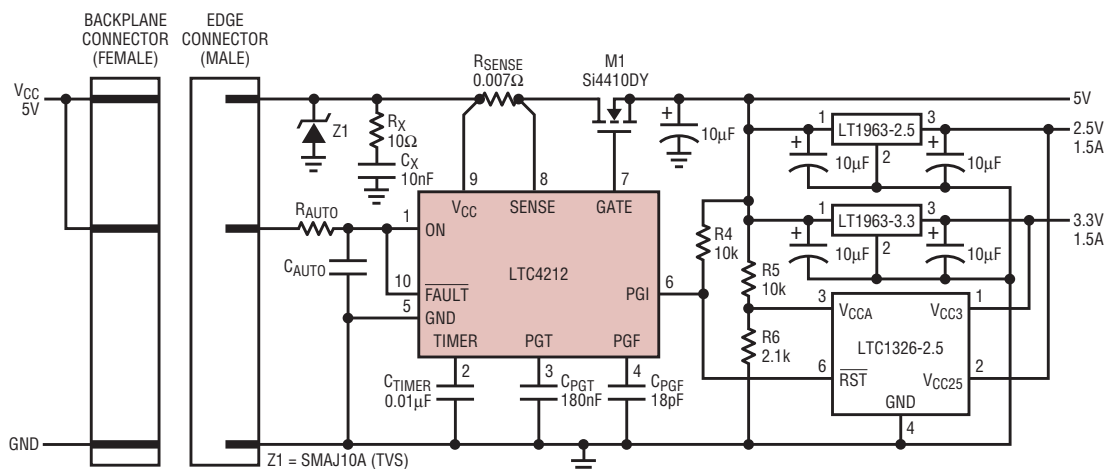

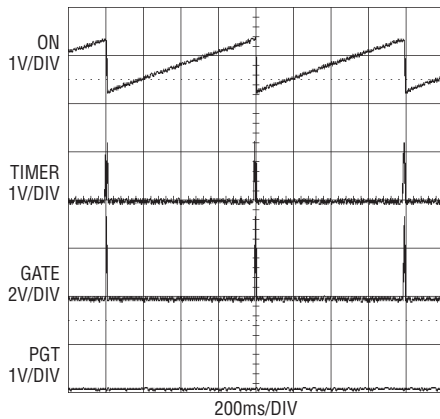
Figure 7. Auto-retry application

Figure 8. Auto-retry with short at 5V output

Figure 9. Auto-retry with short at LDO output

to the PGI pin of the LTC4212. The $\overline{RST}$ signal goes high 200ms after all the monitored voltages rise above the thresholds of the V_{CCA}, V_{CC3} and V_{CC25} comparators in the LTC1326-2.5. The ON pin is shorted to the $\overline{FAULT}$ pin and is pulled up by a 1MΩ resistor (R_{AUTO}) to V_{CC}. A 2µF capacitor (C_{AUTO}) connected from the lower end of R_{AUTO} to ground sets the auto-retry duty cycle. The LTC4212 will retry as long as the short persists. R_{AUTO} and C_{AUTO} must be selected to keep the duty cycle low in order to prevent overheating in the external N-channel MOSFET.

Figure 8 shows the auto-retry cycle when the 5V output is shorted to ground. SLOWCOMP trips the ECB after the 2nd timing cycle. This causes the $\overline{FAULT}$ pin to be pulled low by an internal N-channel FET and C_{AUTO} is discharged to ground. The GATE pin is pulled immediately to ground to disconnect the board. Note that in Figure 8, the time-base setting causes the first and second timing cycles to appear as a single spike. When the ON pin goes below its lower threshold of 0.455V (typical) for more than 120µs, the ECB is reset. The internal N-channel FET at the $\overline{FAULT}$ pin is switched off and R_{AUTO} starts to charge C_{AUTO} slowly towards V_{CC}.

When the ON pin rises above its upper threshold of 1.316V, the LTC4212 attempts to reconnect the board and start the first timing cycle. With a dead short at the 5V output as in Figure 8, the ECB trips after the second timing cycle when the soft-start circuit is
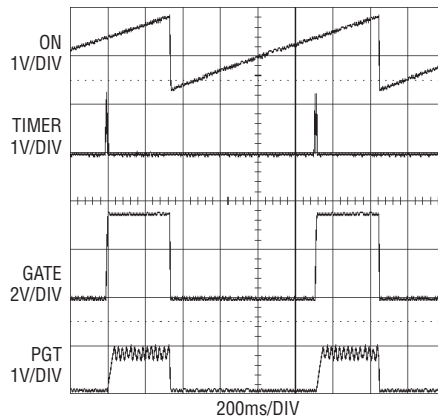
disabled and a 10µA pull-up current source is connected to the GATE pin. The entire cycle is repeated until the short is removed. The duration of each cycle is dominated by the time needed to charge C_{AUTO} between the lower and the upper threshold voltages of the ON pin. With R_{AUTO} = 1MΩ and C_{AUTO} = 2µF, the cycle time is 800ms. The switch is on for about 6ms giving a duty cycle of 0.75%.

At the end of the 2nd timing cycle, the GATE pin is about 3V due to the action of the soft-start circuit (which limits the current to 50mV/R_{SENSE}) and the presence of the short at the

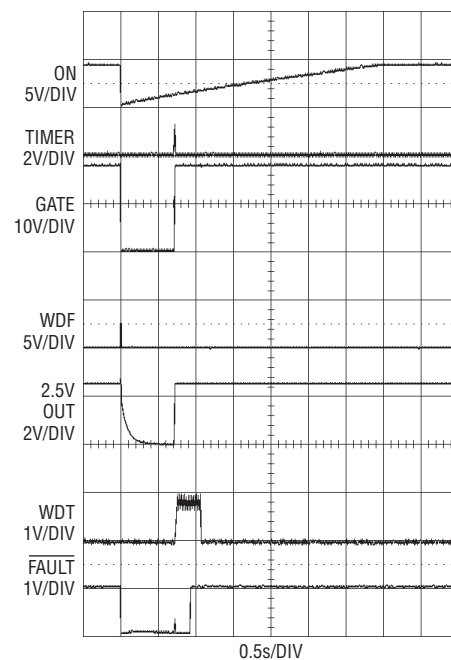
Figure 10. Auto-retry caused by a transient short at the 2.5V output

5V output. The 10µA current source takes several milliseconds to ramp up the 3.3nF of GATE pin capacitance. As a result, SLOWCOMP tends to trip the ECB instead of FASTCOMP.

When powering up with a short at the output of either LDO, the short circuit protection in LDO reduces the fault current. At the end of the Power Good timeout period, the PGI pin is still low due to the short circuit. As shown in Figure 9, the external N-channel MOSFET is turned on for a longer part of each auto-retry cycle if the overload is not enough to trip both SLOWCOMP and FASTCOMP. With R_{AUTO} = 1MΩ and C_{AUTO} = 2µF, the duty cycle increases to 29% causing the LT1963-2.5 LDO to heat up to a case temperature of 106°C at an ambient temperature of 25°C. A larger value of C_{AUTO} is required when operating from higher ambient temperatures. The Si4410DY MOSFET does not heat up appreciably due to its low $R_{DS(ON)}$.

If a transient short at the output of an LDO is long enough to cause the monitoring comparators in the LTC1326-2.5 (13µs typical delay) to switch, the $\overline{RST}$ output will go low for at least 200ms. As shown in Figure 10, the Power Good glitch filter trips the ECB and initiates an auto-retry cycle.

Conclusion

The LTC4212 simplifies the design of hot swapping boards with multiple power supplies. The status outputs from power supply ICs or supply monitor ICs—such as $\overline{RST}$, PGOOD and COMPn—are typically open drain outputs and can be connected together and monitored by the PGI pin of the LTC4212. The power good timer automatically disconnects the card from the backplane supply should any of the supplies fail to power-up within the programmed time period. After normal power-up, the glitch filter provides a means to detect out of regulation supplies while rejecting dips that last shorter than a programmable time period. *LT*

Low Voltage Wizardry Provides the Ultimate Power-On Reset Circuit

by Bob Jurgilewicz

The Low Voltage Reset Problem

A fundamental problem plaguing most power supply supervisory ICs is the inability to establish the correct logic state at the reset node with low input supply voltages. Prior to power-up, external leakage currents often drive the reset node above the logic threshold of the microprocessor input. The LTC2903 (available in a 6-lead SOT-23) virtually eliminates this floating reset node problem by using a proprietary circuit to establish a low impedance path from the reset node to ground. Figure 1 shows just how easy it is to hook up a quad supervisor using the LTC2903.

When a supply, or supplies, resides below its supervisory threshold, the desired state at the reset node is logic low. Typically, an open-drain NMOS transistor is used to pull down the reset node (Figure 2). At low input voltages (<1V), the NMOS transistor lacks sufficient transconductance to overcome the pull-up current source, and the reset node may float up to a logic high level. If the reset node is signaling logic high while it is supposed to be low, a potential system reliability problem exists.

A common approach used to overcome the floating reset node is to integrate an active PMOS transistor pull-up and to specify an external resistor to ground. The external resistor pulls down the reset node at low input voltages. There are several drawbacks to this approach. First, unless an extra supply pin is dedicated to the internal PMOS source, the user has no control of the pull-up voltage (it is hard wired
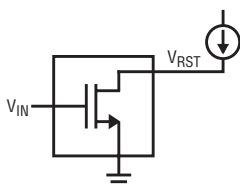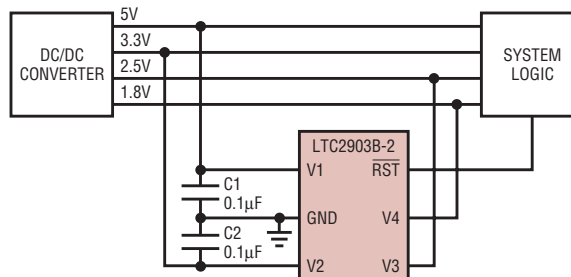

Figure 2. Traditional NMOS pull-down circuit

inside the chip). Second, there is a limit to how small the external resistor can be before the resistor overcomes the pull-up strength of the PMOS transistor. Third, low power systems will suffer while the reset node is logic high, since the external resistor will continuously dissipate power. With a 5V output and a 100kΩ external pull-down resistor, the system must support an additional 50µA load at the reset output, 2.5 times the typical quiescent current of most LTC voltage supervisors. Finally, a strong active pull-up makes wired-OR connections at the reset node impractical since an external circuit must overcome active pull-up current at logic low and guard against pushing reverse current into the pull-up supply at logic high.

The Solution

The LTC2903 solves the floating reset node problem with none of the drawbacks discussed above. A proprietary circuit establishes, at low input voltages, a low impedance path from the reset node to ground. The low impedance path pulls down the reset node and will typically conduct current even when all input voltage supplies are at zero volts (see Figure 3). The reset output is guaranteed to sink at least 5 µA (V_{OL} = 0.15V) for V1, V2 or V3 down to 0.5V. Furthermore, the LTC2903 senses when there is sufficient voltage to operate the NMOS pull-down transistor reliably and will

disconnect the low impedance shunt from the reset node. Removal of the low impedance shunt eliminates the leakage path that would interfere with any pull-up current source. The low impedance shunt re-enables when all supplies are below the level required for NMOS conduction.

A significant performance boost is obtained when input supplies are ramped together. Low impedance shunt action is available from three of the four inputs on the LTC2903 (V1, V2, V3), providing up to three times the pull-down strength available from just a single input. The LTC2923 Power Supply Tracking Controller provides such ramping capability (see waveforms in Figure 4). Figure 5 shows how the LTC2903 reset output performs against the competition with a 10kΩ resistor pulling up the reset node to
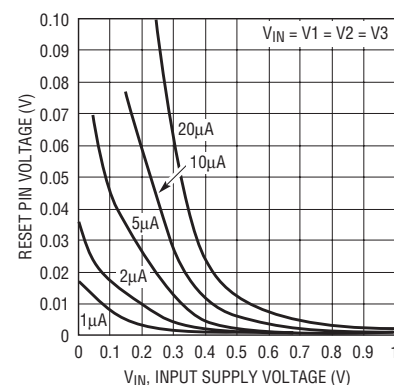

Figure 1. Typical application using the LTC2903B for quad supply monitoring

Figure 3. LTC2903 reset pin voltage (V_{OL}) vs external pull-up current at low input supply voltage
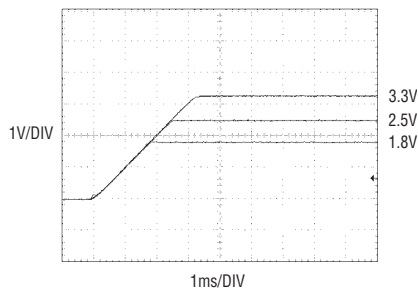
Figure 4. LTC2923 power supply tracking controller ramping example

the input supply. In particular, note that the reset output does not exceed 0.1V during power-on when ramping the supplies together (V1 = V2 = V3), which should satisfy the most demanding V_{OL} requirements.

LTC2903 Features

The LTC2903A, LTC2903B and LTC2903C is a family of quad supply monitors in 6-lead, low profile (1mm) SOT-23 packages. Table 1 summarizes available voltage input combinations. Threshold *accuracy* is ±1.5% of the monitored voltage over the temperature range of –40°C to +85°C (see "Implications of Threshold Accuracy" below).

Thresholds are configured for 10% undervoltage monitoring. For applications requiring an adjustable trip threshold, use the V4 input on the LTC2903A. Connect the tap point on an external resistive divider (R1, R2) placed between the positive voltage being sensed and ground, to the high impedance input on V4. The LTC2903A compares the voltage on the V4 pin to the internal 0.5V reference. Figure 7 demonstrates a generic
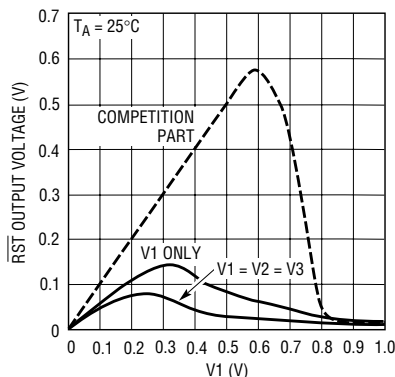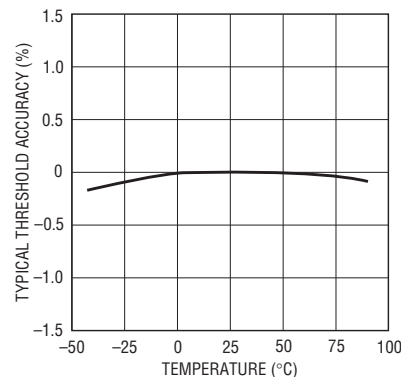
Table 1. LTC2903 voltage input combinations		
LTC2903A	**LTC2903B**	**LTC2903C**
3.3V, 2.5V, 1.8V, ADJ (0.5V)	5V, 3.3V, 2.5V, 1.8V	5V, 3.3V, 1.8V, -5.2V

setup for the positive adjustable application.

The reset output remains low during power-up, power-down and brownout conditions on any of the four voltage inputs. Voltage output low (V_{OL}) is guaranteed to be 150mV or less while pulling down 5µA with V1, V2 or V3 at 0.5V. A 200ms delay timer is integrated with the reset function. After all voltage inputs exceed their respective thresholds for 200ms, the reset output pulls high. The reset output style is open-drain with a weak internal pull-up to the V2 supply. External pull-up resistors can be used to improve rise times or to achieve logic levels above the V2 voltage.

Power supply glitch filtering is built in to each of the four comparators. The internal chip voltage (V_{CC}) is derived from the greater of the V1 or V2 inputs. Quiescent current drawn from V_{CC} is typically 20µA.

Implications of Threshold Accuracy

Specifying system voltage margin for worst-case operation requires consideration of three factors: power-supply tolerance, IC supply voltage tolerance and supervisor reset threshold accuracy. Highly accurate supervisors ease the design challenge by decreasing the overall voltage margin required for reliable system operation. Consider a 5V

system with a ±10% power supply tolerance band. System ICs powered by this supply must operate reliably within this band (and a little more, as explained below). The bottom of the supply tolerance band, at 4.5V (5V–10%), is the exact voltage at which a *perfectly accurate* supervisor would generate a reset. Such a perfectly accurate supervisor does not exist—the actual reset threshold may vary over a specified band (±1.5% for the LTC2903 supervisors). Figure 6 shows the typical relative threshold accuracy for all four inputs, guaranteed over temperature.

With this variation of reset threshold in mind, the nominal reset threshold of the supervisor resides *below* the minimum supply voltage; just enough so that the reset threshold band and the power supply tolerance bands do not overlap. If the two bands overlap, the supervisor could generate a false or nuisance reset when the power supply remains within its specified tolerance band (say, at 4.6V).

Adding half of reset threshold accuracy spread (1.5%) to the ideal 10% thresholds, puts the LTC2903 thresholds at 11.5% (typical) below the nominal input voltage. For example, the 5V typical threshold is 4.425V, or 75mV below the ideal threshold of 4.5V. The guaranteed threshold lies in the band between 4.5V and 4.35V, over temperature.

The powered system must work reliably down to the lowest voltage in the threshold band, or risk malfunc-

Figure 5. LTC2903 reset output voltage with a 10kΩ pull-up to V1 vs V1

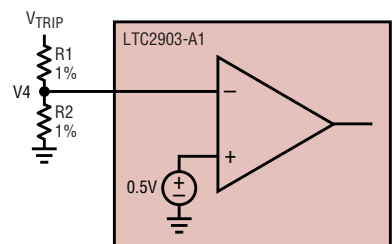**Figure 6. LTC2903 typical threshold accuracy vs temperature**

Figure 7. Setting the positive adjustable trip point

tion before the reset line falls. In our 5V example, using the 1.5% accurate supervisor, the system ICs must work down to 4.35V. System ICs working with a sloppier ±2.5% accurate supervisor must operate down to 4.25V, increasing the required system voltage margin, and the likelihood of system malfunction.

Noise Sensitivity

In any supervisory application, supply noise riding on the monitored DC voltage can cause spurious resets, particularly when the monitored voltage approaches the reset threshold. One common mitigation technique is to add hysteresis to the input comparator, but this has drawbacks. The amount of added hysteresis, usually specified as a percentage of the trip threshold, effectively degrades the advertised accuracy of the part. The LTC2903 does not use hysteresis.

To minimize spurious resets while maintaining threshold accuracy, the LTC2903 employs two forms of noise filtering. The first line of defense incorporates proprietary tailoring of the comparator transient response. Transient events receive electronic integration in the comparator and must exceed a certain magnitude and duration to cause the comparator to switch.
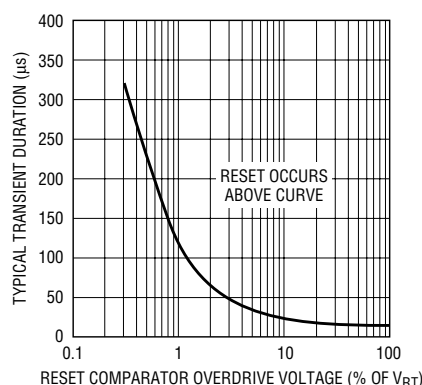

Figure 8. Typical transient duration vs overdrive required to trip comparator

Figure 8 illustrates the typical transient duration versus comparator overdrive (as a percentage of the trip threshold) required to trip the comparators. Once any comparator is switched, the reset line pulls low. The reset time-out counter starts once all inputs return above threshold, and the nominal reset delay time is 200 milliseconds. The counter clears whenever any input drops back below its threshold. This reset delay time effectively provides further filtering of the voltage inputs and is the second line of defense against noise. A noisy input with frequency components of sufficient magnitude above $f = 1/t_{RST}$ = 5Hz holds the reset line low, preventing oscillatory behavior on the reset line.

A reset line holding low provides a remarkably good indication of power supply problems. Common supply problems include improperly set output voltage and/or poor supply regulation.

Although all four comparators have built-in glitch filtering, use a bypass capacitor on the V1 and V2 inputs because the greater of V1 or V2 provides the V_{CC} for the part (a 0.1µF ceramic capacitor satisfies most applications). Apply filter capacitors on the V3 and V4 inputs if supply noise overcomes the built in filtering.

Conclusion

The LTC2903 quad supply monitor greatly improves system reliability by eliminating false resets and maintaining very high accuracy. Its proprietary reset pull-down circuit solves the long standing low voltage POR problem. The reset output can now maintain a logic-low at power-supply voltages down to zero volts. The reset output is guaranteed to sink at least 5µA (V_{OL} = 0.15V) for V1, V2 or V3 down to 0.5V. The LTC2903 monitors four voltages with 1.5% accuracy (over the entire temperature range) using comparators with built-in noise rejection. Non-standard voltages can be monitored with the 0.5V threshold adjustable input. ⨆⊤

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age dips on the supply powering the converter. In the end, the efficiency of the converter suffers which leads to longer charge times.

To illustrate this, two mid-range digital cameras from an industry-leading company are analyzed. Both camera photoflash units use a microprocessor controlled flyback converter. The first microprocessor controlled circuit is simple while the second uses numerous external components to implement a more complex control scheme. Table 3a shows a comparison of the performance parameters between the LT3468 circuit and the microprocessor-based circuits. More telling, though, is Table 3b, which

makes the same comparison, but normalizes the input current.

The performance benefits of the LT3468 are obvious as shown in the nearly 44% reduction in charge time when compared to the microprocessor-based solutions. In addition to the charge time reduction, the LT3468 solution requires fewer, and smaller, components thus significantly reducing the overall size of the circuit.

Conclusion

The LT3468 and LT3468-1 provide a simple and efficient means to charge photoflash capacitors. The high levels of integration inside the parts result in tight output voltage distributions,

small solution size, lower total solution cost and minimal microprocessor software overhead. When compared to traditional methods, charge times can be lowered by more than 44%. The LT3468 family offers a range of input currents for flexibility in the trade-off between input current and charge time. ⨆⊤

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New Power for Ethernet—Disconnect and Clean Up (Epilogue to a 3-part series)

by Jacob Herbold

Introduction

Power over Ethernet, the latest improvement to the venerable Ethernet networking standard, allows up to 13W of DC power to be distributed down the same CAT-5 cables used to transmit data. This magazine recently ran a 3-part series, 'New Power for Ethernet', which introduced IEEE 802.3af Power over Ethernet (*Linear Technology* Vol. XII, No. 3, August 2002, pg. 9), described 802.3af Powered Devices (*Linear Technology* Vol. XII, No. 4, December 2002, pg. 9), and discussed 802.3af Detection and Classification protocols (*Linear Technology* Vol. XIII No. 2, July 2003, pg. 9). As an epilogue to this series, this article ties up some of the loose ends left by the then not-yet-finalized 802.3af standard and discusses the *power off* part of the standard in more detail than presented in the previous articles.

The third installment of the 'New Power for Ethernet' series covered detection and classification, or translated from 802.3af jargon: "how to tell when to turn power on." This postscript focuses on the opposite case: "how to tell when to turn power off," or "disconnect" in 802.3af parlance. The Power Sourcing Equipment (PSE) must turn an Ethernet port's power off once it determines there's no longer a Powered Device (PD) connected that port. The 802.3af standard defines two methods, DC disconnect and AC disconnect, which a PSE can use to sense the absence of a PD.

The latter part of this article brings the 'New Power for Ethernet' series up to date with the 802.3af specification. Since the third installment of the series published, the specification has been ratified and received the title *IEEE standard 802.3af-2003*. Back when this series of articles began, the 802.3af specification was still being revised. Consequently, parts of the specification have undergone minor changes since earlier installments were written.
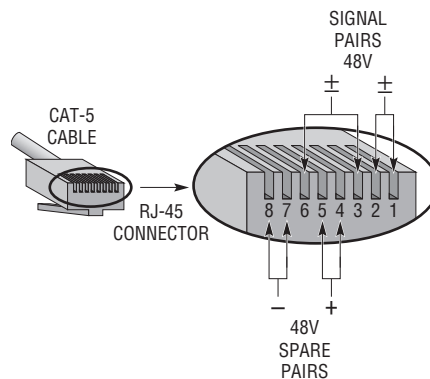

Figure 1. Signal and spare pairs on RJ-45 connector at the PD

Further details are presented towards the end of this article.

Power over Ethernet Disconnect

In the world of Power over Ethernet—PoE for short—turning off the power at the right time is just as important as turning it on at the right time. For the same reason a PSE must never send power to a device that doesn't expect it, a PSE must not leave power on after the powered device has been unplugged so that a powered cable is not plugged into a device that doesn't expect power. Once the PD is removed, a powered cable is like a snake waiting to strike some unsuspecting computer with 48V at nearly half an amp. The 802.3af standard defines two methods for a PSE to sense when the PD is unplugged, allowing implementers to select the method best suited to their systems.

DC Disconnect

DC disconnect determines the presence of a PD based on the amount of DC current flowing from the PSE to the PD. When the current stays below a threshold I_{MIN} for a given time t_{DIS}, the PSE assumes that the PD is absent and turns off the power. It's almost as simple as that. The only complication is that a PD is allowed to reduce its power consumption below $I_{MIN} \bullet V_{PORT}$ (V_{PORT} is the voltage supplied to the PD) while avoiding being DC disconnected by drawing periodic bursts of current. This lowers the minimum power and prevents an Ethernet powered thermostat, for example, from self-heating and giving incorrect readings.

The specifications for DC disconnect are as follows. The PSE's current threshold I_{MIN} must be between 5mA and 10mA. The PSE cannot turn off
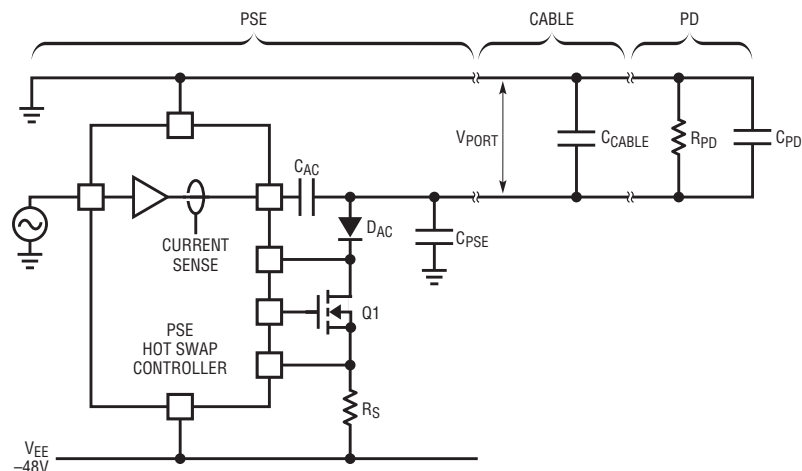

Figure 2. Simplified PSE implementing AC disconnect

power unless the current is below I_{MIN} for a time, t_{DIS}, of 300ms to 400ms. The PSE must be able to recognize a current pulse width of 60ms or more. At the PD end, the minimum current to remain connected is 10mA or more. A low power PD must pulse its current above 10mA for 75ms at least once every 250ms, which is about a tenth of a watt of average power.

A PSE that implements DC disconnect must accurately measure current over 2 decades, from 5mA (DC disconnect) to 450mA (current limit). There's an inherent trade-off in the size of the sense resistor (R_S) used to make this measurement. With higher resistance, 5mA is easy to measure but the resistor dissipates a significant amount of power at 450mA. Lower resistance reduces the power dissipation at high currents but at 5mA the voltage drop is so small, it's hard to accurately measure. Linear Technology builds two PSE Hot Swap™ controller ICs, the LTC4258 and LTC4259, with low offset and low noise sense amplifiers that can measure 5mA current through a 0.5Ω resistor and sense DC disconnect reliably. Note that PSE solutions using higher resistance for R_S can suffer accuracy problems caused by resistor heating unless R_S is a physically large resistor and has a low temperature coefficient.

AC Disconnect

A PSE that implements AC disconnect measures the AC impedance of the Ethernet port. When nothing is connected to the PSE, the port should be high impedance, perhaps several megaohms. When a PD is connected, however, the port impedance is less than 26.25kΩ—usually much less if the PD draws significant power. Port impedance (Z_{PORT}) is determined by forcing voltage (V_{AC}) and measuring the resulting current (I_{AC}) that is, $Z_{PORT} = V_{AC}/I_{AC}$. Again a clear-cut concept, and there seems to be plenty of margin between a connected PD and an open circuit. Unfortunately, taking AC disconnect into the real world is fraught with complications. Figure 2 shows a simplified PSE with AC disconnect.
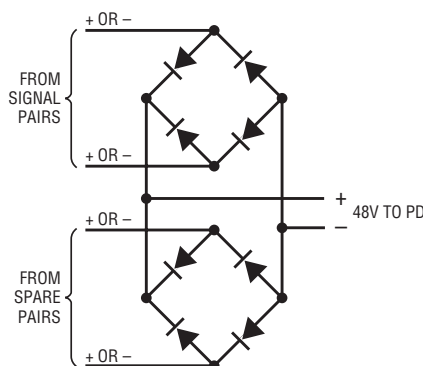

Figure 3. Autopolarity input circuit

The biggest complication comes from the very nature of a PSE's output: it supplies power to a PD, and as a power supply, it necessarily has very low impedance. A series diode, (D_{AC} in Figure 2) allows AC disconnect to overcome the PSE's low port impedance and look for a PD when the diode is not forward biased. The capacitance bypassing the PSE's output is harder to get around. The 802.3af standard defines load regulation, output impedance and ripple requirements that a PSE needs 0.1µF or so of bypass to meet. Even at 100Hz, the 0.1µF capacitor (C_{PSE} in Figure 2) brings the port impedance down to 15kΩ without the PD. Connect the PD's maximum specified impedance of 26.25k and the port impedance drops to 9.7k. AC disconnect really means finding the difference between 15k and 10k—so much for a megaohm of margin.

Some AC disconnect circuit techniques avoid the capacitance issue altogether by "cheating." Rather than measuring the port impedance, these circuits set much lower thresholds and measure the impedance of the D_{AC} diode. Be aware that circuits of this type are really performing DC disconnect but not as reliably nor in as well controlled a manner as using a sense resistor.

Linear Technology uses a different method of sensing the PD's impedance in the newly released LTC4259, shown in Figure 2. This sensing method is insensitive to the AC blocking diode, D_{AC}, and tolerates over 0.1µF of additional C_{PSE} capacitance on the port. Rather than using a conventional square wave, the LTC4259 drives a sine wave

onto the port. A sine wave has much slower slew rates (and fewer EMI problems) than a square wave of the same frequency. The controlled slew rate of the sine wave puts a specific current through the port capacitance, $C_{PORT} = C_{PSE} + C_{CABLE} + C_{PD}$, and a current that depends on the port impedance through C_{AC}. Ignoring the effects of D_{AC} and R_{PD}, the current through C_{AC} is proportional to the series combination of C_{AC} and C_{PORT}. Because the LTC4259 pays attention to the phase of the sine wave, it ignores the impedance of the blocking diode when the port current is small. The LTC4259's sensing thresholds are chosen to provide adequate margin between an open port (even with excess capacitance) and a port powering a PD.

Changes to the Earlier Parts in this Series

On page 10 of the August 2002 issue it states, "A valid PD signature consists of a 25k resistor with up to three diodes in series." As the standard is now written, the PD is allowed to have up to 1.9V of offset in series with its 25k signature resistor. Because the forward drop of three silicon diodes in series will not meet this spec at lower temperatures, the general conclusion is that a PD can only have 2 diodes in series with the signature resistor.

Two specification changes affect Part 2, published in December 2002. First off, the PD is now required to accept power of either polarity from the data pairs. The non-autopolarity input circuit shown on page 10 in Figure 3b of the December 2002 issue is no longer compliant. Figure 4, also on page 10 of the December 2002 issue has the same error; Figure 4 in this article shows a version that is compliant. The PD is also required to accept power of either polarity from the spare pairs as shown in Figure 1 (though a PSE that powers the spare pairs must have pins 4 and 5 positive with 7 and 8 negative). These two changes require every PD to have an autopolarity input circuit. An example is shown in Figure 3a on page 10 of the December issue and reproduced here in Figure 3.

Save Board Space with a High Efficiency Dual Synchronous, 600mA, 1.5MHz Step-Down DC/DC Regulator

by Damon Lee

Introduction

The ever shrinking nature of cell phones, pagers, PDAs and other portable devices drives a corresponding demand for smaller components. One way to shrink DC/DC regulator circuitry is to increase the switching frequency of the regulator, thus allowing the use of smaller and cheaper capacitors and inductors to complete the circuit. Another way is to combine the switcher and MOSFETs in one small, monolithic package. The LTC3407 DC/DC regulator does both.

The LTC3407 is a 10-lead, dual, synchronous, step-down, current mode, DC/DC regulator, intended for low power applications. It operates within a 2.5V to 5.5V input voltage range and has a fixed 1.5MHz switching frequency, making it possible to use tiny capacitors and inductors that are under 1.2mm in height. The LTC3407 is available in small DFN and MSOP packages, allowing two 600mA DC/DC Regulators to occupy less than 0.2 square inches of board real estate, as shown in Figure 1.

The outputs of the LTC3407 are independently adjustable from 0.6V to 5V. For battery-powered applications that have input voltages above
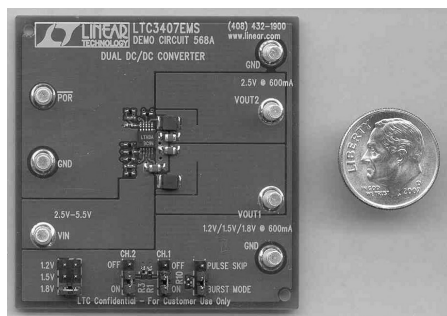

Figure 1. Two DC/DC regulators occupy less than 0.2in^2 of board space.

and below the output voltage, the LTC3407 can be used in a single inductor, positive buck-boost converter configuration. A built in 0.35Ω switch allows up to 600mA of output current at high efficiency. Internal compensation minimizes external components and board space.

Efficiency is extremely important in battery-powered applications, and the LTC3407 keeps efficiency high with an automatic, power saving Burst Mode® operation, which reduces gate charge losses at low load currents. With no load, both converters together draw only 40µA, and in shutdown, the device draws less than 1µA, making it ideal for low current applications.
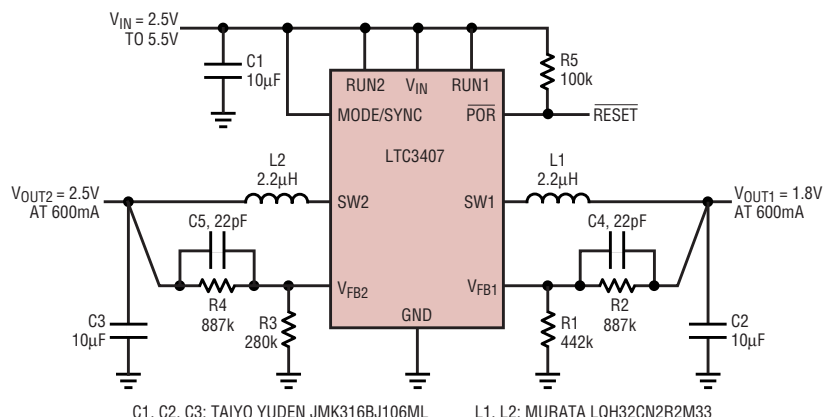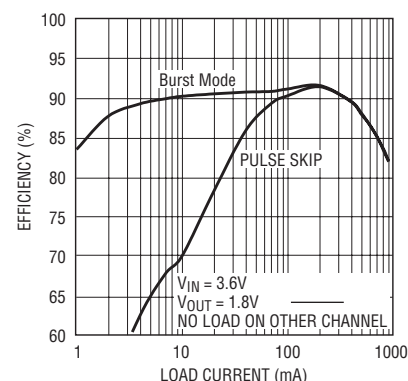

Figure 2. Comparison of Burst Mode operation and pulse skip mode. This particular data is for the circuit shown in Figure 3.

The LTC3407 uses a current-mode, constant frequency architecture that benefits noise sensitive applications. Burst Mode is an efficient solution for low current applications, but sometimes noise suppression is a higher priority. To reduce noise problems, a pulse-skipping mode is available, which decreases the ripple noise at low currents. Although not as efficient as Burst Mode at low currents, pulse-skipping mode still provides high efficiency for moderate loads, as seen in Figure 2. In dropout, the internal P-channel MOSFET switch is turned on continuously, thereby maximizing the usable battery life.
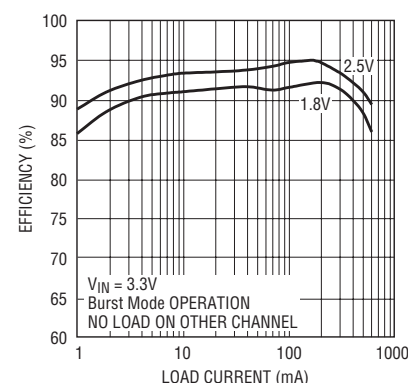

C1, C2, C3: TAIYO YUDEN JMK316BJ106ML   L1, L2: MURATA LQH32CN2R2M33

Figure 3. Dual step-down regulator provides 1.8V and 2.5V at 600mA.

Figure 4. Efficiencies of the circuit in Figure 3

C1, C2, C3: TAIYO YUDEN JMK316BJ106ML
C6: SANYO 6TPB47M
D1: PHILIPS PMEG2010

L1: MURATA LQH32CN2R2M33
L2: TOKO A914BYW-100M (D52LC SERIES)
M1: SILICONIX Si2302
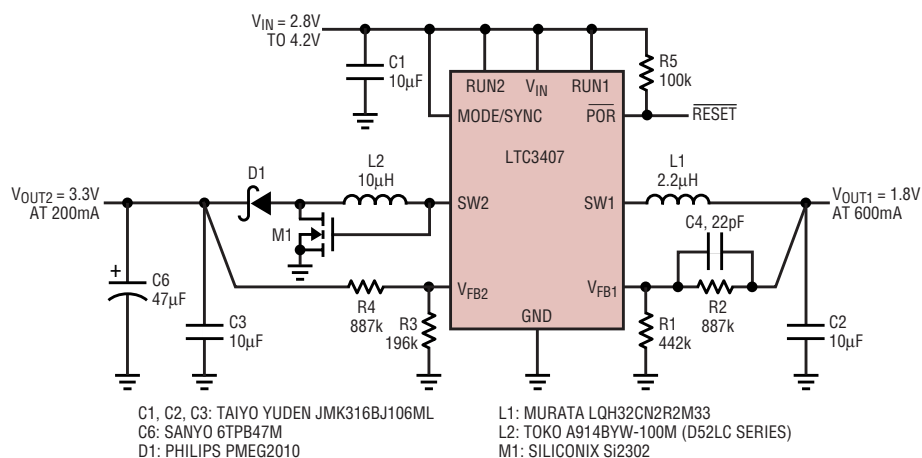
Figure 5. Single inductor, positive buck-boost regulator and a buck regulator with maximum height < 2mm

Figure 6. Efficiencies for the circuit in Figure 4

A Power-On Reset (POR) output is available for microprocessor systems to insure proper startups. Internal overvoltage and undervoltage comparators on both outputs will pull the POR output low if the output voltages are not within ±8.5%. The POR output is delayed by 262,144 clock cycles (about 175ms) after achieving regulation, but will be pulled low immediately when either ouput is out of regulation.

High Efficiency 2.5V and 1.8V Step-Down DC/DC Regulator with all Ceramic Capacitors

The low cost and low ESR of ceramic capacitors make them a very attractive choice for use in switching regulators. In addition, ceramic capacitors have a benign failure mechanism unlike tantalum capacitors. Unfortunately, the ESR is so low that it can cause loop stability issues. A solid tantalum capacitor's ESR generates a loop zero at 5kHz–50kHz that can be instrumental in giving acceptable loop

phase margin. Ceramic capacitors, on the other hand, remain capacitive to beyond 300kHz and usually resonate with their ESL before the ESR becomes effective. Also, inexpensive ceramic capacitors are prone to temperature and voltage effects, requiring the designer to check loop stability over the operating temperature range. For these reasons, great care is usually needed

when using only ceramic input and output capacitors. The LTC3407 was designed with ceramic capacitors in mind and is internally compensated to handle these difficult design considerations. High quality X5R or X7R ceramic capacitors should be used to minimize the temperature and voltage coefficients.

Figure 3 shows a typical application for the LTC3407 using only ceramic capacitors. This circuit provides a regulated 2.5V output and a regulated 1.8V output, both at up to 600mA, from a 2.5V to 5.5V input. Efficiency for the circuit is as high as 95% as shown in Figure 4.

2mm Height Li-Ion, Single Inductor, Buck-Boost Regulator and Buck Regulator

Lithium-Ion batteries are popular in many portable applications because of their light weight and high energy density, but the battery voltage ranges from a fully charged 4.2V down to a drained 2.8V. When a device requires an output voltage that falls somewhere in the middle of the Li-Ion operating range, such as the 3.3V I/O supply, a simple buck or boost converter does not work. One solution is a single inductor, positive buck-boost regulator, which allows the input voltage to vary above and below the output voltage.

In Figure 5, regulator 2 is configured as a single inductor, positive buck-boost regulator to supply a constant 3.3V with 200mA–400mA of load current, depending on the battery voltage. The circuit is well suited to portable
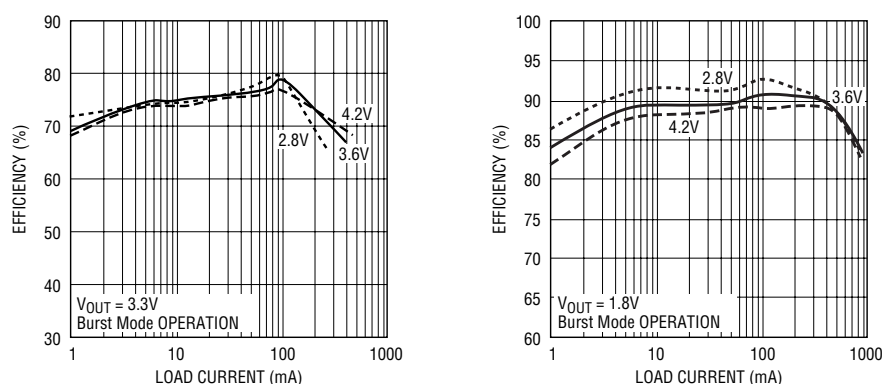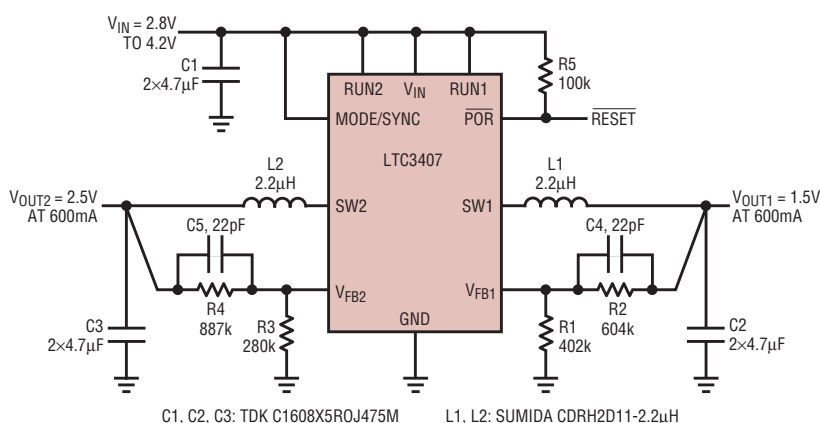

C1, C2, C3: TDK C1608X5ROJ475M   L1, L2: SUMIDA CDRH2D11-2.2μH

Figure 6. Low profile (1.2mm) Lithium-Ion dual step-down regulator
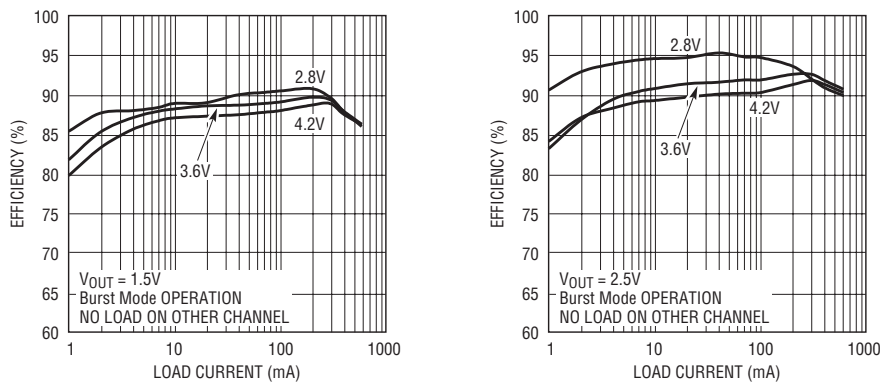
Figure 7. Efficiencies for the circuit in Figure 6

applications because none of the components exceed 2mm in height.

The efficiency varies with the input supply, due to resistive losses at high currents and to switching losses at low currents. As shown in Figure 6, the typical efficiency across both battery voltage and load current is about 75% for the 3.3V output, and about 90% for the 1.8V output.

Low Profile, 1.2mm Height, Lithium-Ion Dual Supply

In some applications, minimizing the height of the circuit takes prime importance. New low profile capacitors and inductors can be combined with the already low profile 1.1mm maximum height of the LTC3407's 10-lead MSOP package. Figure 6 shows a circuit designed to meet a 1.2mm maximum

height requirement, and to occupy less than $0.2in^2$. The circuit provides 2.5V and 1.5V outputs, each with up to 600mA of load current. Two 4.7µF ceramic capacitors are used on each supply, due to the lack of availability of low profile 10µF ceramic capacitors.

The efficiency is slightly lower due to the higher series resistance of the low profile inductors. A peak efficiency of 91% for the 1.5V output and 95% for the 2.5V output is achieved with these components, as seen in Figure 7.

Conclusion

The LTC3407 is a dual monolithic, step-down regulator that switches at 1.5MHz, minimizing component costs and board real estate requirements for DC/DC regulators. The small size, efficiency, low external component count, and design flexibility of the LTC3407 make it ideal for portable applications.

Power over Ethernet, continued from page 18

These changes do add diodes to the PD, but it's definitely for the best. Thanks to Auto-MDI-X, today's Ethernet switches and routers work equally well with or without crossover cables. Because the PD now must also accept power of either polarity, 802.3af Power over Ethernet will work with either type of cable, minimizing end user confusion.

The 802.3af standard now defines specific peak currents for class 1 and 2 PDs. While all PDs can draw 400mA of inrush current when they are first powered, current consumption thereafter depends on the class of the PD.

Class 0 and 3 PDs must still never draw more than 400mA peak and 350mA continuous. Class 1 PDs cannot exceed 120mA peak and consume more than 3.84W continuously and Class 2 PDs must limit their peak current to 210mA and continuously use no more than 6.49W. These peak current limits do not require a class 1 or 2 PD to include active current limiting (unless it has more than 180µF of input bypass) as long as its switching regulator stays below the average power limit and filtering keeps peak currents below the specified maximum. While the standard does not specifically address this point, a PD does not have to stay below these peak limits if V_{PORT} suddenly increases. Furthermore, the standard does not allow a PSE to apply a lower active current limit, I_{LIM}, based on a PD's class. A PSE, however, may monitor the PD's current and decide to disconnect it if PD is not staying within the limits of its class, i.e. the PSE may reduce the I_{CUT} threshold for a class 1 or 2 PD.

In addition to the changes listed above there are some minor parametric changes. Refer to the IEEE 802.3af-2003 standard for further details.
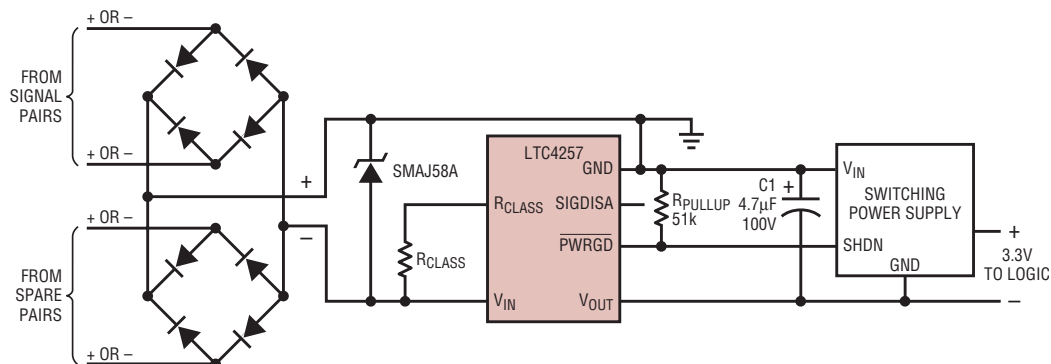

Figure 4. Typical PD application

White LED Driver Minimizes Space, Maximizes Efficiency and Flexibility

by Steven Martin

Introduction

White LEDs are the LCD backlight of choice for portable equipment due to their small profile, exceptional ruggedness and high luminosity. Li-Ion batteries, also rugged and small, are the popular power choice for the same portable equipment. The white LEDs have a nominal forward voltage between 3V and 4V and a Li-Ion battery has a nominal voltage of 3.6V, thus requiring circuitry to step-up the Li-Ion battery's voltage. The problem is, stepping up tends to reduce efficiency, which in turn reduces battery life. The LTC3205 solves this problem by powering up in *direct-connect* mode rather than step up mode. Once powered up, it uses a dropout detector for each white LED to determine if any are running out of drive. As the first white LED just begins to lose current, the chip automatically engages a very powerful 2:3 mode step-up charge-pump. Including 9 precision LED current sources in all, the LTC3205 has enough LED pins and sufficient strength to power a 4-LED main display, a 2-LED sub display and a 3-LED RED, GREEN and BLUE "happy-light".

Figure 1 shows the block diagram of the LTC3205. The chip is controlled by a simple 3-wire serial interface. The 16-bit register provides two control bits for the main display and two control bits for the sub display, giving exponentially-spaced brightness control for each. The remaining 12 bits are divided among the RED, GREEN and BLUE outputs giving 16 shades for each LED and a total of 4096 total colors for the happy light. The RGB LEDs are pulse-width modulated for brightness control while the white LED currents are linearly controlled. A separate logic reference pin (DVCC) allows logic levels from a microcontroller to be supplied at virtually any voltage above or below the battery voltage.

When powered from a Li-Ion battery, the power management section of the LTC3205 connects the LEDs (via the CPO pin) to the battery. Its 2:3 charge-pump only soft-starts when a main or sub display LED has insufficient drive or when the RGB current sources are used. The fractional-ratio charge-pump ensures that the efficiency is high even when the device is in charge-pump mode. The patented constant frequency architecture keeps input noise to a minimum by regulating current on both charge-pump phases.

Two precision servo amplifiers provide inputs to set the reference currents for the LEDs. The main/sub displays and the RGB display are controlled independently for maximum flexibility.
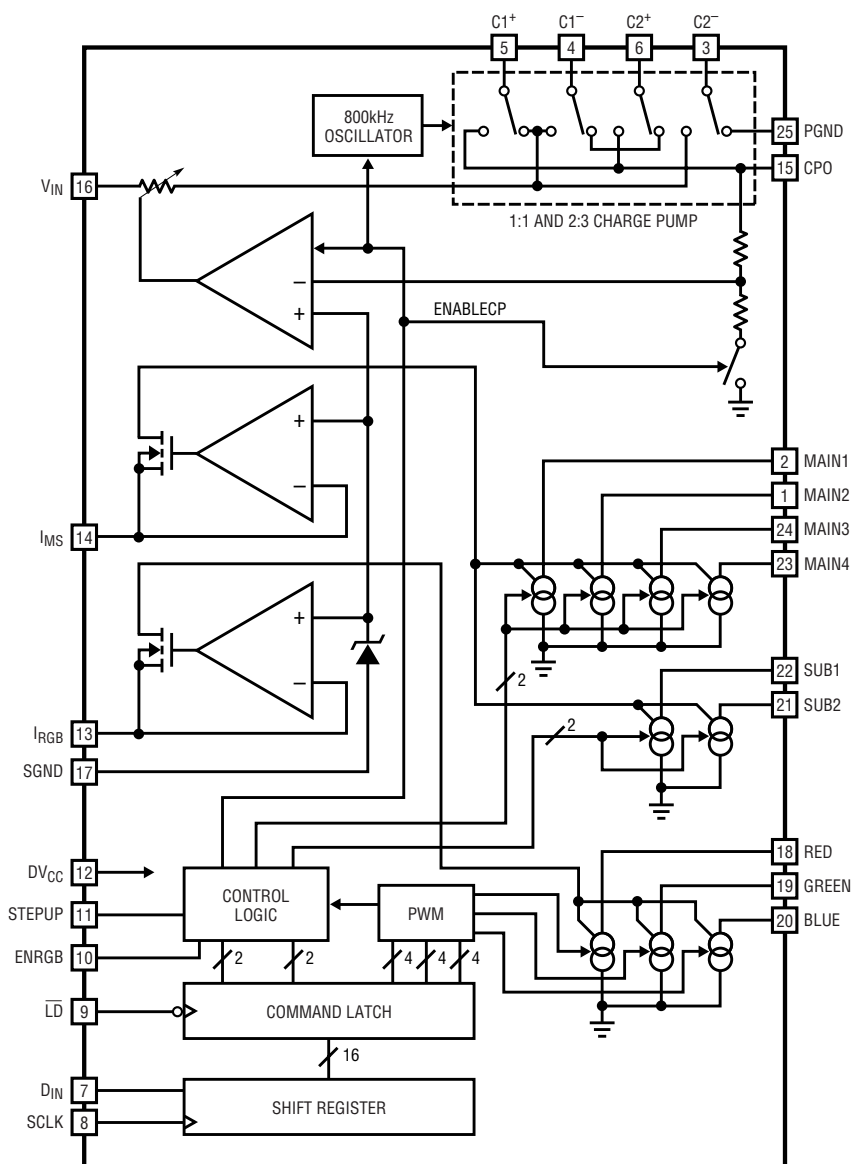

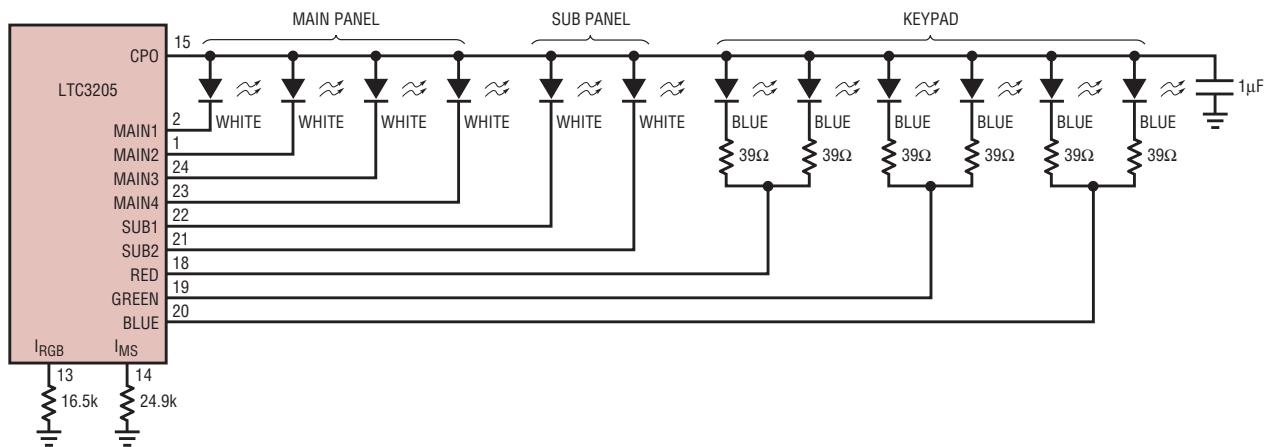**Figure 1. Block diagram of the LTC3205**

Figure 2. 8-LED keyboard display

Flexibility Limited only by Imagination

Because there are so many white LED applications, it's important to arrange each circuit for optimum performance. Given that the LTC3205 has four individual settings for its main display, four individual settings for its sub display and 16 individual settings for each of its color LED pins, the applications it can serve are virtually unlimited.

The LTC3205's primary application provides regulated currents to a 3- or 4-LED main display, a 1- or 2-LED sub display and 4096 colors to an RGB display. Nevertheless, it is possible to arrange the LTC3205 to provide power to an 8-LED keyboard display as shown in Figure 2. Alternatively, it can be used to power a 4-LED camera light as shown in Figure 3.

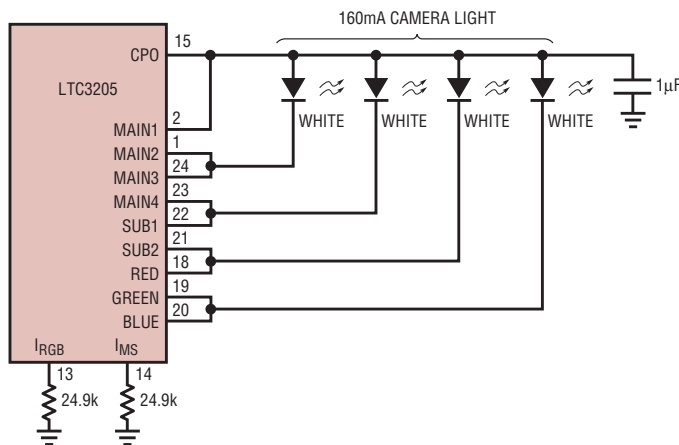Brightness control can be achieved in a number of ways for each of the

Figure 3. 4-LED camera light

displays. The RGB display has 16 built in settings per LED. No external hardware or signals are required. The main and sub displays have four settings each, but these can be easily multiplied by adding a digital control signal to switch a reference resistor in or out as shown in Figure 4. With techniques like this, the number of brightness settings can be increased rapidly to 7 or 13 for the main and sub displays. Brightness can also be controlled by analog means as shown in Figure 5.

Efficiency

Because the LTC3205 only enables its charge-pump as needed, it spends the majority of each battery cycle in direct-connect mode. Since the LED voltages are so close to the battery voltage, true efficiency ($P_{LED}/P_{BATTERY}$) is maximized, as is battery life. Figure 6 shows an example of achievable efficiency as a function of battery volt-

age for a 4-LED application running at 15mA per LED.

To achieve this high level of efficiency, the LED current sources are designed to deliver accurate current with as little as 120mV of compliance voltage. Furthermore, the 0.8Ω pass switch in direct-connect mode drops only 48mV with 60mA of display power.
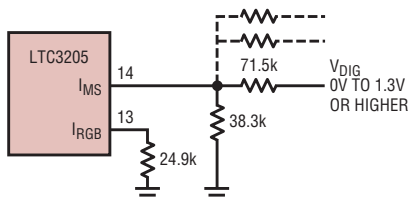
Figure 4. Alternative digital brightness control

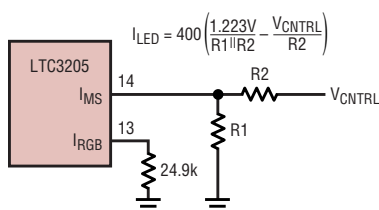$$I_{LED} = 400\left(\frac{1.223V}{R1\|R2} - \frac{V_{CNTRL}}{R2}\right)$$

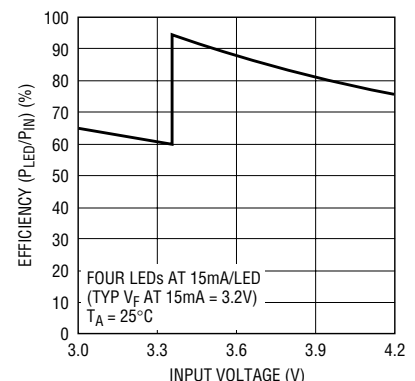Figure 5. Alternative analog brightness control

Figure 6. 4-LED main panel efficiency vs battery voltage

High Input Voltage Monolithic Switcher Steps Up and Down Using Single Inductor

by Jay Celani

Introduction

Ultra-wide input voltage requirements are a common design problem for DC/DC converter applications. When that range includes voltages both above and below the output voltage, a converter must perform both step-up and step-down functions, making the design problem even more complex. A high-voltage input range makes the problem even tougher. These design issues are commonplace in the automotive environment, where

battery powered electronics have to handle everything from cold crank to load dump, a range that can span from 4V to 60V. The requirements of an automotive battery-powered design are somewhat unique, as the operational input voltage is typically relatively well controlled, but an ultra-wide input range must be considered since short-duration events can create extreme input voltage shifts.

There are several common solutions to the step-up/step-down problem.

One solution is to cascade multiple circuits, such as a boost converter followed by a buck converter or an LDO, where the boost converter prevents the output of the step-down converter from dropping out at low input voltages. With high input voltages, the upper bound of the input voltage is directly imposed on the step-down stage, which makes use of an LDO impractical. Cascading a boost converter and high-voltage buck converter will work, but such a topology incurs penalties
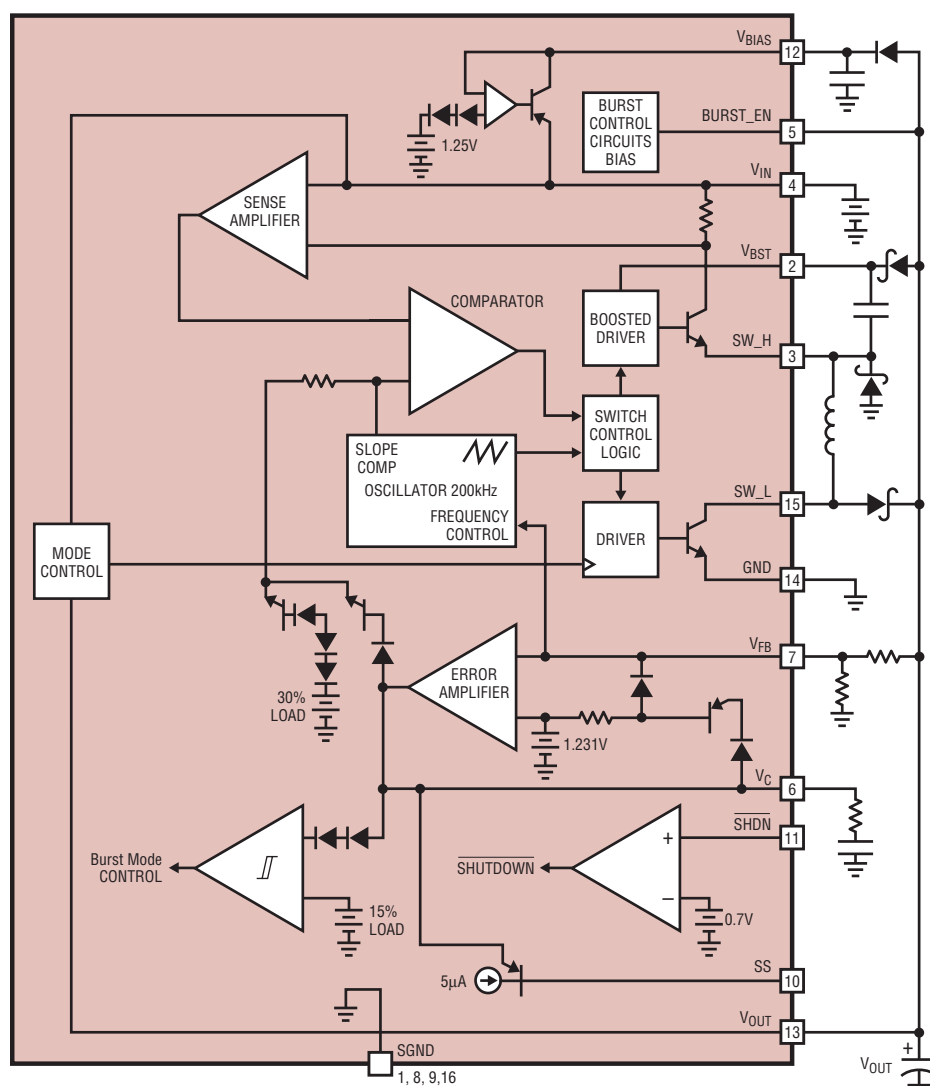

Figure 1. LT3433 block diagram

of complexity, reduced efficiency, and cost. A SEPIC converter is a popular topology for step-up/step-down applications, but a SEPIC converter has inherent drawbacks such as the expense of two inductors, low efficiencies, high switch voltage and current stresses, and high output ripple currents.

Enter the LT3433, a high-voltage monolithic DC/DC converter that incorporates two switch elements, allowing for a unique topology that accommodates both step-down and step-up conversion using a single inductor. When the input voltage is significantly higher then the output, the LT3433 operates in a modified non-synchronous buck configuration using a boosted-drive high-side switch. When the input voltage approaches or falls below the output voltage, the LT3433 activates a ground-referred switch, which creates a bridged switching configuration, or a buck/boost converter, allowing for very low dropout and/or step-up conversion. The LT3433 is primarily intended for use in step-down applications that have transient low voltage input requirements, such as 12V automotive applications that must support a cold-crank condition, where the battery-rail can briefly drop down to 4V. The LT3433 could also be used to significant benefit in certain applications where a SEPIC topology is currently the best option.

What's Inside?

The LT3433 incorporates a 200kHz constant frequency, current mode architecture and can operate with input voltages from 4V to 60V. The LT3433 is packaged in a 16-pin fused TSSOP exposed pad leadframe package, which provides a small footprint and excellent thermal characteristics. An internal 1% voltage reference allows programming of precision output voltages up to 20V using an external resistor divider. A block diagram of the LT3433 is shown in Figure 1.

Burst Mode operation improves efficiencies during light-load conditions. The LT3433 quiescent current drops to ~100µA while in Burst Mode opera-
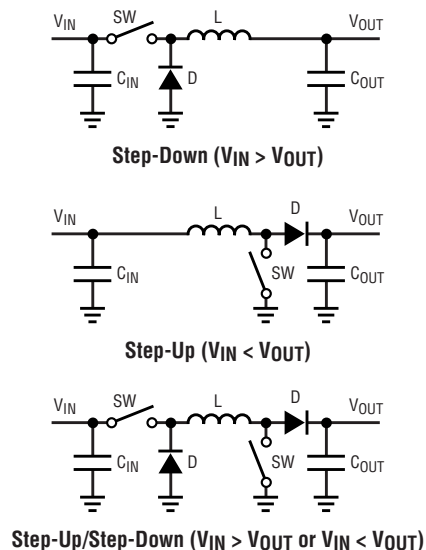
Figure 2. Merging the elements of a buck DC/DC converter topology and a boost DC/DC converter topology form the LT3433 bridged network, enabling buck/boost conversion using a single inductor

tion, minimizing maintenance power for battery powered applications. Burst Mode operation can be disabled by shorting the BURST_EN pin to either the V_{OUT} pin or the V_{BIAS} pin, or by biasing the pin using an external supply. Shorting BURST_EN to ground enables Burst Mode. The LT3433 also has a low-current shutdown mode, reducing quiescent current to ~10µA when the $\overline{SHDN}$ pin is pulled below 0.4V.

The LT3433 uses both current limit and frequency foldback to help control inductor current runaway during startup and short-circuit conditions. A soft-start feature is also included to

reduce output overshoot and inrush currents during startup. Soft-start duration is controlled by a capacitor placed between the SS pin and ground. The LT3433 does not suffer from current limit reduction typically associated with slope-compensation, so switch current limit is unaffected by duty-cycle.

Switching between buck and buck/boost modes of operation is controlled automatically by the LT3433. While in buck mode, if the converter input voltage becomes close enough to the output voltage to require a duty-cycle greater than 75%, the LT3433 enables a second switch during the "switch on" time, which pulls the output side of the inductor to ground. This bridged-configuration switching operation allows voltage conversion to continue when V_{IN} approaches or is less than V_{OUT}.

Bridged Topology

In the simplest terms, a buck DC/DC converter switches the V_{IN} side of the inductor, while a boost converter switches the V_{OUT} side of the inductor. The LT3433 bridged topology merges the elements of buck and boost topologies, providing switches on both sides of the inductor, as shown in Figure 2. Operating both switches simultaneously achieves both step-up and step-down functionality.

Maximum duty-cycle capability (DC_{MAX}) gates the dropout capabilities of a buck converter. As $V_{IN} - V_{OUT}$ is
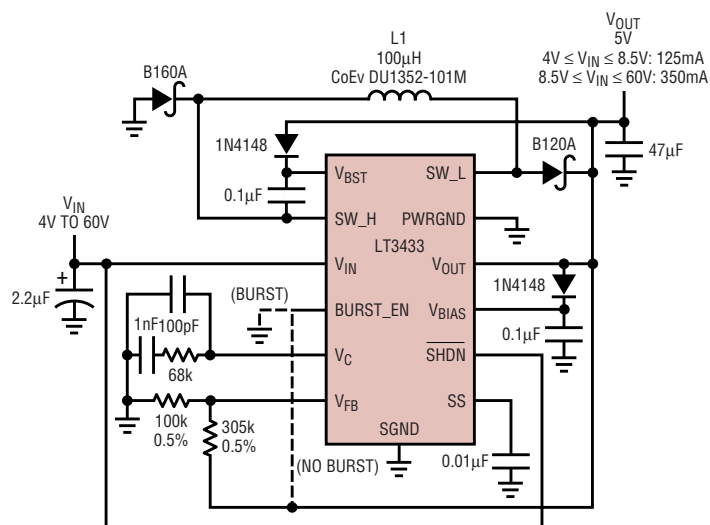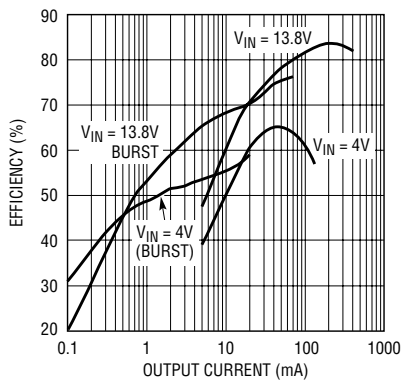
Figure 3. 4V–60V to 5V converter

Figure 4. Conversion efficiency of the 4V–60V to 5V converter shown in Figure 3

Figure 5. Maximum output current vs V_{IN} for the 4V–60V to 5V converter shown in Figure 3

reduced, the required duty cycle increases toward DC_{MAX} until the limit of the converter is reached, and the converter loses regulation. With a second switch bridging the switched inductor between V_{IN} and ground, the entire input voltage is imposed across the inductor, which reduces the duty cycle required to maintain regulation. Using this topology, regulation is maintained as V_{IN} approaches or drops below V_{OUT}.

4V–60V Input to 5V Output Automotive Converter

A 4V–60V to 5V converter is shown in Figure 3. This design is well suited to 12V automotive applications where output regulation is required with battery line voltages from 4V cold crank through 60V load dump. The input voltage threshold for bridged mode
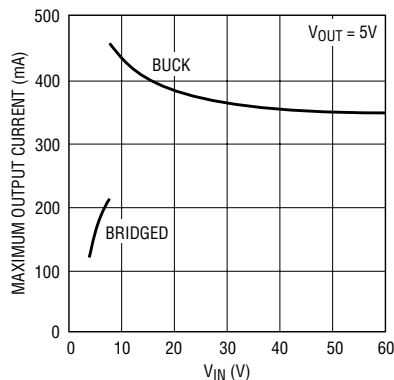
operation is near 8V, so the converter operates primarily in buck mode, except during a cold crank condition. This converter accommodates loads up to 400mA and produces efficiencies greater than 83% when operating with a nominal 13.8V input. Conversion efficiencies with V_{IN} = 4V and V_{IN} = 13.8V in both burst-enabled and burst-disabled configurations are shown in Figure 4.

During a cold-crank condition, where the battery line voltage drops below 8V, the converter switches into buck/boost mode to maintain output voltage regulation. Because the LT3433 switch current limit is fixed, converter load capability is reduced while operating as a buck/boost converter. Output current capability vs. input voltage is shown in Figure 5.
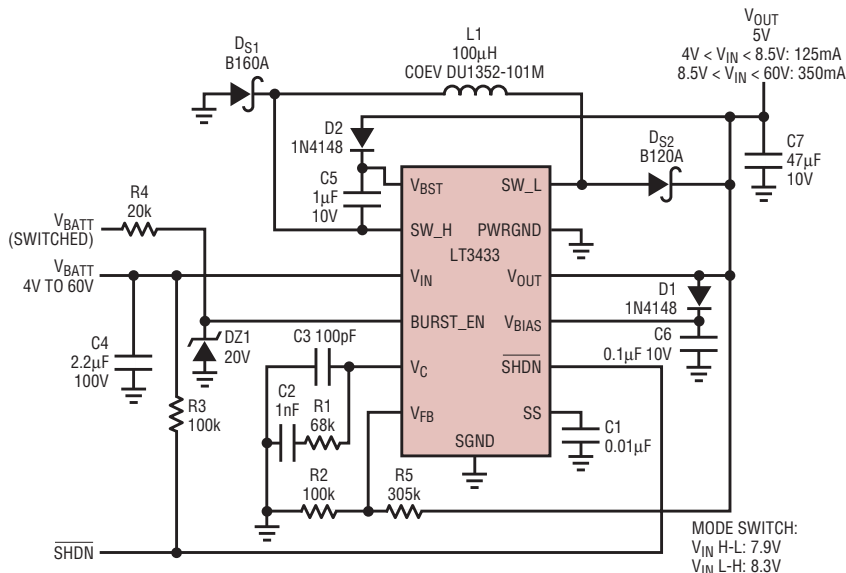
With an input of 4V, the converter accommodates loads up to 125mA.

It is important to use low-V_F Schottky diodes in a LT3433 converter design. Minimizing the forward voltages of the external catch and forward diodes directly reduces operational duty cycle, which increases output current capability, especially during bridged switching. Reduced Schottky forward voltages also increase operational efficiency, which further increases available output current capability. The B120/160 diodes used are a good compromise between size and low V_F. An inductor with low series resistance also helps to maximize converter efficiency and performance.

In maintenance applications, reduced Q-current operation is desired for light-load and no-load conditions. This is easily accomplished by shorting the BURST_EN pin to SGND to enable Burst Mode. In certain low-current applications, however, the IC could enter burst operation during normal load conditions. If the additional output
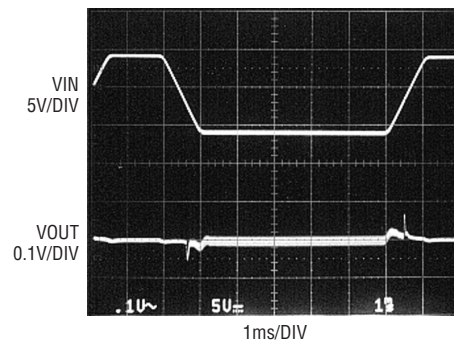

Figure 7. 4V–60V to 5V converter output characteristic (AC coupled) during a 13.8V to 4V 1ms V_{IN} transition with 125mA output load
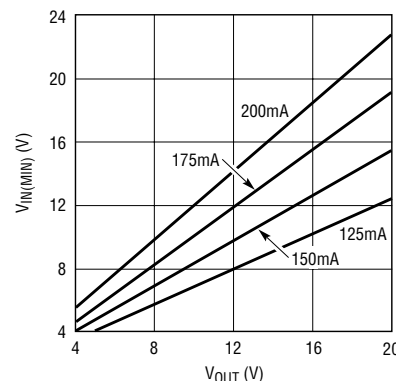

Figure 8. Typical LT3433 converter minimum input voltages vs V_{OUT} for various maximum load currents

Figure 6. 4V–60V to 5V converter with switched Burst Mode enable and shutdown
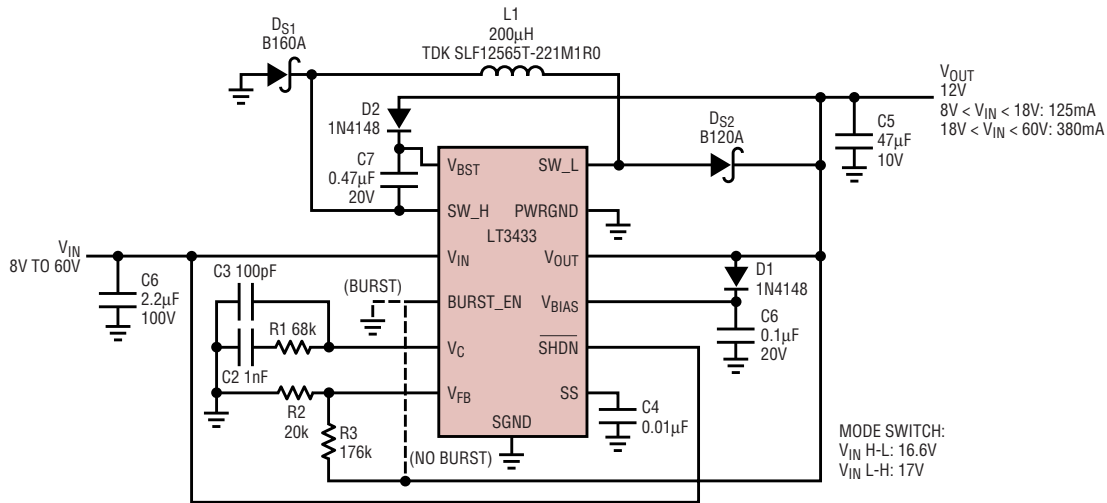
Figure 9. 8V–60V to 12V converter

ripple and noise generated by Burst Mode operation is not desired for normal operation, BURST_EN can be biased using an external supply that is disabled during a no-load condition. This prevents entering Burst Mode operation during normal operation, and enables Burst Mode operation only when it is required. The 4V–60V to 5V automotive converter shown in Figure 6 incorporates a dynamic Burst Mode function controlled by a switched battery input, and also accommodates a user-enabled shutdown feature.

Not only does this LT3433 converter operate across a large range of DC input voltages, it also maintains tight output regulation during input transients. When subjected to a 1ms 13.8V to 4V input transition to simulate a cold crank condition, regulation is maintained to 1% with a 125mA load, as shown in Figure 7.

Increased Output Voltages

The LT3433 can be used in converter applications with output voltages from 3.3V through 20V, but as converter output voltages increase, output current and duty cycle limitations can prevent operation with V_{IN} at the extreme low end of the LT3433 operational range. When a converter operates as a buck/boost, the output current becomes discontinuous, which reduces output current capability by roughly a factor of $(1 - DC)$, where DC = duty cycle. As such, the output current requirement dictates a minimum

input voltage where output regulation can be maintained. Figure 8 shows typical minimum input voltages as a function of converter output voltage and required load current.

8V–60V to 12V Converter

The 8V–60V to 12V converter shown in Figure 9 can provide output current up to 125mA with inputs as low as 8V. This is suitable for 12V automotive applications without cold-crank requirements, as well as many other applications such as those powered by inexpensive wall adapters. This converter typically switches operational modes at 17V and operates in buck mode with higher input voltages. This LT3433 converter accommodates loads up to 435mA and produces efficiencies above 89% when operating with a 20V input. Conversion efficiencies with $V_{IN} = 8V$ and $V_{IN} = 20V$ in both

burst-enabled and burst-disabled configurations are shown in Figure 10. Output current capability vs. input voltage is shown in Figure 11.

Conclusion

The LT3433 simplifies the design of ultra-wide input range DC/DC voltage converters, and is particularly suited for step-down applications that require short-duration step-up conversion. Automatic transitioning between buck and buck/boost modes of operation provides seamless output regulation over wide input voltage ranges and during input voltage transients. The outstanding thermal characteristics of the TSSOP package make the LT3433 usable in harsh environments, and the small-footprint package, use of a single inductor, and few external components provide board space efficient solutions. _LT_
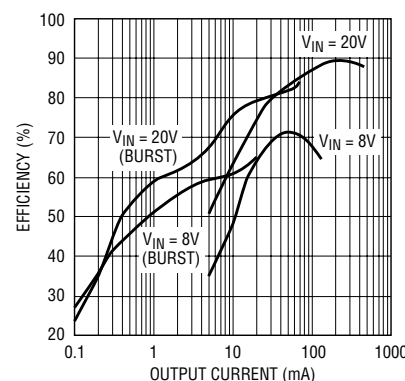

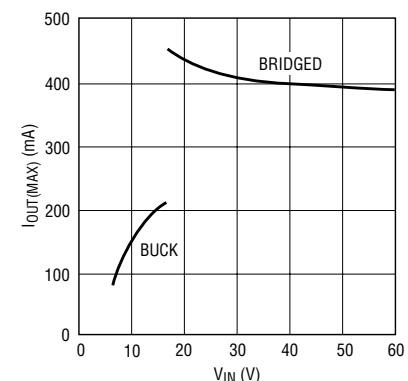**Figure 10. Conversion efficiency of the 8V–60V to 12V converter**

Figure 11. Maximum output current vs V_{IN} for the 8V–60V to 12V converter

Hot Swap Controller Enforces Tracking in Split Supply Systems

by Ted Henderson

Introduction

Split power supplies are widely used in audio, video and data communication systems. These systems typically use ±5V, ±12V or ±15V supply voltages and require a wide range of operating currents. The LT4220 Hot Swap controller—which operates over any combination of split supplies ranging from ±2.7V to ±16.5V—allows a circuit board to be safely inserted or removed from a live backplane without glitching the power supplies while controlling load currents from milliamps to amps.

Glitches can cause anything from objectionable "pops" in audio systems, data loss in digital systems or even connector damage. Pops can also originate from shifting bias points or complementary stages wherein half of the circuit is correctly powered and the other half has not yet been powered.

The LT4220 offers the usual Hot Swap features, such as limiting inrush current to the local supply bypass capacitors and isolating faults from the system supply should they occur, but it also coordinates voltage tracking of the split supplies. Tracking ensures that both the positive and negative supplies power-up either coincidently or ratiometrically, thereby eliminating glitch and pop problems. This complete split supply Hot Swap control system is packaged in a small 16-lead SSOP plastic package.

The LT4220

The LT4220 contains two independent, yet coupled, Hot Swap controllers, one for the negative supply and one for the positive supply. The control action is carefully coordinated such that the supplies turn on together, turn off together and in the case of an over-current fault, both outputs are tripped off simultaneously. Best of all, the LT4220 enforces active tracking between the two supplies during power-up to ease the design requirements of the split supply circuitry and eliminate abnormal circuit behavior arising from asymmetrical supply ramps.

The LT4220 provides other important Hot Swap features, including input voltage monitors, output voltage monitors, a circuit breaker with selectable automatic retry, timed current limiting with foldback, and gate drives for N-channel MOSFET devices to be used on both the negative and positive supplies.

Basic Operation

Figure 1 shows a simplified block diagram of the LT4220. The inputs are monitored and power-up is not started until both are good. The outputs are monitored and PWRGD signals when both are good. Tracking monitors the outputs via the FB pins and controls the gate drives to assure correct power-up. N-channel MOSFETs are used on both supplies, eliminating the need for complementary devices. FAULT indicates when a current limit condition has caused the timer to time out. Connecting FAULT back to ON+ enables automatic retry. Ramp rates are adjusted by gate capacitors and associated gate charging currents. Nevertheless, when track is enabled the actual rate is no faster than the slowest ramp.

Typical Hot Swap Application

Figure 2 shows a complete circuit design for a ±12V, 10A Hot Swap circuit using the LT4220. Q1 and Q2 N-channel MOSFET devices control the ±12V output power-up profiles after insertion. Resistors R_S^+ and R_S^- sense the load current, enabling the LT4220 to protect against temporary overloads and short circuits. R5 and R7 prevent high frequency parasitic oscillations sometimes associated with power MOSFET devices operating in their linear regions. The amount of inrush current is set by the appropriate choice of C1 and C2. In this case the inrush current is limited to approximately 100mA for a 100µF load capacitance. In case of an output short circuit, both Hot Swap channels incorporate timed current limiting with foldback to protect the MOSFET devices against over-dissipation, and
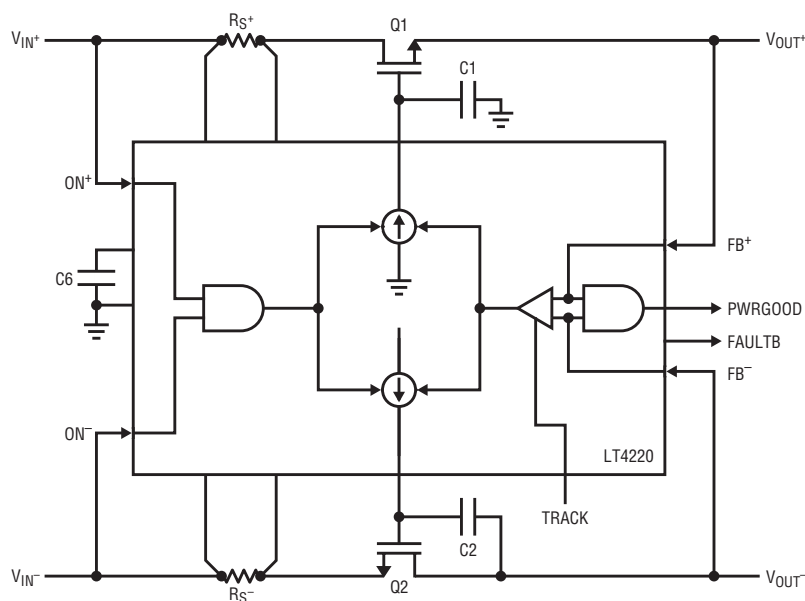

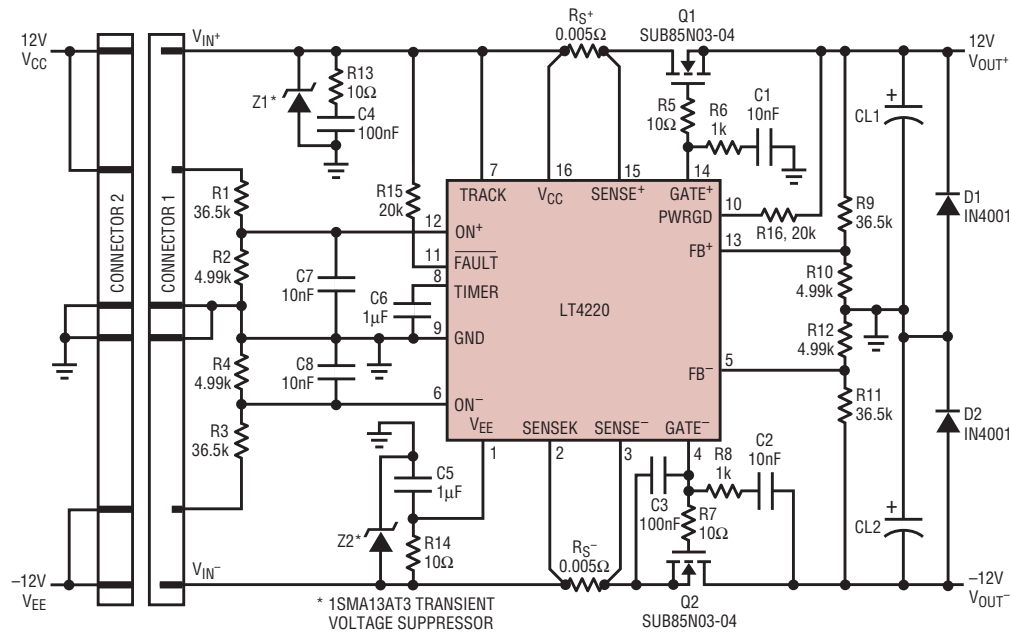Figure 1. LT4220 Simplified block diagram
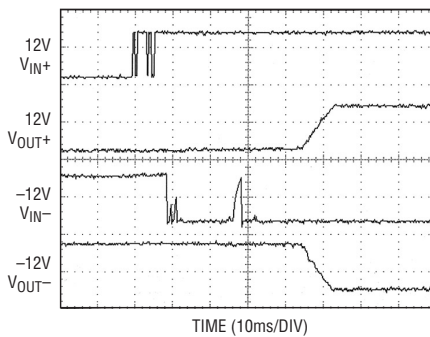
Figure 2. LT4220 ±12V, 10A Hot Swap controller

Figure 3. Power-up sequence

disconnect a faulted circuit from the backplane. Foldback is especially valuable in difficult circumstances such as start up into a 0Ω short circuit, where simple protection schemes may not be sufficient to protect the output MOSFET devices. Resistive divider ratios for R1/R2 and R3/R4

were chosen to enable the GATE drive outputs when both input supplies are within 15% of their final value. Resistive divider ratios for R9/R10 and R11/R12 were chosen to indicate that the output power was good when both outputs are within 15% of their final value. The 15% value was chosen assuming that the system power supply tolerances were ±10%.

Power-Up Sequence

Bouncing contacts and voltage glitches during board insertion wreak havoc with sensitive analog circuitry powered by split supplies. The LT4220 eliminates all of these issues (the results shown in Figure 3). After the ON+ and ON− pins exceed their undervoltage lockout thresholds, the gates of Q1 and Q2 (GATE+, GATE−) are pulled

up by the internal current sources. For large capacitive loads the inrush current is limited by the gate slew rate or by the foldback current limit. For a desired inrush current that is less than the foldback current limit, the feedback capacitors C1 and C2 can be used to control the output voltage slew rates by integrating the gate pullup currents. Once both output supply voltages exceed their power good thresholds and the MOSFETs Q1/Q2 are fully enhanced, the PWRGD signal is released and pulled high by R16 (Figure 2).

Supply Tracking

When the TRACK pin is connected to V_{IN}^+, track mode is enabled. The function of this mode is to control the GATE+ and GATE− pullup currents
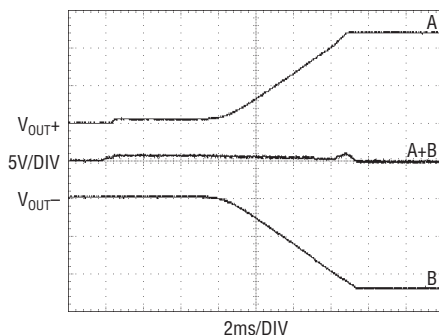

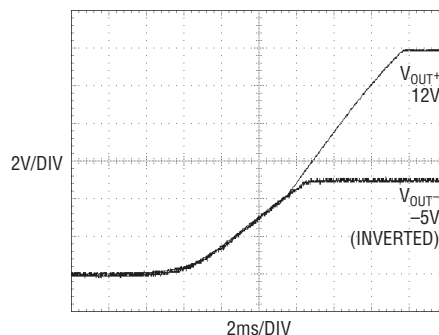
Figure 4. ±12V coincident supply tracking

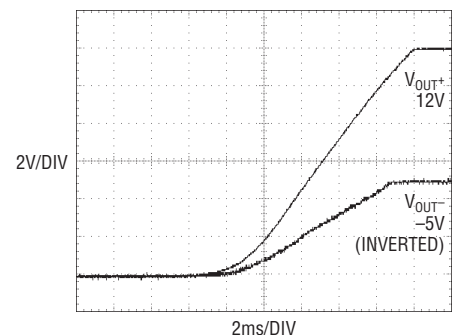Figure 5. +12V, −5V coincident supply tracking (−5V signal inverted)

Figure 6. +12V, −5V ratiometric supply tracking (−5V signal inverted)

such that the desired output voltages ramp characteristic is achieved. The gate pullup currents are controlled via the FB$^+$ and FB$^-$ pins.

Figure 4 shows coincident tracking for a system operating with +12V and –12V supplies as per the circuit in Figure 2. The circuit in Figure 2 is easily converted to work with –5V and +12V supplies by simply changing R3, R9 and R11 to 12.4kΩ. The new coincident tracking behavior is shown in Figure 5. Ratiometric tracking is sometimes preferable, especially in signal processing applications. Figure 6 shows this mode of operation, obtained by changing only R3 and R11 to 12.4kΩ. Note that in this case the supply ramps are made to start and finish at the same time.

Short-Circuit Protection

Current limiting provides protection for the output MOSFET devices. The current limit for either supply is set by sense resistors R_S^+ and R_S^- (Figure 2). The voltage across the sense resistor is regulated by the current limit circuitry to 50mV for conditions where foldback current limiting is not enabled. The

TIMER pin provides a means for setting the maximum time the LT4220 is allowed to operate in current limit. Whenever the current limit circuitry becomes active, by either the positive or negative sense amplifier operating in current limit, a pull-up current source of 60uA is connected to the TIMER pin and the voltage rises with a slope of dV/dt = 60µA/C_{TIMER}. If the overload is removed, a small 3µA pulldown current slowly discharges the timer pin. If the timer succeeds in charging to a 1.24V threshold, an internal fault latch is set and the $\overline{FAULT}$ pin is pulled low. Both MOSFETs are quickly turned off while the TIMER pin is slowly discharged to ground.

The power dissipation will be high in the output MOSFET devices when the output is shorted with zero ohms. To prevent excessive power dissipation in these pass transistors the current limit on each supply is reduced as the output voltage falls. This characteristic, commonly referred to as "current foldback", reduces the fault current as the output voltage drops and reaches the lowest level into the short. The foldback current limiting reduces

short circuit MOSFET dissipation by a factor of 2.5. The FB± pins effectively measure the MOSFET V_{DS} voltage and control the appropriate current limit sense amplifier input offset to provide the foldback current limit.

Automatic Restart

Normally the LT4220 latches off in the presence of a fault. Nevertheless, by removing R15 in Figure 2, you can connect the $\overline{FAULT}$ and ON$^+$ together to enable automatic restart. $\overline{FAULT}$ pulls the ON$^+$ pin low allowing an automatic restart to be initiated once the TIMER pin ramps below 0.5V.

Conclusion

The LT4220 combines all of the functions necessary for split supply Hot Swap control in one small 16-lead SSOP plastic package. This device is adaptable to applications covering a wide range of positive and negative supply voltages, ramping profiles, capacitance and load currents, including optical/laser, audio and ECL systems. *LT*

Conclusion

Though crystal based oscillators have dominated the timing and clocking market for many years, the LTC6903 (I^{2}C) and LTC6904 (SPI) offer solutions that are smaller, more flexible, more

robust and lower power. Selecting a frequency from the 1kHz–68MHz frequency range is simple through the serial ports, and both devices operate over a wide range of supply voltages. *LT*

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Both of these features are required to keep the LTC3205 in direct-connect mode as long as possible.

Conclusion

The LTC3205, designed specifically for portable backlighting applications, provides all of the necessary current

regulation, power circuitry and control logic to deliver efficient and accurate power to a large number of LEDs in a portable product. To further reduce board level complexity, it uses only four 0603 sized ceramic capacitors keeping the total solution height under 1mm. A straightforward serial interface re-

duces the number of wires needed to control all of the LEDs. Given its feature set, the LTC3205 packs an amazing amount of backlighting horsepower, flexibility and performance into a very small 4mm × 4mm footprint. *LT*

Voltage Margining Made Easy

by Jeff Heath

Introduction

Linear Technology has introduced two devices that simplify supply margin testing and are particularly well suited for multiple power supply applications. The LTC2920-1 is a single power supply margining controller packaged in a 5-lead SOT-23. The LTC2920-2 is a dual power supply margining controller packaged in an 8-lead MSOP. Both parts provide an easy and accurate way to accomplish onboard power supply margining with a minimum of design time and board space.

What is Voltage Margining?

High performance and high reliability systems typically require end-of-line testing, or include automated self-testing, to assure rated performance with the supply voltage at the upper and lower limits of its regulation band. This

Figure 1. Typical voltage margining waveforms

testing is often called "supply margining" or "voltage margining." The testing is typically accomplished by forcing the power supply modules or DC/DC converters in the system to ±5% of their nominal voltage. Once the supply voltage has settled at the margined voltage, the system performance can be evaluated. Figure 1 shows typical rise and fall times for voltage margining waveforms.

Typical Applications

Figure 2 shows how the 5-lead SOT-23 LTC2920-1 controls a LTC1435A switching regulator by sourcing or sinking current at the feedback pin. This margining solution takes fewer components, less board space, and less design time than the traditional approach of using resistors, switches, and level shifters. Figure 3 shows the LTC2920-1 controlling a DC/DC converter module. In this case, current is forced into or out of the trim pin on the module, causing it to raise or lower its output voltage accordingly.

Easy to Use, Easy to Connect

The LTC2920-1 uses only three pins to setup and control the margining of a power supply: the I_M current pin, the current selecting pin R_S, and the control pin IN. The feedback node or

trim pin of the power supply to be margined is connected to the I_M pin. The margining current is selected with a single resistor, R_{SET}, connected to the R_S pin. The R_{SET} resistor can program the margin current over a 400:1 range from 5µA to 2mA. The control input is a three-state signal: LOW to margin down, HIGH to margin UP, and FLOAT to allow the power supply to regulate at its nominal voltage. The only other pins are power and ground. The LTC2920-2 has an additional independent margining channel, adding a second set of I_M, R_S, and I_N pins.

The LTC2920-1 uses less than 14mm^2 of application board space, and the LTC2920-2 uses less than 27mm^2 (Figure 4). These numbers include the current setting resistors and the LTC2920's power supply bypass capacitor.

How It Works

Feedback Circuits

The LTC2920 provides symmetric power supply margining by taking advantage of the architecture common to most power supplies. Most regulated power supplies rely on feedback and gain to maintain power supply output voltages. Even complicated multi-phase switching power supplies can typically be modeled as a simple amplifier with a voltage reference and two feedback resistors (Figure 5). The
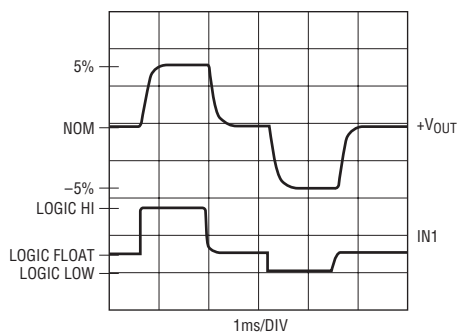

Figure 2. Voltage margining a switching power supply
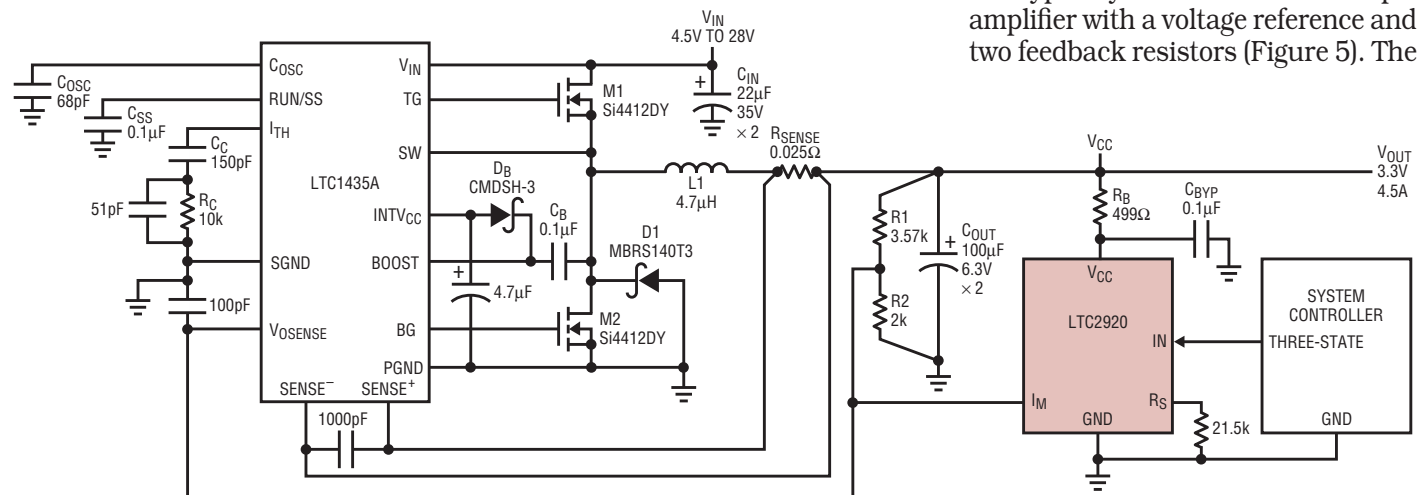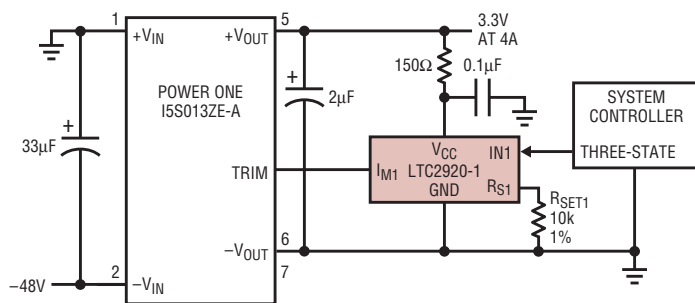
Figure 3. DC to DC converter voltage margining

Figure 4. Dual power supply voltage margin controller occupies less than 27mm^2

LTC2920 creates a delta voltage across the feedback resistor R_F by sourcing or sinking current from the feedback node. Here's how it works:

Knowing the value of the resistors R_F and R_G, and the voltage of V_{REF}, V_{PSOUT} can be calculated from the basic op amp feedback equation:

$$V_{PSOUT} = V_{REF} \bullet [1 + (R_F/R_G)]$$

Since the op amp keeps its inverting terminal equal to the noninverting terminal, the voltage at the inverting terminal between R_F and R_G is V_{REF}. There is no significant current flowing into or out of the op amp inputs, so:

$$I_F = I_G = V_{REF}/R_G$$

Knowing that this current flows in the feedback resistor network, V_{PSOUT} can be alternately calculated by:

$$V_{PSOUT} = V_{REF} + (I_{FB} \bullet R_F)$$

This equation is in a form which is helpful for understanding how the LTC2920 changes the power supply output voltage. Figure 6 shows the simplified model with the LTC2920 added. As before, the op amp keeps the voltage at its inverting input at V_{REF}. If we add or subtract current at this node, the delta current is always added to or subtracted from I_{FB}, and never I_{RG}. Because of this, the voltage across R_F is:

$$V_{RF} = (I_{FB(NOM)} \pm I_{MARGIN}) \bullet R_F$$

or

$$V_{RF} = (I_{FB(NOM)} \bullet R_F) \pm (I_{MARGIN} \bullet R_F)$$

When added to the nominal voltage at the feedback pin V_{REF}, the power supply output becomes:

$$V_{POSOUT} = V_{REF} + (I_{FB(NOM)} \bullet R_F) \pm (I_{MARGIN} \bullet R_F)$$

This is the nominal power supply output voltage, plus or minus the margining current, I_{MARGIN}, supplied by the LTC2920 times the feedback resistor R_F:

$$V_{PSOUT} = V_{POSOUT(NOM)} \pm (I_{MARGIN} \bullet R_F)$$

Note that the delta voltage V_{MARGIN} depends only on I_{MARGIN} and R_F, and not R_G or V_{REF}.

Simple Design: Calculate the Value of One Resistor

There is one resistor value to calculate when designing in the LTC2920 for voltage margining applications: the current setting resistor R_{SET}. To calculate this value, there are only two things the designer needs to know: the amount of voltage to margin the power supply, V_{MARGIN}, and the value of the feedback resistor of the margined power supply, R_F.

The value of the current setting resistor can then be determined by calculating the desired I_{MARGIN} current sourced or sunk by the LTC2920:

$$I_{MARGIN} = V_{MARGIN} / R_F$$

The value of the current setting resistor is then:

$$R_{SET} = 1V/I_{MARGIN}$$
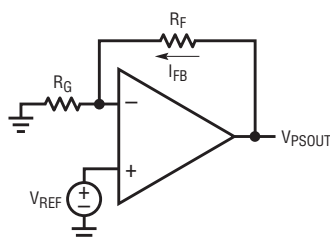
And in its simplest form:

$$R_{SET} = R_F / V_{MARGIN}$$

No Access to the Feedback Pin? No Problem

DC to DC power supply modules typically do not provide access to the feedback pin directly, but DC to DC power modules often have a trim pin. In this application, the LTC2920 operates by sourcing and sinking current out of the trim pin on the power supply being margined. Calculation of the R_{SET} resistor is slightly more complicated than the case described above, requiring a bench measurement to be made on the DC to DC power supply module. See the LTC2920 data sheet for details on the operational details and how to calculate the R_{SET} resistor.

Conclusion

The LTC2920-1 and LTC2920-2 Power Supply Margining Controllers provide a cost effective way to add self-testing capability to high performance and high reliability systems. They are easy to design with easy to interface to. Both parts have the ability to control power supplies with either feed back nodes, or trim pins. With printed circuit footprints of less than 14mm^2 and 27mm^2, the LTC2920-1 and LTC2920-2 respectively provide versatile power supply margining with a minimum impact on PCB space. *LT*

Figure 5. Simplified power supply model

Figure 6. Simplified power supply model with voltage margining

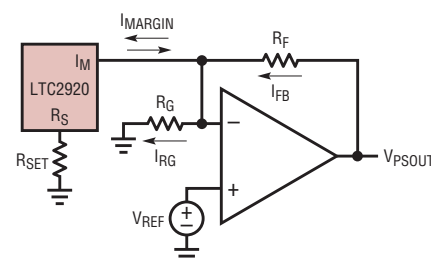# Buck DC/DC Controller Achieves High Efficiency over Four Decades of Load Current

by Mark Vitunic

Introduction

The impressive efficiency of a buck DC/DC regulator at the upper end of the load current range often overshadows its low- or no-load current performance. Efficiency numbers at the lower end of the load spectrum can be misleading. Zero load current means zero power out and therefore zero efficiency, but if the output voltage must remain in regulation even at no load, then the no-load quiescent current—not efficiency—of the regulator is the important limiting factor in battery life. Burst Mode operation makes it possible for the LTC3801 buck DC/DC controller to achieve high efficiency over a wide range of load currents (greater than 10,000: 1), and yet it consumes only 16µA of input DC supply current under no-load conditions.

The LTC3801 includes many of the features expected in a high-performance switcher: high efficiency

Figure 1. Compact 2.5V, 2A buck regulator

(up to 94%), wide V_{IN} range (2.4V to 9.8V), high constant frequency operation (550kHz), and current mode control for excellent AC and DC line and load regulation. The LTC3801 provides ±1.5% output voltage accuracy. It consumes only 195µA of quiescent current in normal operation (dropping to 16µA under no-load conditions) and only 6µA in shutdown. The device incorporates a fixed internal soft start to limit in-rush currents. The LTC3801 is offered in a tiny low-profile (1mm) SOT-23 package.

2.5V/2A High Efficiency Micropower Step-Down DC-DC Regulator

Figure 1 shows the LTC3801 regulating a 2.5V/2A output. Figure 2 shows the efficiency of this circuit at various input voltages. Efficiencies up to 93% are achieved at higher currents while still maintaining good efficiency at lighter currents. Even at a load current of only 200µA, a full four decades below the maximum load current of 2A, the LTC3801's efficiency beats an "ideal" linear regulator with the same input voltage.

Powered from a Li-Ion battery, the circuit of Figure 1 sips a mere 17.5µA of input current at 4.2V. This is significantly less than the self-discharge rate of a typical Li-Ion battery of standard capacity. This feature allows for con-

"Even at a load current of only 200µA, a full four decades below the maximum load current of 2A, the LTC3801's efficiency beats an "ideal" linear regulator with the same input voltage."

tinuous operation from a Li-Ion battery without the need to shut down and start up (as load conditions change) to save battery life. This is critical in handheld applications where the device may be idle, but not off, for much of the time, and calls for several amps when active. ☐☐
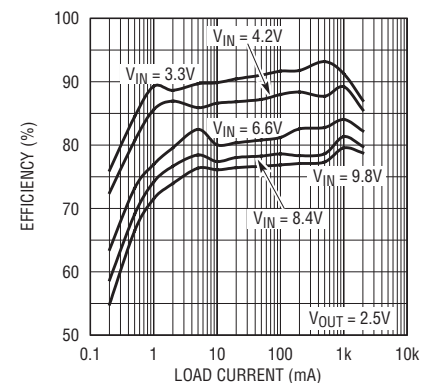
Figure 2. The regulator shown in Figure 1 achieves high efficiency over four decades of load current—an important feature for conserving batteries in portable applications.

For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

Single IC Monitors Redundant –48V Supplies and Fuses without Precision External Components

by Brendan Whelan

Introduction

Reliability is a top priority for the designers of modern telephone and communications equipment. Designers take extra care to protect circuitry from failure by employing redundancy whenever possible, especially for power supplies. Supply voltages and fuses are monitored for early warnings of impending failure, often via a complicated array of precision components. The resulting circuits are expensive in terms of component cost, board space

and engineering time. The LTC1921 replaces complicated monitoring systems with a simple, yet versatile, integrated precision monitoring system contained entirely in an MSOP–8 or SO–8 package.

LTC1921 is a high precision, all-in-one monitor for redundant –48V supplies. This device is the only fully integrated dual –48V supply monitor that meets common telecom specifications for supply range warning and

can also withstand the high transient voltages required by telecom systems. Using a second LTC1921, dual –48V systems which have both –48V supply and return diodes and fuses on the same card can be monitored. The LTC1921-based circuits described in this article can be used to monitor a complete redundant 4-diode –48V supply system with guaranteed precision with just a few external components.

How it Works

The LTC1921 monitors supply voltages by dividing the voltage internally and comparing the result to an internal precision reference. No precision external components are required, thus ensuring maximum accuracy while simultaneously reducing component cost, board space and engineering requirements. The LTC 1921 has telecom industry accepted preset voltage thresholds including undervoltage (–38.5V), undervoltage recovery (–43V) and overvoltage (–70V). The overvoltage threshold has a 1.3V hysteresis that defines the overvoltage recovery threshold. These thresholds are factory trimmed to meet the exacting requirements common to most power supply specifications. This eliminates the need to calculate the aggregate error of discrete components (i.e. the otherwise required separate reference, multiple comparator offsets, and resistors).

The LTC1921 is designed to indicate proper supply status over a wide range of conditions. In order to accomplish this, the internal architecture is symmetrical. The LTC1921 is powered via the supply monitor input pins, V_A and V_B. Supply current can be drawn from either or both pins, so the device can operate properly as long as at least one supply is within the operating
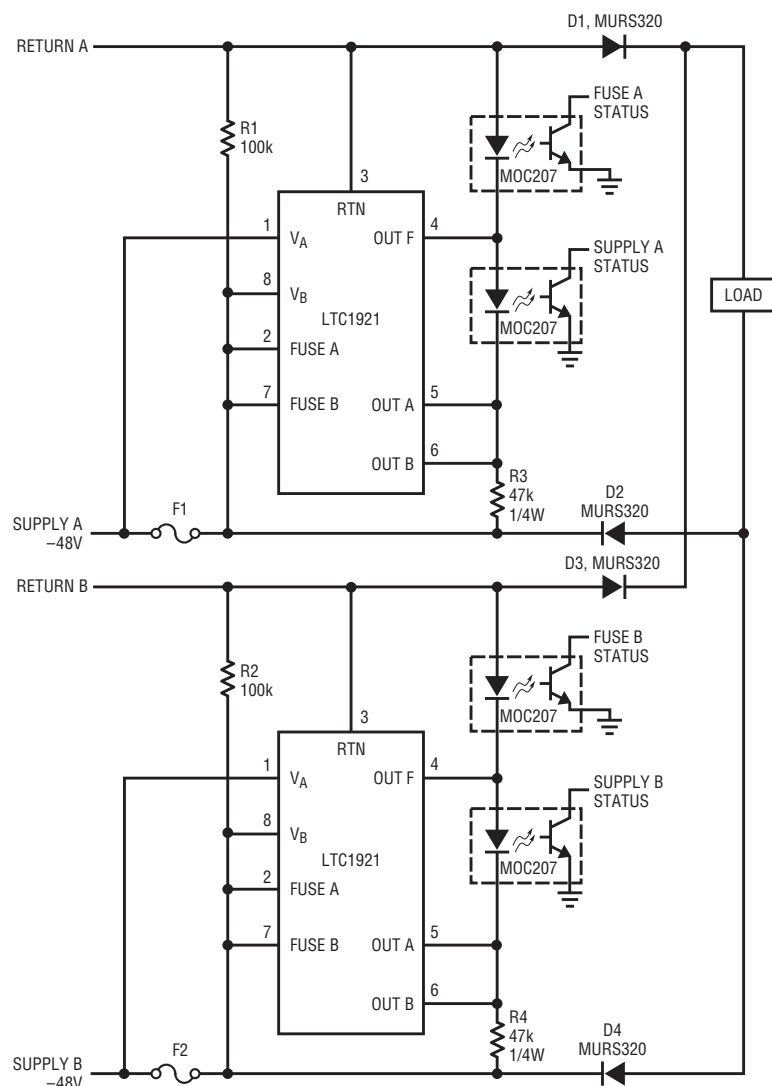

Figure 1. An LTC1921 monitors each supply at the card edge in a 4-diode application
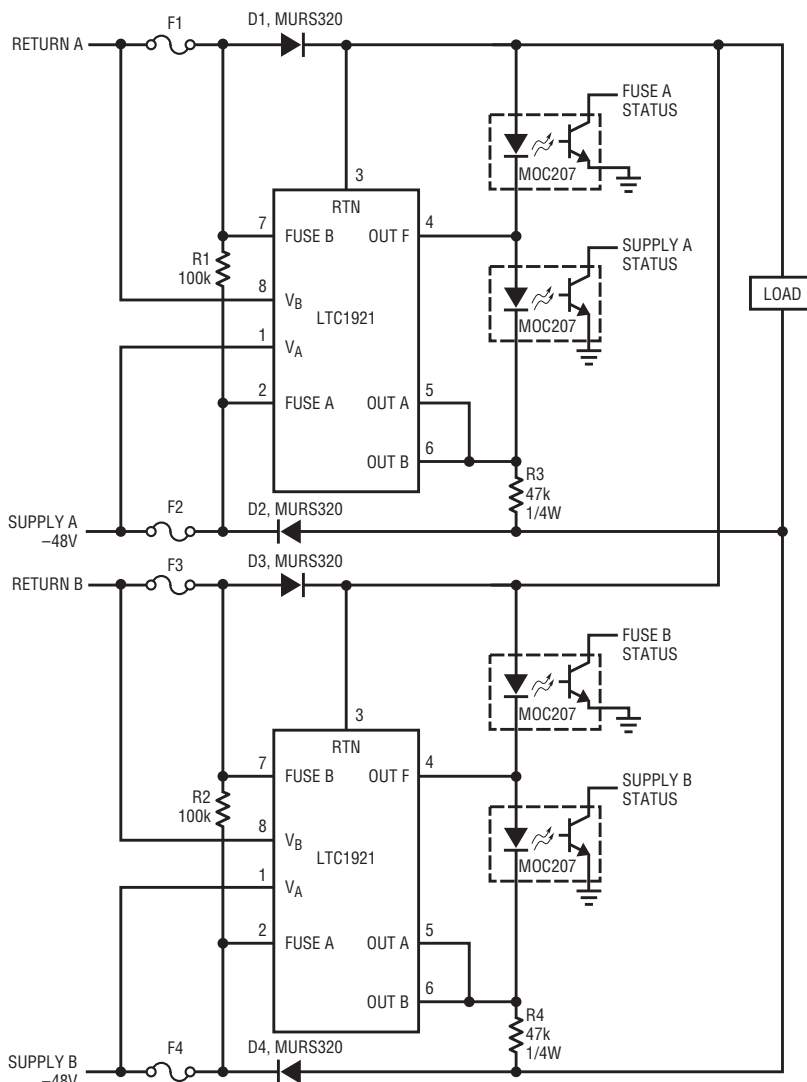
Figure 2. Two LTC1921s monitor supply voltages, plus supply and return fuses for redundant –48V supplies

the individual supply and return signals, the monitors are able to compare the supply voltages at the card edge without the diode drop of the return ORing diode. This circuit essentially duplicates the output circuitry, so that there are four outputs, each with a separate optoisolator. The outputs of the optoisolators may be combined in AND or OR fashion, but all four are required. In this circuit, if either supply voltage falls out of spec, its respective indicator changes to a warning state. If a fuse opens or the supply fails entirely, then all indicators for that supply indicate a warning.

Figure 2 shows a slightly different approach. Each RTN pin in this case is wired to the combined return point. One LTC1921 is used for each supply. The circuit, while using essentially the same components as the previous example, provides added benefits. The outputs of the two LTC1921s can be wire-ORed directly, if required, reducing the number of optoisolators. If separate fuse or supply warnings are not required, then any or all of the outputs of the two monitors may be combined, as shown in Figure 3. In addition, the secondary supply/fuse monitor pairs (VB and FUSEB) can be used to monitor a return-line fuse or diode. This is possible due to the symmetrical nature of the LTC1921. Power can be drawn entirely from V_A, while V_B serves only as a reference for the return fuse monitor pin (FUSE B), illustrating the flexibility of this part.

range. Since power is not drawn from downstream of the ORing diodes, the LTC1921 functions properly even if the fuses or diodes are not functional.

acts independently, with the RTN pins wired to the return pins at the card edge rather than the OR point which combines the returns. By monitoring

Application Example

The LTC1921 measures two supply voltages by comparing them to a common reference. This requires that the returns be common, as is the case with many telecom switch cards. Some applications, however, have both supply and return OR diodes on the switch card. If an application requires separate monitoring of the returns, and possibly return fuses, a second LTC1921 can be used.

One of many possible configurations, Figure 1 shows a circuit that allows the monitoring of multiple returns. In this circuit each LTC1921
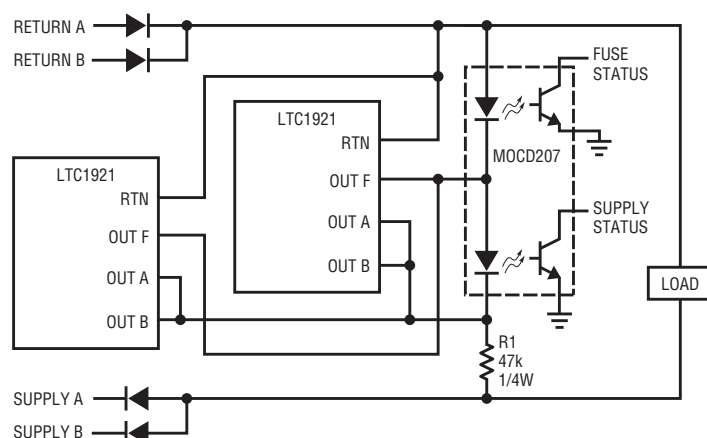

Figure 3. Supply and fuse status outputs combined into one dual optoisolator

Video Signal Distribution Using Low Supply-Voltage Amplifiers

by Jon Munson

Introduction

Video designs are often pressed to operate on the lowest possible rail voltages—a simple result of the trend towards lower voltage logic and the advantages of sharing supply potentials wherever possible. Video designs are further complicated by the need to accommodate the dynamic offset variation inherent in AC-coupled designs as picture content varies. Traditional op amps require relatively large amounts of output-swing headroom and are therefore impractical for AC coupling at even 5V. Linear Technology offers a new family of video op amps which addresses these issues and offers the ability to operate down to 3.3V in most instances. This family includes the LT6205 (single), LT6206 (dual), LT6207 (quad), LT6550 (triple, fixed gain of 2), and LT6551 (quad, fixed gain of 2).

Video Signal Characteristics

To determine the minimum video amplifier supply voltage, we must first examine the nature of the signal. Composite video is the most commonly used signal in broadcast-grade products. Composite video combines luma (or
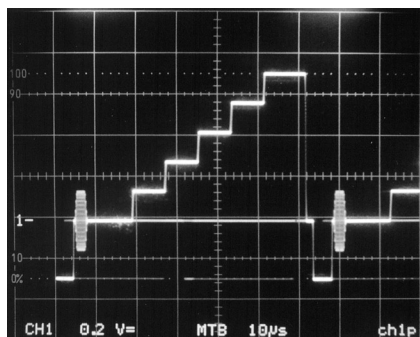

Figure 1. Typical 1V$_{P-P}$ video waveform (several lines overlaid)

luminance, the intensity information), chroma (the colorimetry information) and sync (vertical and horizontal raster timing) elements into a single signal, NTSC and PAL being the common formats. The component video formats for entertainment systems use separate signal(s) for the luma and chroma (i.e. Y/C or YPbPr) with sync generally applied to the luma channel (Y signal). In some instances, native RGB signals (separate intensity information for each primary color: red, green, blue) have sync included as well. All the signal types that include sync are electrically similar from a volt-age-swing standpoint, though various timing and bandwidth relationships exist depending on the applicable standard.

The typical video waveforms that include sync (including full composite) are specified to have a nominal 1.0V$_{P-P}$ amplitude, as shown in Figure 1. The lower 0.3V is reserved for sync tips that carry timing information. The black level (zero intensity) of the waveform is at (or setup very slightly above) this upper limit of the sync information. Waveform content above the black-level is intensity information, with peak brightness represented at the maximum signal level. The sync potential represents blacker-than-black intensity, so scan retrace activity is invisible on a CRT. In the case of composite video, the modulated color subcarrier is superimposed on the waveform, but the dynamics generally remain inside the 1V$_{P-P}$ limit (a notable exception is the chroma ramp used for differential-gain and differential-phase measurements, which can reach 1.15V$_{P-P}$).

Amplifier Considerations

Most video amplifiers drive cables that are series terminated (back-terminated) at the source and load-terminated at the destination with resistances equal to the cable characteristic impedance, Z$_0$ (usually 75Ω). This configuration forms a 2:1 resistor divider in the cabling that must be corrected in the driver amplifier by delivering 2.0V$_{P-P}$ output into an effective 2 • Z$_0$ load (e.g. 150Ω). Driving the cable can require in excess of 13mA while the output is approaching the saturation-limits of the amplifier output. The absolute minimum supply is V$_{MIN}$ = 2.0 + V$_{SATH}$ + V$_{SATL}$, where the V$_{SAT}$ values represent the minimum voltage drops that an amplifier can be guaranteed to develop with respect to the appropriate supply rail.
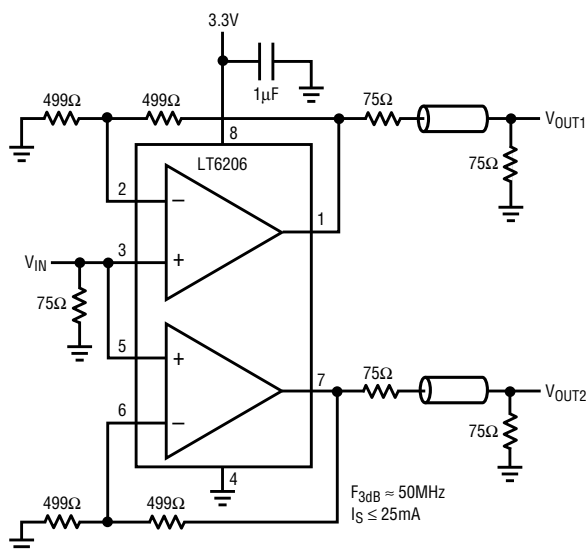

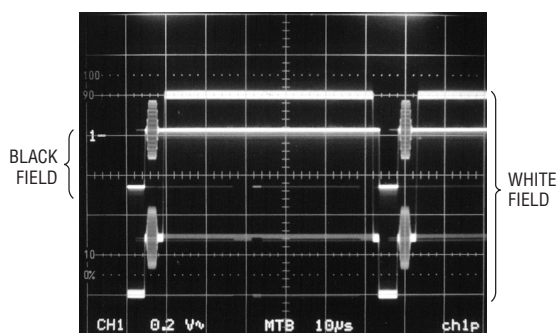**Figure 2. DC-coupled dual composite-video driver powered from 3.3V.**

Figure 3. Video offset-shift due to picture content with conventional AC coupling

For example, the LT6206 dual operating on 3.3V in Figure 2, with exceptionally low $V_{SATH} \leq 0.5V$ and $V_{SATL} \leq 0.35V$, provides a design margin of 0.45V, enough to cover supply variations and DC bias accuracy for the DC-coupled video input.

Handling AC-Coupled Video Signals

Unfortunately, one cannot always be assured that source video has the appropriate DC content to satisfy the amplifier involved, so other design solutions are frequently required. AC-coupled video inputs are intrinsically more difficult to handle than those with DC-coupling because the average signal voltage of the video waveform is effected by the picture content, meaning that the black-level at the amplifier wanders with scene brightness. By analyzing the worst-case wander, we can determine the AC-coupled constraint.

Figure 3 shows two superimposed AC-coupled waveforms, the raised trace being black field and the lowered trace being white field. The wander is measured as 0.56V for the $1V_{P-P}$ NTSC waveform shown, so an additional 1.12V allowance must be made in the amplifier supply (assuming gain

of 2, so $V_{MIN} = 3.12 + V_{SATH} + V_{SATL}$). The amplifier output (for gain of 2) must swing +1.47V to –1.65V around the DC-operating point, so the biasing circuitry needs to be designed accordingly for optimal fidelity. For example, an LT6551 operating on 5.0V, with excellent $V_{SATH} \leq 0.8V$ and $V_{SATL} \leq 0.2V$, has a healthy design margin of 0.88V for the Luminance (with sync) signal. The chroma signal is a symmetric color subcarrier waveform that is about $0.7V_{P-P}$ max, so it works fine with the same bias as the Luminance channel.

A popular method of further minimizing supply requirements with

AC-coupling is to employ a simple clamping scheme as shown in Figure 4. In this circuit, the LT6205 (single version of LT6206) is able to operate from 3.3V by having the sync-tips control the charge on the coupling capacitor, thereby reducing the black-level input wander to ≈ 0.07V. A minor drawback to this circuit is the slight sync-tip compression (≈ 0.025V at input) due to the diode conduction current, though the picture content remains full fidelity. This circuit has nearly the design margin of its DC-coupled counterpart, at 0.31V (for this circuit, $V_{MIN} = 2.14 + V_{SATH} + V_{SATL}$).

Conclusion

With the industry's lowest V_{SAT} output characteristics, the low voltage video amplifiers, including the LT6205 (single), LT6206 (dual), LT6207 (quad), LT6550 (triple, fixed gain of 2), and LT6551 (quad, fixed gain of 2), offer the video designer the ability to share reduced supply voltages along with the logic circuitry. This ability to share supply voltages helps save space and cost by reducing power dissipation and power converter complexity. ∠T
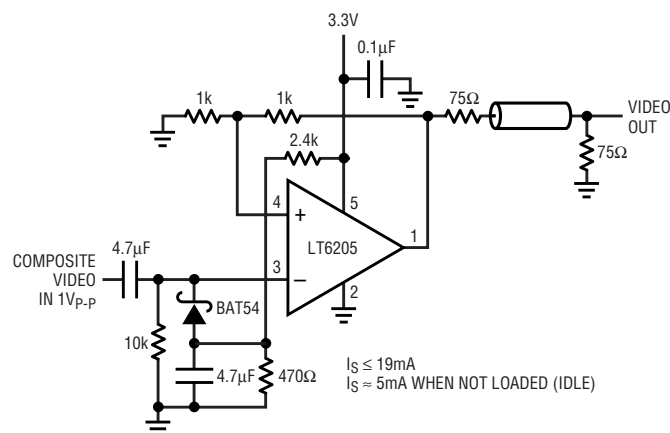
Figure 4. AC-coupled clamped-video amplifier powered from 3.3V

Finally, the combined RTN reference allows each supply monitor to properly indicate status even if a fuse opens, since power is supplied to both sets of outputs as long as at least one supply is functional.

Conclusion

The LTC1921 reduces the board space, component costs and engineering time devoted to telecom power supply monitoring circuitry. It provides an integrated precision monitoring sys-

tem contained entirely in an MSOP–8 or SO–8 package. Despite its remarkably simple setup requirements, the LTC1921 is flexible enough to work in a wide variety of complicated redundant power supply systems. ∠T

New Device Cameos

Dual 16-/14-/12-Bit Rail-to-Rail DACs in 8-Lead MSOP

The LTC2602/LTC2612/LTC2622 are dual 16-, 14- and 12-bit, 2.5V-to-5.5V rail-to-rail voltage-output DACs, in a tiny 8-lead MSOP package. They have built-in high performance output buffers and are guaranteed monotonic.

These parts establish advanced performance standards for output drive, crosstalk and load regulation in single supply, voltage output multiples.

The parts use a simple SPI™/MICROWIRE™ compatible 3-wire serial interface which can be operated at clock rates up to 50MHz.

The LTC2602/LTC2612/LTC2622 incorporate a power on reset circuit. During power-up, the voltage outputs rise less than 10mV above zero scale, and after power up, they stay at zero scale until a valid write and update take place.

215MHz, Rail-to-Rail Output, 1.1nV/√Hz, 3.4mA Op Amp Family

The LT6230/LT6231/LT6232 are single/dual/quad low noise, rail-to-rail output unity gain stable op amps that feature 1.1nV/√Hz noise voltage and draw only 3.4mA of supply current per amplifier—less than a fifth of the current required by parts that compete at similar noise levels. These amplifiers combine very low noise and supply current with a 215MHz gain bandwidth product, a 70V/µs slew rate and are optimized for low supply voltage signal conditioning systems. The LT6230-10 is a single amplifier optimized for higher gain applications resulting in higher gain bandwidth and slew rate. The LT6230 and LT6230-10 include an enable pin that can be used to reduce the supply current to less than 10µA.

The amplifier family has an output that swings within 50mV of either supply rail to maximize the signal dynamic range in low supply applications and is specified on 3.3V, 5V and ±5V supplies. The $e_n \cdot \sqrt{I_{SUPPLY}}$ product of 1.9

per amplifier is among the most noise efficient of any op amp.

The LT6230/LT6230-10 is available in the 6-lead SOT-23 package and the LT6231 dual is available in the 8-pin SO package with standard pinouts. For compact layouts, the dual is also available in a tiny dual fine pitch leadless package (DFN). The LT6232 is available in the 16-pin SSOP package.

Rugged, CompactPCI Hot Swap Controller Offers Increased Immunity to Inductive Power Supplies

The LTC4244 Hot Swap controller allows a board to be safely inserted and removed from a CompactPCI™ bus slot. External N-channel transistors control the 5V and 3.3V supplies while on-chip switches control the ±12V supplies. The 3.3V and 5V supplies can be ramped up at an adjustable rate. Electronic circuit breakers protect all four supplies against over current faults. The 3.3V and 5V circuit breakers feature two levels of short-circuit protection. Overloads of 1x to 3x the current limit trip the circuit breaker only if they last longer than 25µs. Larger current overloads are actively limited to 3x the current limit during the 25µs interval. An absolute maximum rating of ±14.4V for $12V_{IN}$ and V_{EEIN}, respectively, allow the LTC4244 to operate safely from inductive power supplies, while de-glitched undervoltage lockouts on all four supplies ensure that the part will turn on once all the supplies are within tolerance.

After the power-up cycle is complete, the TIMER pin capacitor serves as auxiliary chip V_{CC} enabling the LTC4244 to function without interruption in the presence of large voltage spikes on the $12V_{IN}$ supply. The $\overline{PWRGD}$ output indicates when all four output supplies are within tolerance. The OFF/$\overline{ON}$ pin is used to cycle board power or reset the circuit breaker. The PRECHARGE output can be used to bias the bus I/O pins during card insertion and extraction. PCI_RST# is

combined on-chip with the HEALTHY# signal in order to generate LOCAL_PCI_RST#. The LTC4244-1 is configured for CompactPCI applications where the –12V supply is not needed.

The LTC4244 and the LTC4244-1 are offered in a 20-lead SSOP package in both commercial and industrial temperature ranges. The LTC4244 is pin compatible with the LTC1644.

3.3V, 3.2Gbps VCSEL Driver

The LTC5100 is a 3.2Gbps VCSEL (Vertical Cavity Surface Emitting Laser) driver offering an unprecedented level of integration and high speed performance. The part incorporates a full range of features to ensure consistently outstanding eye diagrams. The data inputs are AC coupled, eliminating the need for external capacitors. The LTC5100 has a precisely controlled 50Ω output that is DC coupled to the laser, allowing arbitrary placement of the IC. No coupling capacitors, ferrite beads or external transistors are needed, simplifying layout, reducing board area and the risk of signal corruption. The unique output stage of the LTC5100 confines the modulation current to the ground system, isolating the high speed signal from the power supply to minimize RFI.

The LTC5100 supports fully automated production with its extensive monitoring and control features. Integrated 10-bit DACs eliminate the need for external potentiometers. An onboard 10-bit ADC provides the laser current and voltage, as well as monitor diode current and temperature. Status information is available from the I²C™ serial interface for feedback and statistical process control.

An internal digital controller compensates laser temperature drift and provides extensive laser safety features.

Emulation and setup software is available at the www.linear.com. *LT*

DESIGN TOOLS

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Software

SwitcherCAD™ III/LTC SPICE — LTC SwitcherCAD III is a fully functional SPICE simulator with enhancements and models to ease the simulation of switching regulators. This SPICE is a high performance circuit simulator and integrated waveform viewer, and also includes schematic capture. Our enhancements to SPICE result in much faster simulation of switching regulators than is possible with normal SPICE simulators. SwitcherCAD III includes SPICE, macromodels for 80% of LTC's switching regulators and over 200 op amp models. It also includes models of resistors, transistors and MOSFETs. With this SPICE simulator, most switching regulator waveforms can be viewed in a few minutes on a high performance PC. Circuits using op amps and transistors can also be easily simulated. Download at www.linear.com

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SPICE Macromodel Library — This library includes LTC op amp SPICE macromodels. The models can be used with any version of SPICE for analog circuit simulations. These models run on SwitcherCAD III/LTC SPICE.

Noise Program — This PC program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp.

World Headquarters

Linear Technology Corporation
1630 McCarthy Blvd.
Milpitas, CA 95035-7417
Phone: (408) 432-1900
FAX: (408) 434-0507
www.linear.com

U.S. Sales Offices

NORTHWEST AREA
Bay Area
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Los Angeles
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Dallas, TX 75248
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Houston, TX 77043
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FAX: (713) 463-5009

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Cary, NC 27513
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FAX: (919) 678-0041

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Asia Sales Offices

CHINA
Linear Technology Corp. Ltd.
Unit 2108, Metroplaza Tower 2
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Phone: +852 2428-0303
FAX: +852 2348-0885

Linear Technology Corp. Ltd.
Room 1610, Central Plaza
No. 227 Huangpi Bei Lu
Shanghai, 200003, PRC
Phone: +86 (21) 6375-9478
FAX: +86 (21) 6375-9479

Linear Technology Corp. Ltd.
Room 707, 7th Floor
Beijing Canway Building
66 Nan Li Shi Lu
Beijing, 100045, PRC
Phone: +86 (10) 6801-1080
FAX: +86 (10) 6805-4030

JAPAN
Linear Technology KK
8F Shuwa Kioicho Park Bldg.
3-6 Kioicho Chiyoda-ku
Tokyo, 102-0094, Japan
Phone: +81 (3) 5226-7291
FAX: +81 (3) 5226-0268

Linear Technology KK
6F Kearny Place Honmachi Bldg.
1-6-13 Awaza, Nishi-ku
Osaka-shi, 550-0011, Japan
Phone: +81 (6) 6533-5880
FAX: +81 (6) 6543-2588

KOREA
Linear Technology Korea Co., Ltd.
Yundang Building, #1002
Samsung-Dong 144-23
Kangnam-Ku, Seoul 135-090
Korea
Phone: +82 (2) 792-1617
FAX: +82 (2) 792-1619

SINGAPORE
Linear Technology Pte. Ltd.
507 Yishun Industrial Park A
Singapore 768734
Phone: +65 6753-2692
FAX: +65 6752-0108

TAIWAN
Linear Technology Corporation
8F-1, 77, Nanking E. Rd., Sec. 3
Taipei, Taiwan
Phone: +886 (2) 2505-2622
FAX: +886 (2) 2516-0702

Europe Sales Offices

FRANCE
Linear Technology S.A.R.L.
Immeuble "Le Quartz"
58, Chemin de la Justice
92290 Chatenay Malabry
France
Phone: +33 (1) 41 07 95 55
FAX: +33 (1) 46 31 46 13

Linear Technology
"Le Charlemagne"
140, cours Charlemagne
69286 Lyon Cedex 2
France
Phone: +33 (4) 72 41 63 86
FAX: +33 (4) 72 41 62 99

GERMANY
Linear Technology GmbH
Oskar-Messter-Str. 24
D-85737 Ismaning
Germany
Phone: +49 (89) 962455-0
FAX: +49 (89) 963147

Haselburger Damm 4
D-59387 Ascheberg
Germany
Phone: +49 (2593) 9516-0
FAX: +49 (2593) 951679

Zettachring 12
D-70567 Stuttgart
Germany
Phone: +49 (711) 1329890
FAX: +49 (711) 7285055

ITALY
Linear Technology Italy Srl
Via Giovanni da Udine, 34
I-20156 Milano
Italy
Phone: +39 (02) 38093656
FAX: +39 (02) 38093659

SWEDEN
Linear Technology AB
Sollentunavägen 63
S-191 40 Sollentuna
Sweden
Phone: +46 (8) 623-1600
FAX: +46 (8) 623-1650

UNITED KINGDOM
Linear Technology (UK) Ltd.
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United Kingdom
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