

RELIABILITY REPORT  
FOR  
**MAX1081xxUP**  
PLASTIC ENCAPSULATED DEVICES

July 21, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.  
SUNNYVALE, CA 94086

Written by



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## Conclusion

The MAX1081 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX1081 10-bit analog-to-digital converters (ADCs) combines an 8-channel analog-input multiplexer, high-bandwidth track/hold (T/H), and serial interface with high conversion speed and low power consumption. The MAX1081 operates from a single +2.7V to +3.6V supply. The devices analog inputs are software configurable for unipolar/bipolar and single-ended/pseudo-differential operation.

The 4-wire serial interface connects directly to SPI™/QSPI™ and MICROWIRE™ devices without external logic. A serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX1081 uses an external serial-interface clock to perform successive-approximation analog-to-digital conversions. The device features an internal +2.5V reference and a reference-buffer amplifier with a ±1.5% voltage-adjustment range. An external reference with a 1V to  $V_{DD1}$  range may also be used.

The MAX1081 provides a hard-wired SHDN-bar pin and four software-selectable power modes (normal operation, reduced power (REDP), fast power-down (FASTPD), and full power-down (FULLPD)). This device can be programmed to automatically shut down at the end of a conversion or to operate with reduced power. When using the power-down modes, accessing the serial interface automatically powers up the devices, and the quick turn-on time allows them to be shut down between all conversions. This technique can cut supply current below 100mA at lower sampling rates.

The MAX1081 is available in a 20-pin TSSOP package.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
VDD_ to GND	-0.3V to 6V
VDD1 to VDD2	-0.3V to 0.3V
CH0–CH7, COM to GND	-0.3V to (VDD1 + 0.3V)
REF, REFADJ to GND	-0.3V to (VDD1 + 0.3V)
Digital Inputs to GND	-0.3V to 6V
Digital Outputs to GND	-0.3V to (VDD2 + 0.3V)
Digital Output Sink Current	25mA
Operating Temperature Ranges	
MAX1081xCUP	0°C to +70°C
MAX1081xEUP	-40°C to +85°C
Storage Temperature Range	-60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
20-Pin TSSOP	559mW
Derates above +70°C	
20-Pin TSSOP	7.0mW/°C

## II. Manufacturing Information

- A. Description/Function: 300ksps/400ksps, Single-Supply, Low-Power, 8-Channel, Serial 10-Bit ADCs with Internal Reference
- B. Process: S12 (Standard 1.2 micron silicon gate CMOS)
- C. Number of Device Transistors: 4286
- D. Fabrication Location: Oregon, USA
- E. Assembly Location: Philippines or Korea
- F. Date of Initial Production: October, 1999

## III. Packaging Information

- A. Package Type: **20-Pin TSSOP**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate
- D. Die Attach: Conductive Epoxy
- E. Bondwire: Gold (1.3 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: # 05- 0101-0508
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

## IV. Die Information

- A. Dimensions: 85 x 130 mils
- B. Passivation:  $\text{Si}_3\text{N}_4/\text{SiO}_2$  (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 1.2 microns (as drawn)
- F. Minimum Metal Spacing: 1.2 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric:  $\text{SiO}_2$
- I. Die Separation Method: Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)  
Bryan Preeshl (Executive Director)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 318 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 3.41 \times 10^{-9}$$

$$\lambda = 3.41 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5391) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

### C. E.S.D. and Latch-Up Testing

The AD95 die type has been found to have all pins able to withstand a transient pulse of  $\pm 1500\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX1081xxUP**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		318	0
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	TSSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

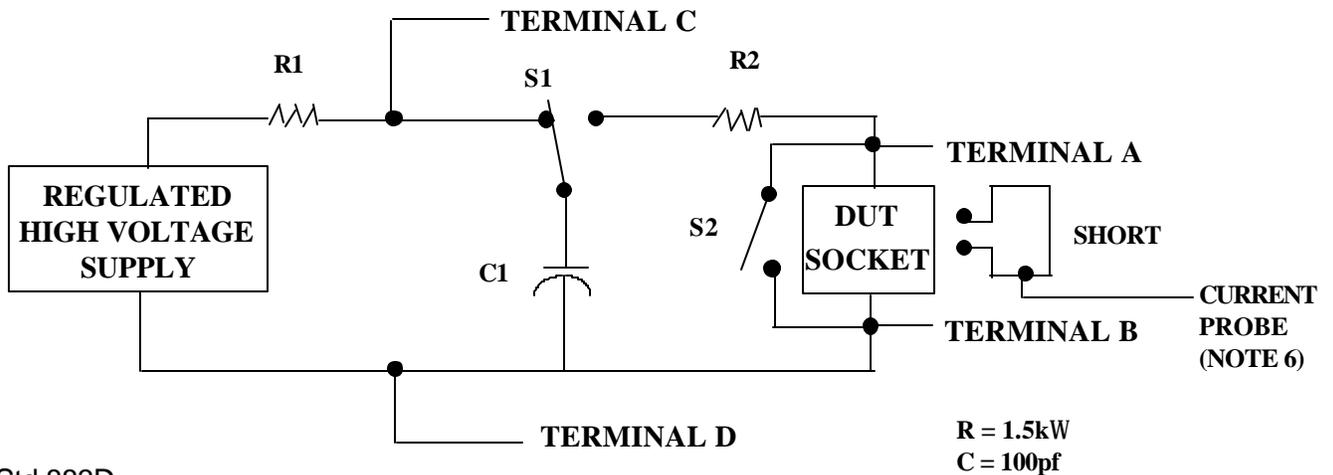
2/ No connects are not to be tested.

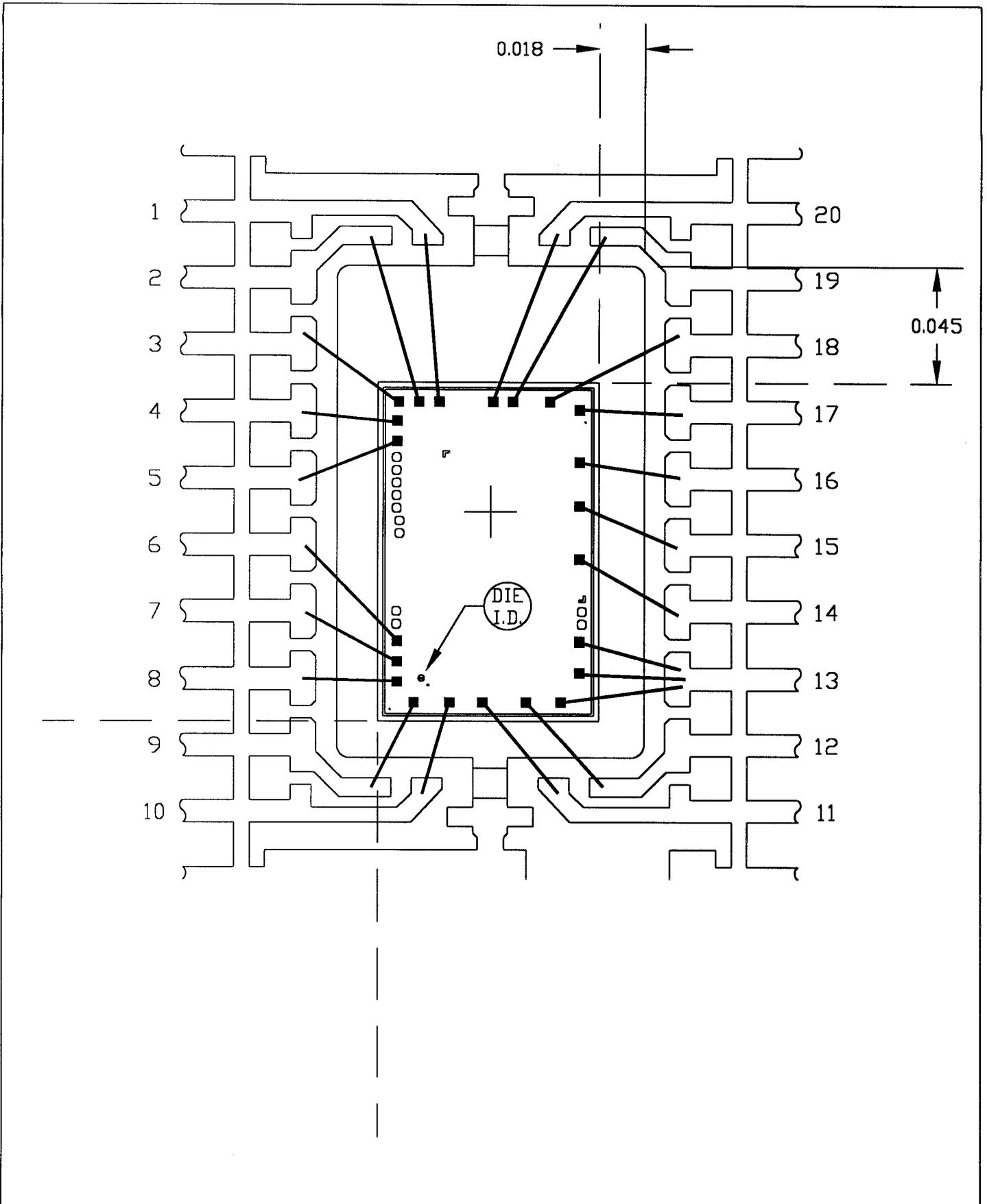
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ ,  $GND$ ,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

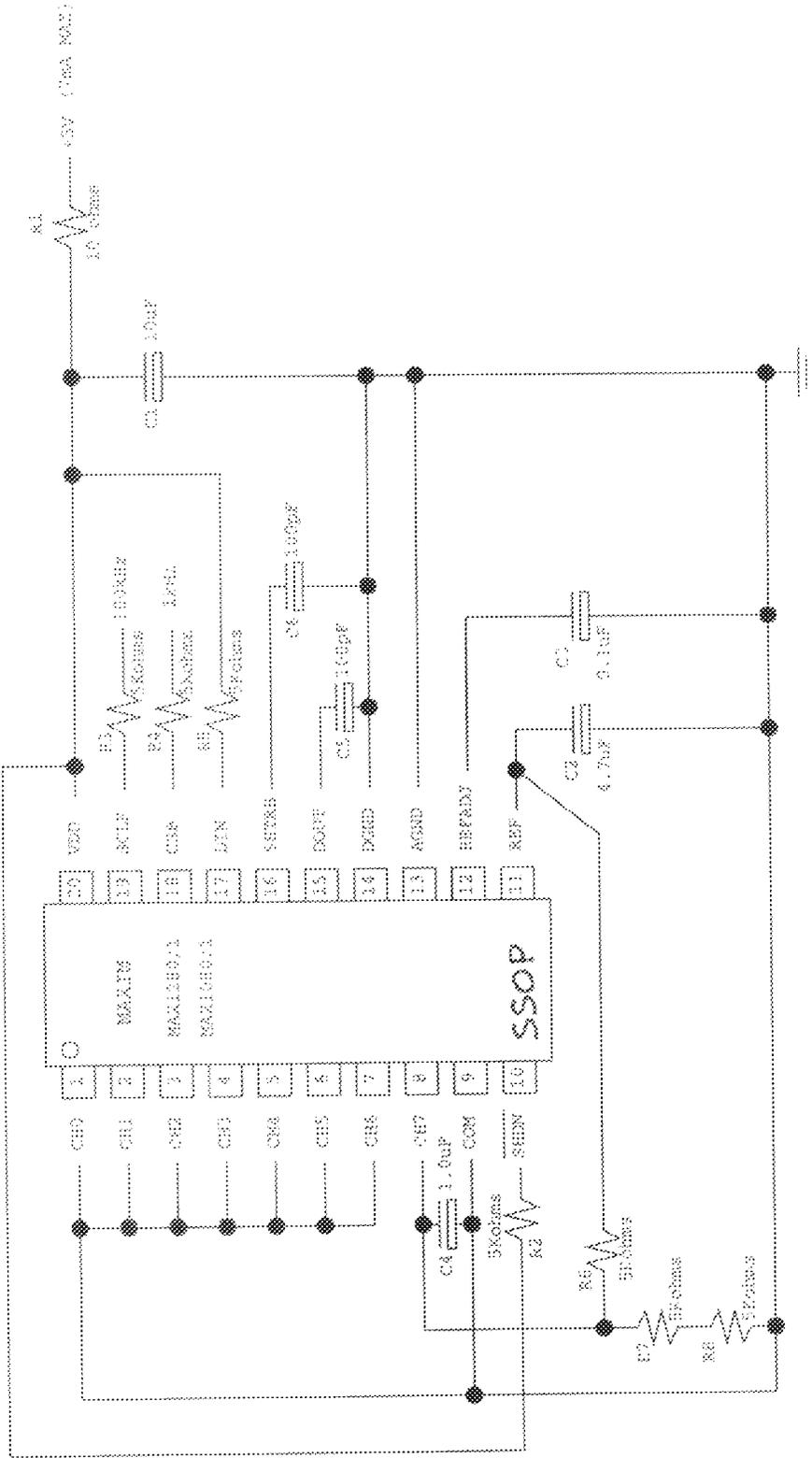
3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: U20-2		APPROVALS	DATE	<b>MAXIM</b>	
CAV./PAD SIZE: 118X189	PKG. DESIGN		7/8/99 9/8/99	BUILDSHEET NUMBER: 05-0101-0508	REV: A



NOTE:

1. Max power dissipation is 350mW per package.
2. All resistors are 1/4W, +/-5%.
3. Burn-in boards may use fuses in supply lines for multiple packages.

06-5391

MAXIM CONFIDENTIAL	CREATED:	00/00/00	BY:	PM3	REVA:	FRONT SHEET	ENGR:	DAVE FLETCHER
	LAST REV'D:	2-3-1999, 16:29		SIZE:	A	PARTIAL	REV NO:	-
BIB20	PROJECT:	A095C		FILE:	BIB20		SHEET:	1 OF 1
	DESC:	8879-01 BOARD FOR COM2 PARTS		FILE:	BIB20		SHEET:	1 OF 1