RELIABILITY REPORT

FOR

MAX11103ATB+T / MAX11103AUB+T

PLASTIC ENCAPSULATED DEVICES

February 1, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX11103ATB+T / MAX11103AUB+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

I. General

The MAX11102, MAX11103, MAX11105, MAX11106, MAX11110, MAX11111, MAX11115-MAX11117 are 12-/10-/8-bit, compact, high-speed, low-power, successive approximation analog-to-digital converters (ADCs). These high-performance ADCs include a high-dynamic range sample-and-hold and a high-speed serial interface. These ADCs accept a full-scale input from 0V to the power supply or to the reference voltage. The MAX11102/MAX11103/MAX11106/MAX11111 feature dual, single-ended analog inputs connected to the ADC core using a 2:1 MUX. The devices also include a separate supply input for data interface and a dedicated input for reference voltage. In contrast, the single-channel devices generate the reference voltage internally from the power supply. These ADCs operate from a 2.2V to 3.6V supply and consume only 5.2mW at 3Msps and 3.7mW at 2Msps. The devices include full power-down mode and fast wake-up for optimal power management and a high-speed 3-wire serial interface. The 3-wire serial interface directly connects to SPI, QSPII, and MICROWIRE® devices without external logic. Excellent dynamic performance, low voltage, low power, ease of use, and small package size make these converters ideal for portable battery-powered data-acquisition applications, and for other applications that demand low-power consumption and minimal space. These ADCs are available in a 10-pin TDFN package, 10-pin µMAX® package, and a 6-pin SOT23 package. These devices operate over the -40°C to +125°C temperature range.

II. Manufacturing Information

A. Description/Function:	2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs	
B. Process:	0.18u CMOS	
C. Number of Device Transistors:	17522	
D. Fabrication Location:	Taiwan	
E. Assembly Location:	China, Taiwan, Thailand	Philippines, Thailand
F. Date of Initial Production:	April 23, 2010	

III. Packaging Information

A. Package Type:	10-pin TDFN 3x3	10-pin uMAX
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (1 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-3812	#05-9000-3811
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	54°C/W	97°C/W
K. Single Layer Theta Jc:	9°C/W	5°C/W
L. Multi Layer Theta Ja:	41°C/W	77.6°C/W
M. Multi Layer Theta Jc:	9°C/W	5°C/W

IV. Die Information

A. Dimensions:	57X35 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \text{ (Chi square value for MTTF upper limit)}$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.11 @ 25C and 1.87 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QYTZBQ001H, D/C 1010)

The AC83 die type has been found to have all pins able to withstand an HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX11103ATB+T / MAX11103AUB+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	QYTYBQ001C, D/C 0950

Note 1: Life Test Data may represent plastic DIP qualification lots.