RELIABILITY REPORT

FOR

MAX11156ETC+T

PLASTIC ENCAPSULATED DEVICES

February 16, 2016

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX11156ETC+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX11156 18-bit, 500ksps, SAR ADC offers excellent AC and DC performance with true bipolar input range, small size, and internal reference. The MAX11156 measures a ±5V (10VP-P) input range while operating from a single 5V supply. A patented charge-pump architecture allows direct sampling of high-impedance sources. The MAX11156 integrates an optional 6ppm/°C reference with internal buffer, saving the cost and space of an external reference. The MAX11156 produces 94.6dB SNR and -105dB THD (typ). The MAX11156 guarantees 18-bit no-missing codes. The MAX11156 communicates using an SPI-compatible serial interface at 2.5V, 3V, 3.3V, or 5V logic. The serial interface can be used to daisy-chain multiple ADCs in parallel for multichannel applications and provides a busy indicator option for simplified system synchronization and timing. The MAX11156 is offered in a 12-pin, 3mm x 3mm, TDFN package and is specified over the -40°C to +85°C temperature range.-

II. Manufacturing Information

A. Description/Function:	18-Bit, 500ksps, ±5V SAR ADC with Internal Reference in TDFN
B. Process:	S45
C. Number of Device Transistors:	35573
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Taiwan
F. Date of Initial Production:	March 12, 2013

III. Packaging Information

A. Package Type:	12L TDFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4679
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	63℃/W
K. Single Layer Theta Jc:	8.5℃/W
L. Multi Layer Theta Ja:	41℃/W
M. Multi Layer Theta Jc:	8.5℃/W

IV. Die Information

A. Dimensions:	62X87 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 79 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.9 \times 10^{-9}$

λ = 13.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S45 Process results in a FIT Rate of 3.20 @ 25C and 55.4 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot T2UZBQ001F, D/C 1251)

The AC91 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX11156ETC+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0	T2UZBQ002B, D/C 1220

Note 1: Life Test Data may represent plastic DIP qualification lots.