

RELIABILITY REPORT
FOR
MAX1116EKA
PLASTIC ENCAPSULATED DEVICES

May 8, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Conclusion

The MAX1116 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	IV.Die Information
Attachments

I. Device Description

A. General

The MAX1116 low-power, 8-bit, analog-to-digital converter (ADC) features an internal track/hold (T/H), voltage reference, V_{DD} monitor, clock, and serial interface. The MAX1116 is specified from +4.5V to +5.5V. The part consumes only 175 μ A at 100ksps.

The full-scale analog input range is determined by the internal reference of +2. The MAX1116 also features AutoShutdown™ power-down mode which reduces power consumption to <1 μ A when the device is not in use. The 3-wire serial interface directly connects to SPI™, QSPI™, and MICROWIRE™ devices without external logic. Conversions up to 100ksps are performed using an internal clock.

The MAX1116 is available in an 8-pin SOT23 package with a footprint that is just 30% of an 8-pin SO.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
VDD to GND	-0.3V to +6.0V
CH0 to GND	-0.3V to (VDD + 0.3V)
Digital Output to GND	-0.3V to (VDD + 0.3V)
Digital Input to GND	-0.3V to +6.0V
Maximum Current into Any Pin	\pm 50mA
Operating Temperature Range	-40°C to + 85°C
Junction Temperature	+150°C
Storage Temperature Range	-60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
8-Pin SOT	714mW
Derates above +70°C	
8-Pin SOT	8.9mW/°C

II. Manufacturing Information

A. Description/Function:	Single-Supply, Low-Power, Serial 8-Bit ADCs
B. Process:	S6 (Standard 0.6 micron silicon gate CMOS)
C. Number of Device Transistors:	2000
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	October, 2000

III. Packaging Information

A. Package Type:	8-Pin SOT
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Non-Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-2101-0029
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1

IV. Die Information

A. Dimensions:	31 x 55 mils
B. Passivation:	$\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	0.6 microns (as drawn)
F. Minimum Metal Spacing:	0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 159 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

 Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 6.83 \times 10^{-9}$$

$$\lambda = 6.83 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5604) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AC22-2 die type has been found to have all pins able to withstand a transient pulse of $\pm 2500\text{V}$ per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX1116EKA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		159	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SOT	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

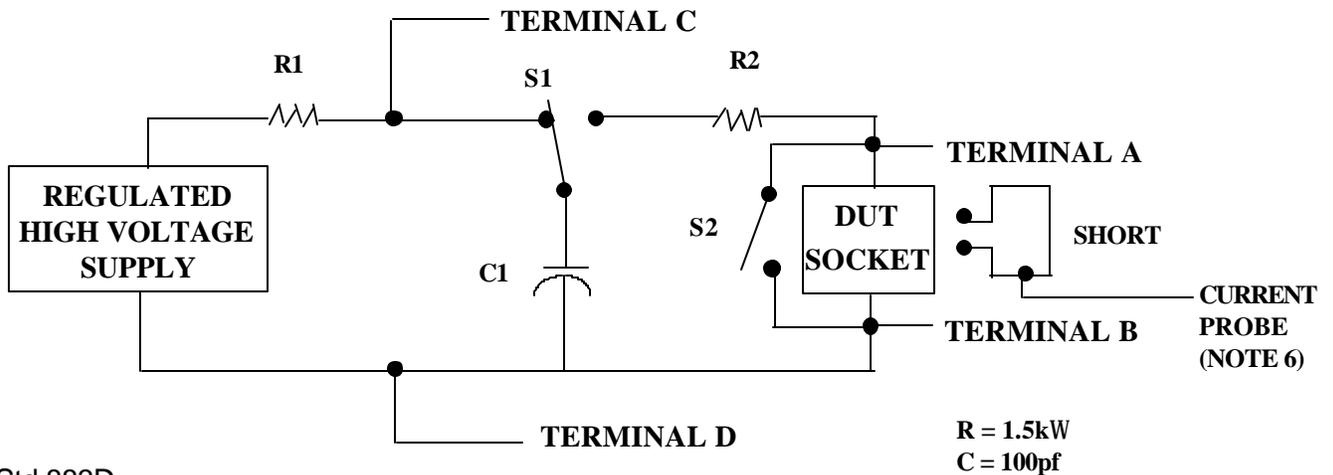
2/ No connects are not to be tested.

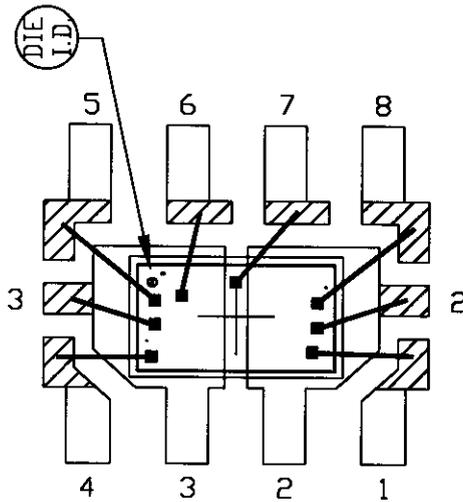
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND , $+V_S$, $-V_S$, V_{REF} , etc).

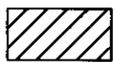
3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





NOTE: CAVITY DOWN

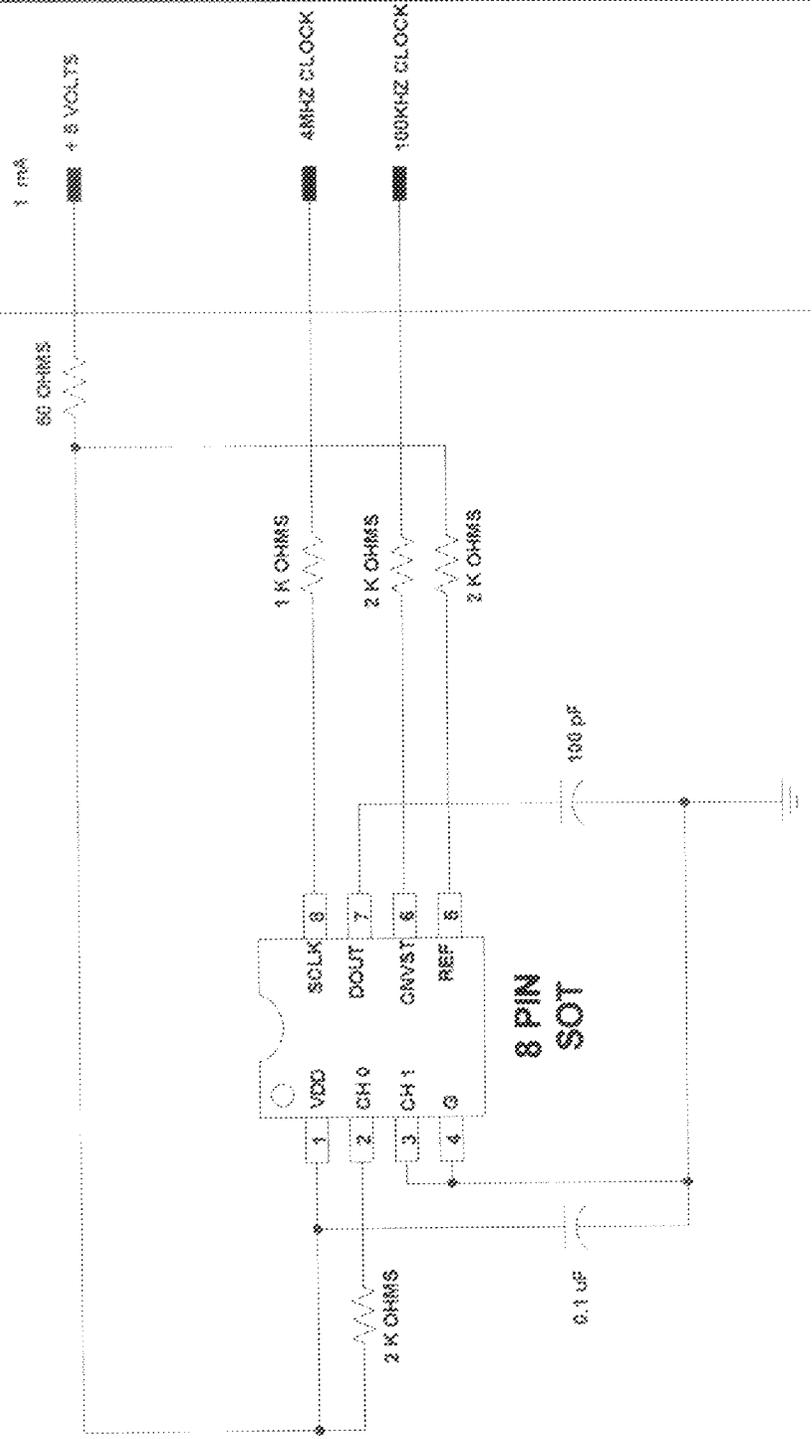
 BONDABLE AREA

USE NON-CONDUCTIVE EPOXY

PKG. CODE: K8S-3		SIGNATURES	DATE	 CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 75x37	PKG. DESIGN		BOND DIAGRAM #: 05-2101-0029	

ONCE PER SOCKET

ONCE PER BOARD



MAXIM BURN-IN SCHEMATIC
SPEC 06-5604 REV. B
DATE: 4 / 12 / 2000

DEVICES: MAX 1115/16/17/18/19
MAX. EXPECTED CURRENT = 1 mA

DRAWN BY: CHRIS JANBARO
NOTES: