RELIABILITY REPORT

FOR

MAX114ENG+

PLASTIC ENCAPSULATED DEVICES

October 28, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX114ENG+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX114/MAX118 are microprocessor-compatible, 8-bit, 4-channel and 8-channel analog-to-digital converters (ADCs). They operate from a single +5V supply and use a half-flash technique to achieve a 660ns conversion time (1Msps). A power-down (active-low PWRDN) pin reduces current consumption typically to 1µA. The devices return from power-down mode to normal operating mode in less than 200ns, allowing large supply-current reductions in Burst Mode® applications (in Burst Mode, the ADC wakes up from a low-power state at specified intervals to sample the analog input signals). Both converters include a track/hold, enabling the ADC to digitize fast analog signals. Microprocessor (µP) interfaces are simplified because the ADC can appear as a memory location or I/O port without external interface logic. The data outputs use latched, three-state buffer circuitry for direct connection to an 8-bit parallel µP data bus or system input port. The MAX114/MAX118 input/reference configuration enables ratiometric operation. The 4-channel MAX114 is available in a 24-pin DIP or SSOP. The 8-channel MAX118 is available in a 28-pin DIP or SSOP. For +3V applications, refer to the MAX113/MAX117 data sheet.

II. Manufacturing Information

A. Description/Function:	+5V, 1Msps, 4 and 8-Channel, 8-Bit ADCs with 1µA Power-Down
B. Process:	S3
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Philippines
F. Date of Initial Production:	Pre 1997

III. Packaging Information

A. Package Type:	24-pin PDIP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0101-0417
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	75°C/W
K. Single Layer Theta Jc:	30°C/W
L. Multi Layer Theta Ja:	N/A
M. Multi Layer Theta Jc:	N/A

IV. Die Information

A. Dimensions:	132X107 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	3.0 microns (as drawn)
F. Minimum Metal Spacing:	3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{1000 \times 4340 \times 144 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 1.47 \times 10^{-9}$

$\lambda = 1.47$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S3 Process results in a FIT Rate of 0.03 @ 25C and 0.5 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot NMPBBQ002, D/C 9904)

The AD69-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1

Reliability Evaluation Test Results

MAX114ENG+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 1000 hrs.	DC Parameters & functionality	144	0	N5LAEA008Q, D/C 9904

Note 1: Life Test Data may represent plastic DIP qualification lots.