RELIABILITY REPORT

FOR

MAX118xxI

PLASTIC ENCAPSULATED DEVICES

August 13, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX118 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX118 is a microprocessor-compatible 8-bit, 8 channel analog-to-digital converter (ADC). It operates from a single +5V supply and uses a half-flash technique to achieve a 660ns conversion time (1Msps). A power-down (/PWRDN) pin reduces current consumption typically to 1µA. The device returns from power-down mode to normal operating mode is less than 200ns, allowing large supply-current reductions in burst-mode applications (in burst mode, the ADC wakes up from a low-power state at specified intervals to sample the analog input signals). This converter includes a track/hold, enabling the ADC to digitize fast analog signals.

Microprocessor (µP) interfaces are simplified because the ADC can appear as a memory location or an I/O port without external interface logic. The data output uses latched, three-state buffer circuitry for direct connection to an 8-bit parallel µP data bus or system input port. The MAX114 input/reference configuration enables ratiometric operation.

B. Absolute Maximum Ratings

Item	Rating
V_{DD} to GND	-0.3V to +7V
Digital Input Voltage to GND	-0.3V to (V_{DD} + 0.3V)
Digital Output Voltage to GND	-0.3V to (V_{DD} + 0.3V)
REF+ to GND	-0.3V to (V_{DD} + 0.3V)
REF- to GND	-0.3V to (V_{DD} + 0.3V)
IN_ to GND	-0.3V to (V_{DD} + 0.3V)
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
28 Lead SSOP	762mW
28 Lead W. PDIP	1.14W
Derates above +70°C	
28 Lead SSOP	9.52mW/°C
28 Lead W. PDIP	14.29mW/°C

II. Manufacturing Information

A. Description/Function:	+5V, 1 Msps, 8-Channel, 8-Bit ADC with 1µA Power-Down
B. Process:	SG3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	2011
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Korea
F. Date of Initial Production:	June, 1996

III. Packaging Information

A. Package Type:	**28 Lead SSOP**	**28 lead W. PDIP**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-0101-0415	# 05-0101-0413
H. Flammability Rating:	Class UL94-V0	Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions:	132 x 10 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83 \text{ (Chi square value for MTTF upper limit)}}{192 \times 4389 \times 200 \times 2}$$

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 5.43 \times 10^{-9}$

$\lambda = 5.43$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AD69 die type has been found to have all pins able to withstand a transient pulse of ± 2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX118xxI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION		SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		200	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	28 DIP 28 SSOP 560	77 1	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Shrink Small Outline package.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

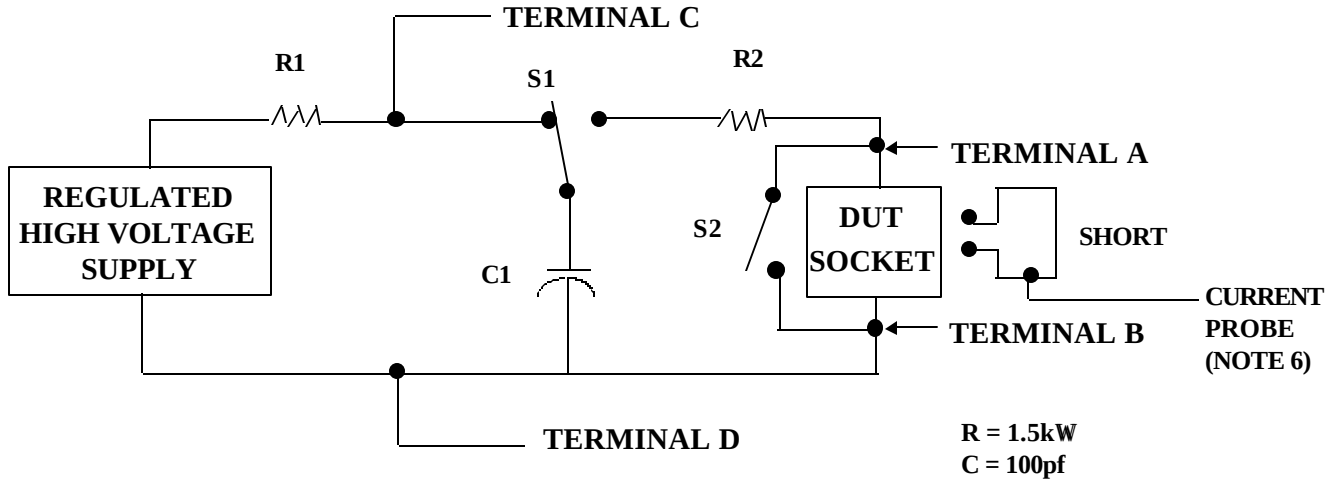
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

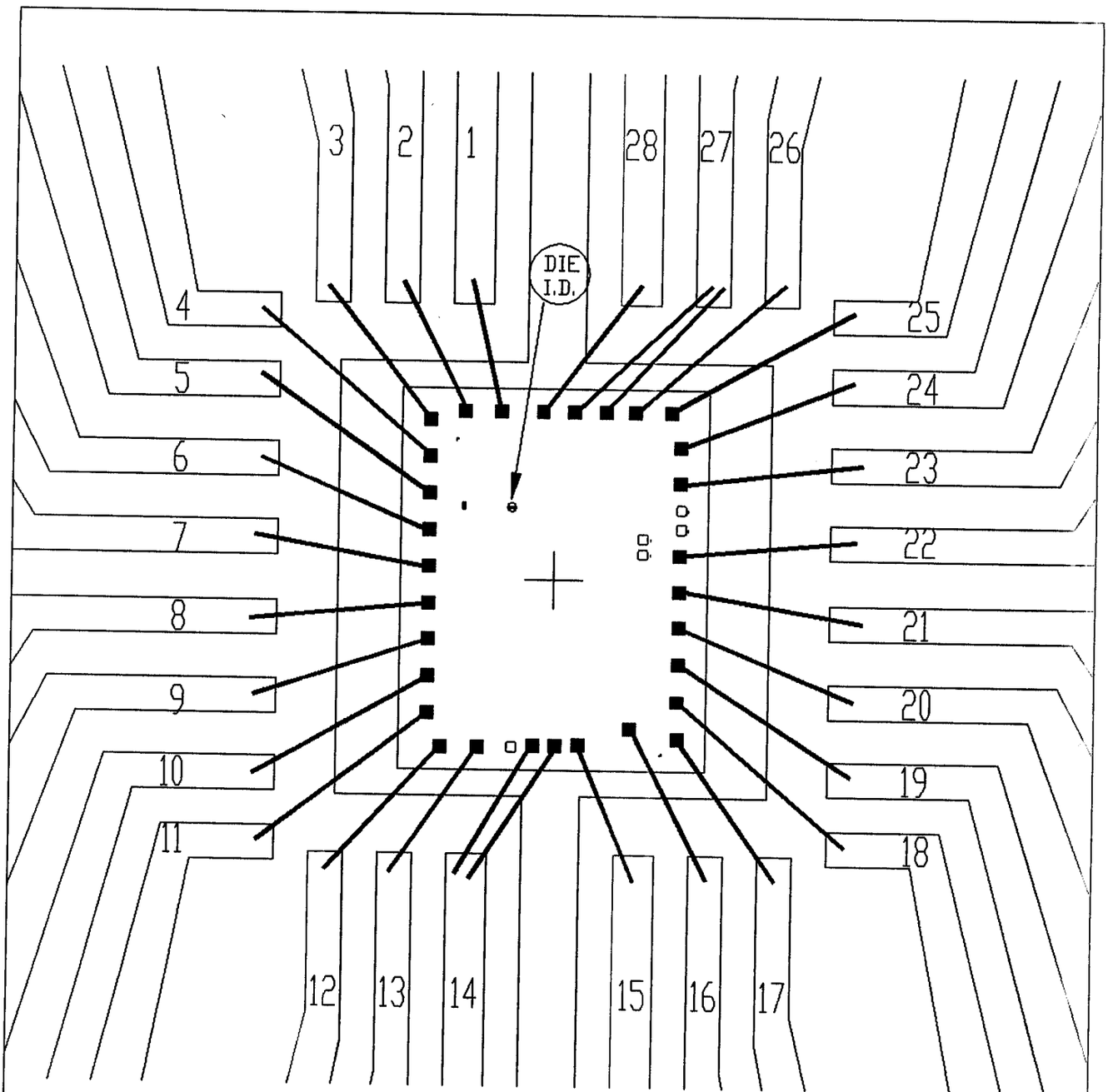
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

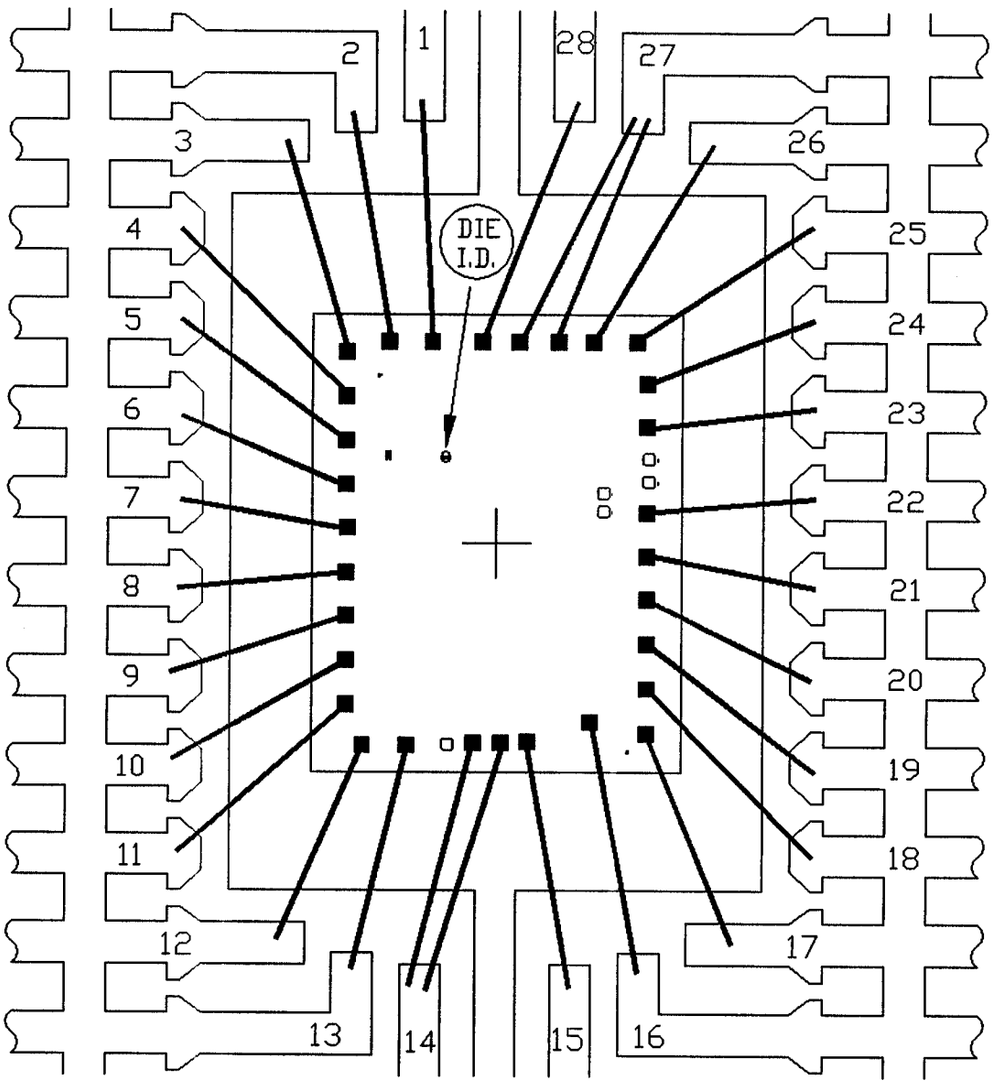
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and



the combination of all the other input and output pins shall be open.



PKG.CODE: P28-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 150 X 150	PKG. DESIGN			BUILDSHEET NUMBER: 05-0101-0413	REV.: A



PKG.CODE: A28-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 154X200	PKG. DESIGN			BUILDSHEET NUMBER: 05-0101-0415 / REV.: A