

RELIABILITY REPORT
FOR
MAX125CCAX+
PLASTIC ENCAPSULATED DEVICES

March 9, 2016

MAXIM INTEGRATED

160 RIO ROBLES
SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX125CCAX+D successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I.Device Description	IV.Die Information
II.Manufacturing Information	V.Quality Assurance Information
III.Packaging Information	VI.Reliability Evaluation
.....Attachments	

I. Device Description

A. General

The MAX125/MAX126 are high-speed, multichannel, 14-bit data-acquisition systems (DAS) with simultaneous track/holds (T/Hs). These devices contain a 14-bit, 3 μ s, successive-approximation analog-to-digital converter (ADC), a +2.5V reference, a buffered reference input, and a bank of four simultaneous-sampling T/H amplifiers that preserve the relative phase information of the sampled inputs. The MAX125/MAX126 have two multiplexed inputs for each T/H, allowing a total of eight inputs. In addition, the converter is overvoltage tolerant to ± 17 V; a fault condition on any channel will not harm the IC. Available input ranges are ± 5 V (MAX125) and ± 2.5 V (MAX126). An on-board sequencer converts one to four channels per active-low CONVST pulse. In the default mode, one T/H output (CH1A) is converted. An interrupt signal (active-low INT) is provided after the last conversion is complete. Convert two, three, or four channels by reprogramming the MAX125/MAX126 through the bidirectional parallel interface. Once programmed, the MAX125/MAX126 continue to convert the specified number of channels per active-low CONVST pulse until they are reprogrammed. The channels are converted sequentially, beginning with CH1. The INT signal always follows the end of the last conversion in a conversion sequence. The ADC converts each assigned channel in 3 μ s and stores the result in an internal 14x4 RAM. Upon completion of the conversions, data can be accessed by applying successive pulses to the active-low RD pin. Four successive reads access four data words sequentially. The parallel interface's data-access and bus-release timing specifications are compatible with most popular digital signal processors and 16-bit/32-bit microprocessors, so the MAX125/MAX126 conversion results can be accessed without resorting to wait states.

II. Manufacturing Information

A. Description/Function:	2x4-Channel, Simultaneous-Sampling, 14-Bit DAS
B. Process:	S3
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon
E. Assembly Location:	Philippines, Malaysia
F. Date of Initial Production:	October 25, 1997

III. Packaging Information

A. Package Type:	36-pin SSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0101-0412
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	84.7°C/W
K. Single Layer Theta Jc:	19.3°C/W
L. Multi Layer Theta Ja:	57.6°C/W
M. Multi Layer Theta Jc:	19.3°C/W

IV. Die Information

A. Dimensions:	205X170 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	3.0 microns (as drawn)
F. Minimum Metal Spacing:	3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

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|-----------------------------------|---|
| A. Quality Assurance Contacts: | Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 210 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 5.24 \times 10^{-9}$$

$$\lambda = 5.24 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S3 Process results in a FIT Rate of 0.03 @ 25C and 0.52 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot XKXABB001A, D/C 9821)

The AD75 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-150mA.

Table 1
Reliability Evaluation Test Results

MAX125CCAX+D

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C	DC Parameters	80	0	NKXAEA008B, D/C 0008
	Biased	& functionality	50	0	XKXABX001D, D/C 9728
	Time = 192 hrs.		80	0	XTEAQQ004B, D/C 9120

Note 1: Life Test Data may represent plastic DIP qualification lots.