MAX12553ETL
Rev. C

RELIABILITY REPORT

FOR

MAX12553ETL

PLASTIC ENCAPSULATED DEVICES

July 20, 2006

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX12553 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX12553 is a 3.3V, 14-bit, 65Msps analog-to-digital converter (ADC) featuring a fully differential wideband track-and-hold (T/H) input amplifier, driving a low-noise internal quantizer. The analog input stage accepts singleended or differential signals. The MAX12553 is optimized for low-power, small size, and high dynamic performance. Excellent dynamic performance is maintained from baseband to input frequencies of 175MHz and beyond, making the MAX12553 ideal for intermediatefrequency (IF) sampling applications.

Powered from a single 3.15V to 3.60V supply, the MAX12553 consumes only 363mW while delivering a typical signal-to-noise (SNR) performance of 71dB at an input frequency of 175MHz. In addition to low operating power, the MAX12553 features a 150µW powerdown mode to conserve power during idle periods.

A flexible reference structure allows the MAX12553 to use the internal 2.048V bandgap reference or accept an externally applied reference. The reference structure allows the full-scale analog input range to be adjusted from ±0.35V to ±1.10V. The MAX12553 provides a common- mode reference to simplify design and reduce external component count in differential analog input circuits.

The MAX12553 supports both a single-ended and differential input clock drive. Wide variations in the clock duty cycle are compensated with the ADC's internal duty-cycle equalizer (DCE).

ADC conversion results are available through a 14-bit, parallel, CMOS-compatible output bus. The digital output format is pin selectable to be either two's complement or Gray code. A data-valid indicator eliminates external components that are normally required for reliable digital interfacing. A separate digital power input accepts a wide 1.7V to 3.6V supply, allowing the MAX12553 to interface with various logic levels.

The MAX12553 is available in a 6mm x 6mm x 0.8mm, 40-pin thin QFN package with exposed paddle (EP), and is specified for the extended industrial (-40°C to +85°C) temperature range.

B. Absolute Maximum Ratings

Item	Rating
V_{DD} to GND	-0.3V to +3.6V
OV_{DD} to GND	-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
INP, INN to GND	-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
REFIN, REFOUT, REFP, REFN, COM to GND	-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
CLKP, CLKN, CLKTYP, G/T, DCE, PD to GND	-0.3V to the lower of (V_{DD} + 0.3V) and +3.6V
D13–D0, DAV, DOR to GND	-0.3V to (OV_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)	
40-Pin Thin QFN 6mm x 6mm x 0.8mm (derated 26.3mW/°C above +70°C)	2105.3mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering 10s)	+300°C

II. Manufacturing Information

A. Description/Function:	14-Bit, 65 Msps, 3.3V ADC
B. Process:	TC18 (.18 Micron CMOS)
C. Number of Device Transistors:	70,538
D. Fabrication Location:	Taiwan
E. Assembly Location:	Thailand
F. Date of Initial Production:	July, 2004

III. Packaging Information

A. Package Type:	**40-Pin Thin QFN**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-Filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-9000-1746
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	134 x 124 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	
F. Minimum Metal Spacing:	
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Managing Director of QA**)**

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 96 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 11.45 \times 10^{-9}$

λ = 11.45 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-7140) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N** & **RR-B3A)**

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The CA15-1 die type has been found to have all pins able to withstand a transient pulse of ±2500V JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of ±250mA.

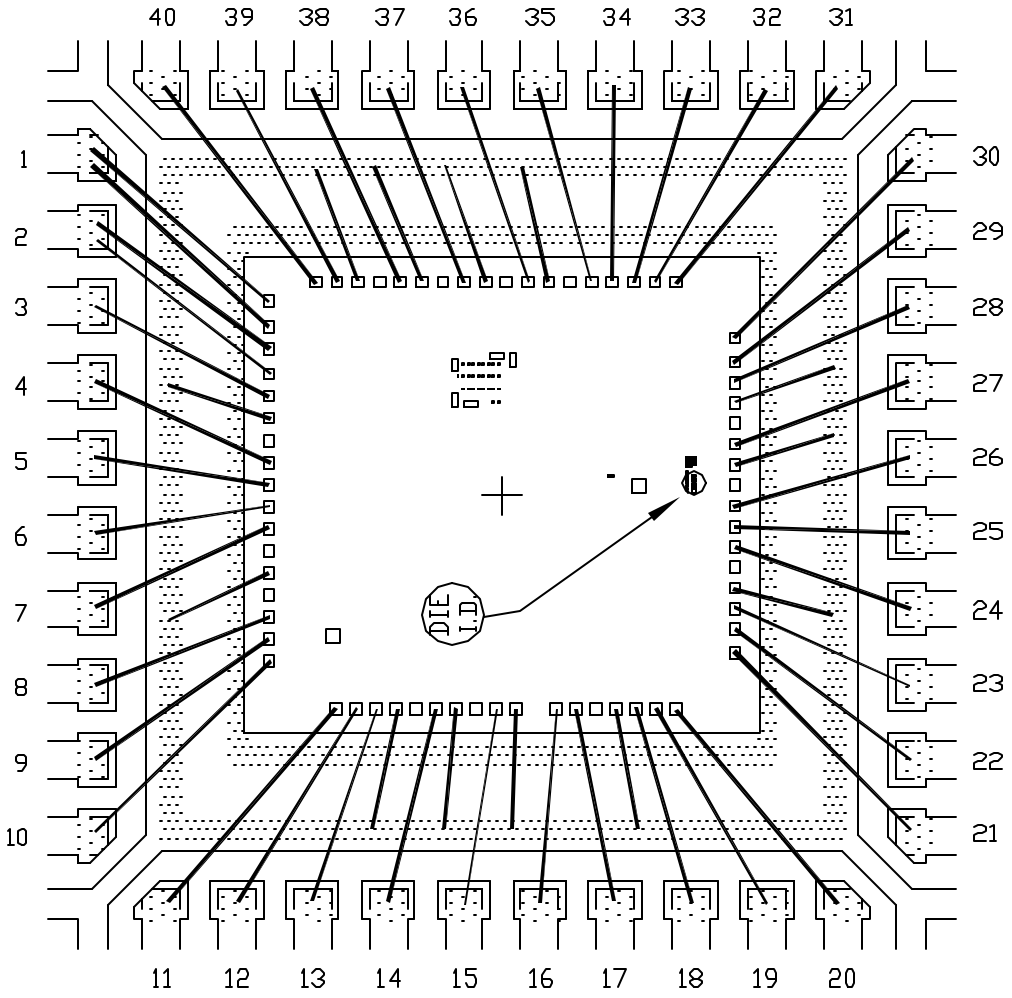
Table 1
Reliability Evaluation Test Results

MAX12553ETL

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		96	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	Thin QFN	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

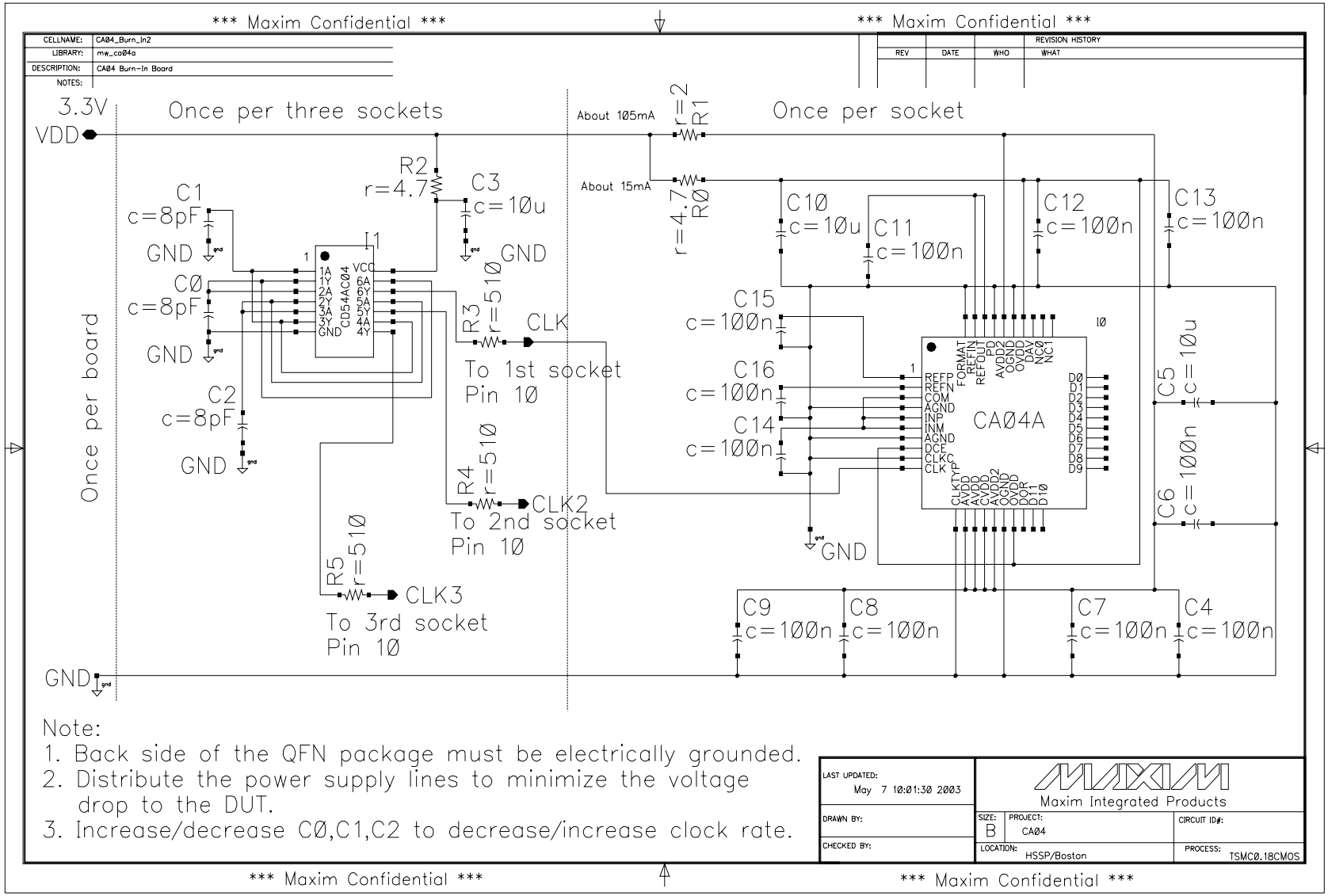
Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

6x6x0.8mm THIN QFN PKG. EXPOSED PAD PKG.



BONDABLE AREA

PKG. CODE: T4066-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 185x185	PKG.			BOND DIAGRAM #: 05-9000-1746	REV: A
	DESIGN				


*** Maxim Confidential ***
*** Maxim Confidential ***
CELLNAME: CA04_Burn_In2
LIBRARY: mw_ca04a
DESCRIPTION: CA04 Burn-In Board
NOTES:
REVISION HISTORY
REV DATE WHO WHAT
3.3V
VDD
Once per three sockets
Once per board
About 105mA
About 15mA
Once per socket
R1 r=2
R0 r=4.7
R2 r=4.7
C3 c=10u
C1 c=8pF
C0 c=8pF
C2 c=8pF
GND
U1
CD54AC04
VCC
1A 1Y 2A 2Y 3A 3Y GND
6A 6Y 5A 5Y 4A 4Y
R3 r=510
R4 r=510
R5 r=510
CLK
CLK2
CLK3
To 1st socket Pin 10
To 2nd socket Pin 10
To 3rd socket Pin 10
C10 c=10u
C11 c=100n
C12 c=100n
C13 c=100n
C15 c=100n
C16 c=100n
C14 c=100n
C5 c=10u
C6 c=100n
C9 c=100n
C8 c=100n
C7 c=100n
C4 c=100n
CA04A
REFP REFN COM AGND INP INM AGND DCE CLKO CLK
FORMAT REFIN REFOUT PD AVDD2 CGND OVDD DAV NC1
CLKTYP AVDD AVDD CVDD2 CGND OVDD D0R D11 D10
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9
Note:
1. Back side of the QFN package must be electrically grounded.
2. Distribute the power supply lines to minimize the voltage drop to the DUT.
3. Increase/decrease C0,C1,C2 to decrease/increase clock rate.
LAST UPDATED: May 7 10:01:30 2003
DRAWN BY:
CHECKED BY:
Maxim Integrated Products
SIZE: B
PROJECT: CA04
CIRCUIT ID#:
LOCATION: HSSP/Boston
PROCESS: TSMC0.18CMOS
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