RELIABILITY REPORT

FOR

MAX1396ETB+

PLASTIC ENCAPSULATED DEVICES

June 27, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Conclusion

The MAX1396ETB+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX1393/MAX1396 micropower, serial-output, 12-bit, analog-to-digital converters (ADCs) operate with a single power supply from +1.5V to +3.6V. These ADCs feature automatic shutdown, fast wake-up, and a highspeed 3-wire interface. Power consumption is only 0.734mW (VDD = +1.5V) at the maximum conversion rate of 312.5ksps. AutoShutdown(tm) between conversions reduces power consumption at slower throughput rates. The MAX1393/MAX1396 require an external reference VREF that has a wide range from 0.6V to VDD. The MAX1393 provides one true-differential analog input that accepts signals ranging from 0 to VREF (unipolar mode) or ±VREF/2 (bipolar mode). The MAX1396 provides two single-ended inputs that accept signals ranging from 0 to VREF. Analog conversion results are available through a 5MHz 3-wire SPI(tm)-/QSPI(tm)-/MICROWIRE(tm)-/digital signal processor (DSP)-compatible serial interface. Excellent dynamic performance, low voltage, low power, ease of use, and small package sizes make these converters ideal for portable battery-powered data-acquisition applications, and for other applications that demand low power consumption and minimal space. The MAX1393/MAX1396 are available in a space-saving (3mm x 3mm) 10-pin TDFN package. The parts operate over the extended (-40°C to +85°C) temperature range.

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II. Manufacturing Information

A. Description/Function:	1.5V to 3.6V, 312.5ksps, 1-Channel True-Differential/2-Channel Single-Ended, 12-Bit, SAR ADCs
B. Process:	S4
C. Number of Device Transistors:	
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	China, Thailand, or Malaysia
F. Date of Initial Production:	April 23, 2005

III. Packaging Information

A. Package Type:	10-pin TDFN 3x3
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1450
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8.5°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8.5°C/W

IV. Die Information

A. Dimensions:	57 X 44 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 95 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.6 \times 10^{-9}$

λ = 11.6 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.13 @ 25C and 2.31 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (ESD lot SWL0BQ001H D/C 0631, Latch-Up lot SWL0AZ001B D/C 0436)

The AC68 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2000V per JEDEC JESD22-A114
ESD-CDM:	+/-750V per JEDEC JESD22-C101
ESD-MM:	+/-200V per JEDEC JESD22/A115

Latch-Up testing has shown that this device withstands a current of +/-250mA.

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Table 1
Reliability Evaluation Test Results

MAX1396ETB+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	48	0	SWL0BQ001D, D/C 0631
	Biased	& functionality	47	0	SWL0AZ001B, D/C 0436
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.

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