

RELIABILITY REPORT
FOR
MAX1402xAI
PLASTIC ENCAPSULATED DEVICES

October 28, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX1402 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1402 low-power, multichannel, serial-output analog-to-digital converter (ADC) features matched 200 μ A current sources for sensor excitation. This ADC uses a sigma-delta modulator with a digital decimation filter to achieve 16-bit accuracy. The digital filter's user-selectable decimation factor allows the conversion resolution to be reduced in exchange for a higher output data rate. True 16-bit performance is achieved at an output data rate of up to 480sps. In addition, the modulator sampling frequency may be optimized for either lowest power dissipation or highest throughput rate. The MAX1402 operates from a +5V supply. This device offers three fully differential input channels that may be independently programmed with a gain between +1V/V and +128V/V. Furthermore, it can compensate an input-referred DC offset up to 117% of the selected full-scale range. These three differential channels may also be configured to operate as five pseudo-differential input channels. Two additional, fully differential system-calibration channels are provided for gain and offset error correction. The MAX1402 may be configured to sequentially scan all signal inputs and provide the results via the serial inter-face with minimum communications overhead. When used with a 2.4576MHz or 1.024MHz master clock, the digital decimation filter can be programmed to produce zeros in its frequency response at the line frequency and associated harmonics, ensuring excellent line rejection without the need for further post-filtering. The MAX1402 is available in a 28-pin SSOP package.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
V+ to AGND, DGND	-0.3V to +6V
VDD to AGND, DGND	-0.3V to +6V
AGND to DGND	-0.3V to +0.3V
Analog Inputs to AGND	-0.3V to (V+ + 0.3V)
Analog Outputs to AGND	-0.3V to (V+ + 0.3V)
Reference Inputs to AGND	-0.3V to (V+ + 0.3V)
CLKIN and CLKOUT to DGND	-0.3V to (V _{DD} + 0.3V)
All Other Digital Inputs to DGND	-0.3V to +6V
All Digital Outputs to DGND	-0.3V to (V _{DD} + 0.3V)
Maximum Current Input into Any Pin	50mA
Continuous Power Dissipation (TA = +70°C)	
28-Pin SSOP	524mW
Derates above +70°C	
28-Pin SSOP	9.52mW/°C
Operating Temperature Ranges	
MAX1402CAI	0°C to +70°C
MAX1402EAI	-40°C to +85°C
Storage Temperature Range	-60°C to +150°C
Lead Temperature (soldering, 10sec)	+300°C

II. Manufacturing Information

- A. Description/Function: +5V, 18-Bit, Low-Power, Multichannel, Over sampling (Sigma-Delta) ADC
- B. Process: S12 (Standard 1.2 micron silicon gate CMOS)
- C. Number of Device Transistors: 34,648
- D. Fabrication Location: California or Oregon, USA
- E. Assembly Location: Philippines or Malaysia
- F. Date of Initial Production: January, 1999

III. Packaging Information

- A. Package Type: **28-PinSSOP**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate
- D. Die Attach: Silver-filled Epoxy
- E. Bondwire: Gold (1.3 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: # 05-0101-0454
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

- A. Dimensions: 144 x 247 mils
- B. Passivation: $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 1.2 microns (as drawn)
- F. Minimum Metal Spacing: 1.2 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO_2
- I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{4.04}{192 \times 4389 \times 80 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

\triangle Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 29.97 \times 10^{-9}$$

$$\lambda = 29.97 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5304) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AD80-3 die type has been found to have all pins able to withstand a transient pulse of $\pm 400\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$.

Table 1
Reliability Evaluation Test Results

MAX1402xAI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	1
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

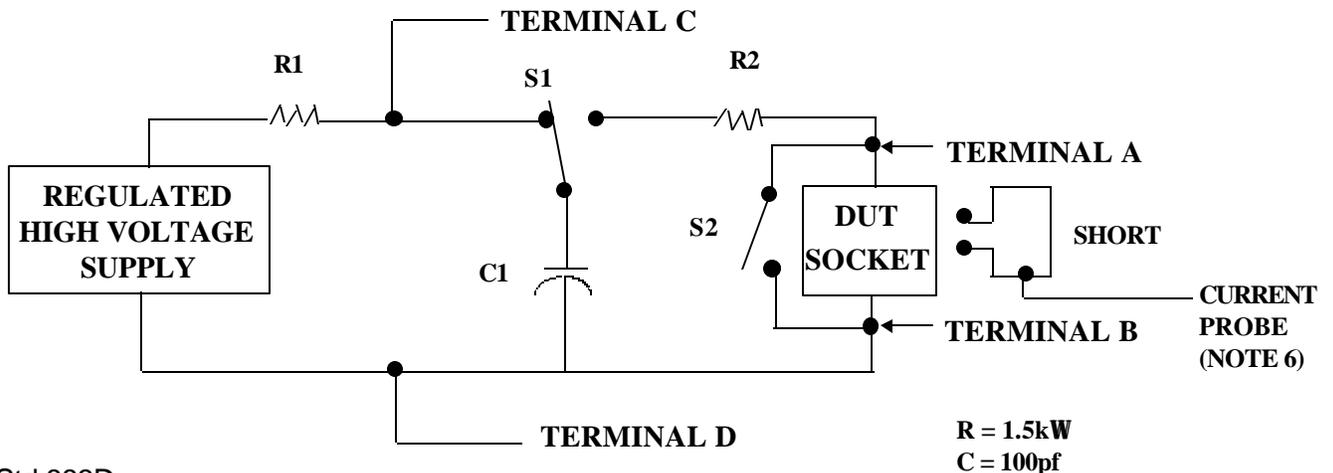
2/ No connects are not to be tested.

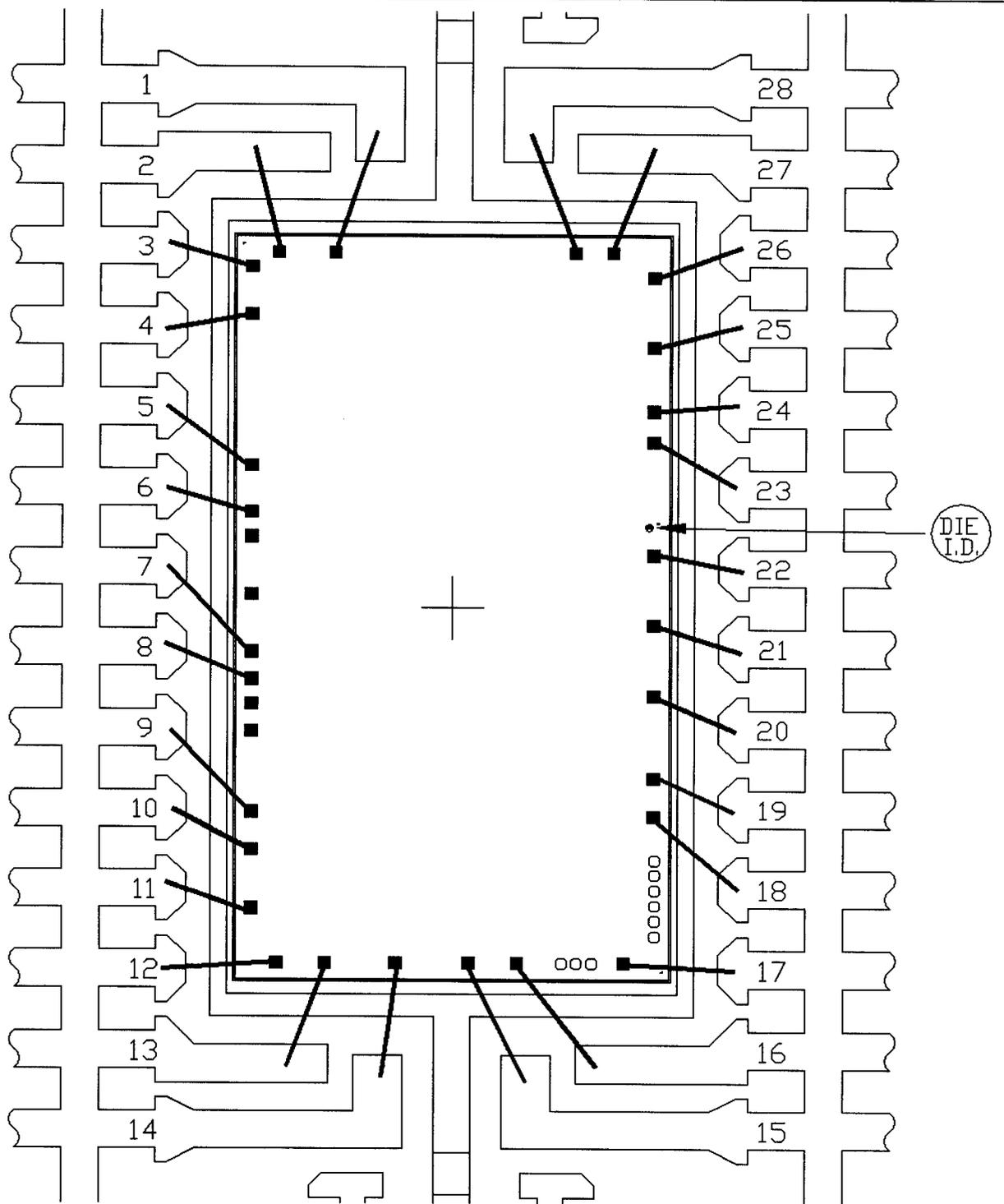
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: A28-2

CAV./PAD SIZE:
154X260

PKG.
DESIGN

APPROVALS

DATE

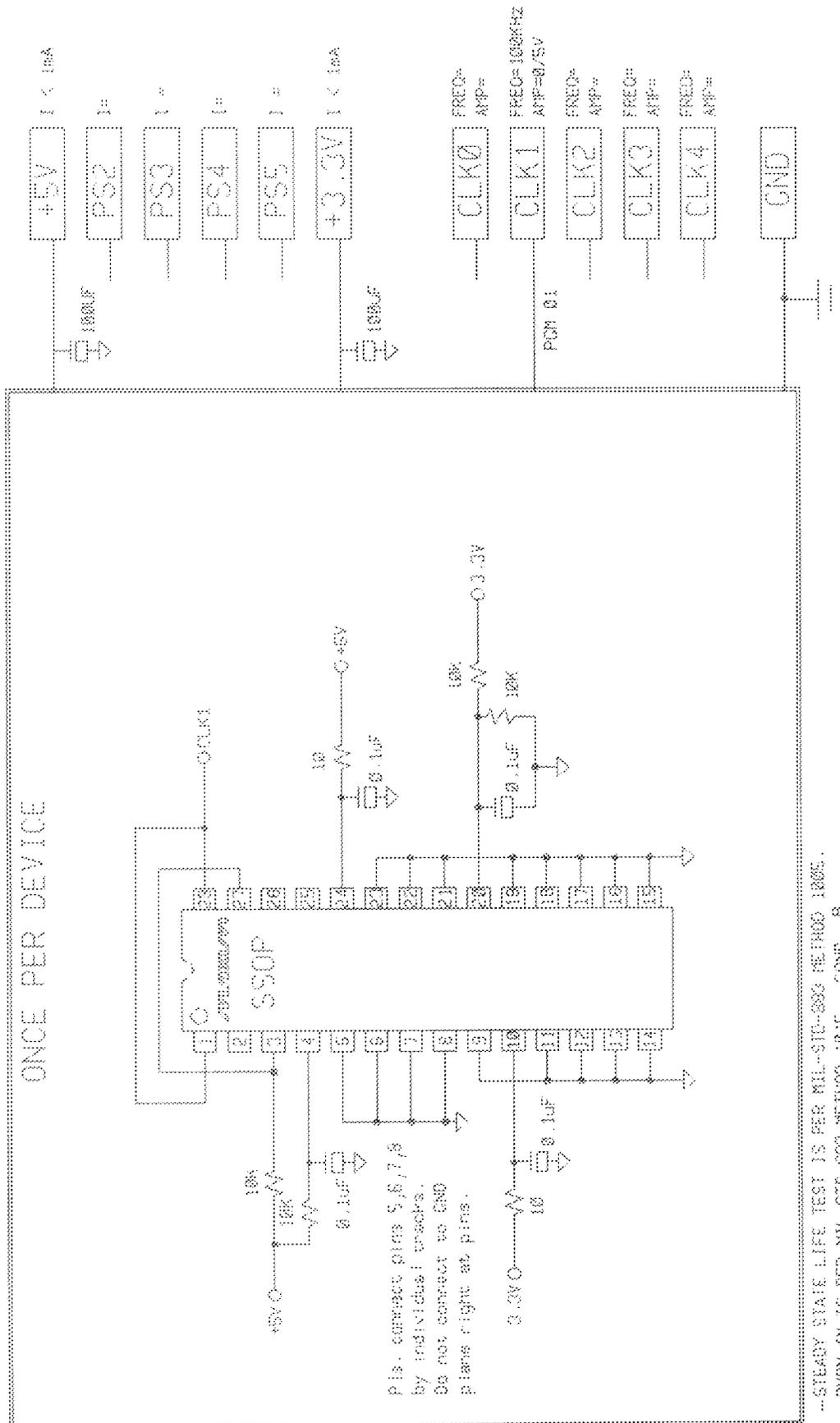
MAXIM

BUILD SHEET NUMBER:
05-0101-0454

REV.:
A

ONCE PER BOARD

ONCE PER DEVICE



Pls. connect pins 5,6,7,8 by individual tracks. Do not connect to GND plane right at pins.

--STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
 --BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. B

NOTES :

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR EXJ COMMERCIAL EXJ HR/883

SPEC. NO. 06-5304 REV: A

DATE: 7/20/97

DRAWN BY:

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE(G): ALSO REFERENCE 06-9388

MAX1400/1/2/3