RELIABILITY REPORT

FOR

MAX14591ETA+

PLASTIC ENCAPSULATED DEVICES

November 25, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX14591ETA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14591 is a dual-channel, bidirectional logic-level translator with the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, VCC and VL, set the logic levels on either side of the device. A logic signal present on the VL side of the device appears as the same logic signal on the VCC side of the device, and vice-versa. The device is optimized for the I²C bus as well as the management data input/output (MDIO) bus where often high-speed, open-drain operation is required. When TS-bar is high, the device allows the pullup to be connected to the I/O port that has the power. This allows continuous I²C operation on the powered side without any disruption while the level translation function is off. The part is specified over the extended -40°C to +85°C temperature range, and is available in 8-bump WLP and 8-pin TDFN packages.

II. Manufacturing Information

A. Description/Function:	High-Speed, Open-Drain Capable Logic-Level Translator
B. Process:	S18
C. Number of Device Transistors:	2410
D. Fabrication Location:	California
E. Assembly Location:	Thailand
F. Date of Initial Production:	December 21, 2011

III. Packaging Information

A. Package Type:	8L TDFN
B. Lead Frame:	Copper
C. Lead Finish:	NiPd
D. Die Attach:	Non-conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4531
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	N/A
K. Single Layer Theta Jc:	N/A
L. Multi Layer Theta Ja:	162°C/W
M. Multi Layer Theta Jc:	20°C/W

IV. Die Information

A. Dimensions:	65.35X34.25 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{240 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 11.0 \times 10^{-9}$

$\lambda = 11.0$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (lot S1ZZAQ001C, D/C 1119)

The LT17 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of+/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX14591ETA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 240 hrs.	DC Parameters & functionality	80	0	S1ZZAQ001C, D/C 1119

Note 1: Life Test Data may represent plastic DIP qualification lots.