RELIABILITY REPORT

FOR

MAX14611ETD+T

PLASTIC ENCAPSULATED DEVICES

April 18, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
Sokhom Chum
Quality Assurance
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Conclusion

The MAX14611ETD+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX14611 is a quad bidirectional logic-level translator that provides the level shifting necessary to allow data transfer in a multivoltage system. Externally applied voltages, VCC and VL, set the logic levels on either side of the device. A low-voltage logic signal present on the VL side of the device appears as a high-voltage logic signal on the VCC side of the device, and vice-versa. The device is ideal for I²C bus as well as MDIO bus applications where open-drain operation is often required. The device features a three-state output mode (active-low TS). Drive active-low TS high to connect the pullup to the powered I/O port. This allows for continuous, undisrupted I²C operation on the powered side of the device while the level translation function is off. The MAX14611 is a pin-to-pin compatible upgrade to the MAX3378E in the TDFN package. The MAX14611 features enhanced high-electrostatic-discharge (ESD) protection on all I/OVCC_ ports up to ±6kV HBM. The device operates over the -40°C to +85°C extended temperature range and is available in 3mm x 3mm, 14-pin TDFN and 4.9mm x 5.1mm, 14-pin TSSOP packages.

II. Manufacturing Information

A. Description/Function:	Quad Bidirectional Low-Voltage Logic-Level Translator
B. Process:	S18
C. Number of Device Transistors:	2213
D. Fabrication Location:	California
E. Assembly Location:	Taiwan
F. Date of Initial Production:	April 10, 2012

III. Packaging Information

A. Package Type:	14L TDFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Cu (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4652
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	1
J. Single Layer Theta Ja:	54°C/W
K. Single Layer Theta Jc:	8°C/W
L. Multi Layer Theta Ja:	41°C/W
M. Multi Layer Theta Jc:	8°C/W

IV. Die Information

A. Dimensions:	31.8898X49.6063 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18um
F. Minimum Metal Spacing:	0.18um
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25C and 0.93 @ 55C (0.8 eV, 60% UCL).

B. E.S.D. and Latch-Up Testing (SACU1Q001D, D/C 1148)

The LT18-0 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX14611ETD+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	SACU1Q001D, D/C 1149

Note 1: Life Test Data may represent plastic DIP qualification lots.