

RELIABILITY REPORT
FOR
MAX14746BEWA+
WAFER LEVEL DEVICES

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## **MAXIM INTEGRATED**

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#### Conclusion

The MAX14746BEWA+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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#### I. Device Description

#### A. General

The MAX14746/MAX14747 are a series of USB charger detectors with an integrated Smart Power Selector(tm) linear charger solutions that provide a single-chip solution for charging and charger detection.

The MAX14746/MAX14747 charger detectors are compliant to USB Battery Charger Detection Rev 1.2\* and capable of detecting multiple USB battery-charging methods, including Standard Downstream Ports (SDP), Charging Downstream Ports (CDP), and Dedicated Charger Ports (DCP). The devices also detect common proprietary charge adapters, including those from Apple.

The MAX14746/MAX14747 battery chargers feature Smart Power Selector operation, allowing operation with dead or no battery present. The devices limits USB VBUS current based on the detect charger source type. If the charger power source is unable to supply the entire system load, the smart-power control circuit supplements the system load with current from the battery.

The devices protect against overvoltage faults up to 28V.

This series of USB charger detectors are available with several options, with slight variations in, for example, power-up states. These variations are noted throughout this data sheet.

There are five options available with slight variations in, for example, power-up states. The devices are available in a 25-ball, 0.4mm pitch wafer-level package (WLP), and are specified over the -40°C to +85°C extended temperature range.



## II. Manufacturing Information

A. Description/Function: USB Detection with Smart Power Selector Li+ Chargers

B. Process: S18
C. Number of Device Transistors: 77294
D. Fabrication Location: USA
E. Assembly Location: Taiwan

F. Date of Initial Production: December 18, 2015

## III. Packaging Information

A. Package Type: 25-bump WLP

B. Lead Frame: N/AC. Lead Finish: N/AD. Die Attach: None

E. Bondwire: N/A (N/A mil dia.)

F. Mold Material: NoneG. Assembly Diagram: #05-100114H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity Level 1

per JEDEC standard J-STD-020-C

J. Single Layer Theta Ja: N/A°C/W
K. Single Layer Theta Jc: N/A°C/W
L. Multi Layer Theta Ja: 52°C/W
M. Multi Layer Theta Jc: N/A°C/W

#### IV. Die Information

A. Dimensions: 81.8897X81.8897 mils

B. Passivation: Si<sub>3</sub>N<sub>4</sub>/SiO<sub>2</sub> (Silicon nitride/ Silicon dioxide)

C. Interconnect: AI/0.5%Cu with Ti/TiN Barrier

D. Backside Metallization: None

E. Minimum Metal Width: 0.23 microns (as drawn)F. Minimum Metal Spacing: 0.23 microns (as drawn)

G. Isolation Dielectric: SiO<sub>2</sub>H. Die Separation Method: Wafer Saw



#### V. Quality Assurance Information

A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)

Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.

0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm</li>D. Sampling Plan: Mil-Std-105D

#### VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (3.) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$
 (Chi square value for MTTF upper limit) 
$$\frac{192 \times 4340 \times 80 \times 2}{\text{(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)}}$$
 
$$\lambda = 13.7 \times 10^{-9}$$

λ = 13.7 x 10° λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

## B. E.S.D. and Latch-Up Testing

The AL99-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.



# **Table 1**Reliability Evaluation Test Results

## MAX14746BEWA+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS	
Static Life Test (Note 1)						
	Ta = 135C	DC Parameters	80	0		
	Biased	& functionality				
	Time = 192 hrs.					

Note 1: Life Test Data may represent plastic DIP qualification lots.