RELIABILITY REPORT

FOR

MAX14748EWW+T

WAFER LEVEL DEVICES

November 13, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX14748EWW+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14748 USB battery charger integrates a charger detector, boost/buck converter, and Li+ battery charger with smart power selector to provide fast and safe charging of 2s Li+ battery packs. The MAX14748 provides support for devices functioning as a UFP/DRP per the USB Type-C 1.1 standard, while also providing detection of legacy USB Battery Charging Specification Revision 1.2 (BC1.2) compliant chargers in addition to other nonstandard chargers. The programmable Automatic Input Current Limiting (AICL) feature ensures that maximum safe current is drawn from the charging adapter. The Li+ charger includes an automatic Smart Power Selector™ to simultaneously charge the battery and provide power to the system load. The Smart Power Selector function will supplement the system power with the battery if power from the charging adapter is insufficient. The Li+ charger features JEITA thermal monitoring and charger voltage/current reduction or charger disable. The MAX14748 is available in a 54-bump, 0.4mm pitch, 3.97mm x 2.77mm x 0.64mm wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

II. Manufacturing Information

A. Description/Function:	USB Type-C Charger
B. Process:	S18
C. Number of Device Transistors:	216621
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan
F. Date of Initial Production:	June 28, 2017

III. Packaging Information

A. Package Type:	54-bump WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-100443
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	40.88°C/W
M. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Dimensions:	157.4803X110.2362 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AO01-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX14748EWW+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.