RELIABILITY REPORT

FOR

MAX14819ATM+T

PLASTIC ENCAPSULATED DEVICES

April 20, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX14819ATM+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14819 low-power, dual-channel, IO-Link® master transceiver with sensor/actuator power-supply controllers is fully compliant with the latest IO-Link and binary input standards and test specifications, IEC 61131-2, IEC 61131-9 SDCI, and IO-Link 1.1.2. This master transceiver also includes two auxiliary digital input (DI_) channels. The MAX14819 is configurable to operate either with external UARTs or using the integrated framers on the IC. To ease selection of microcontroller, the master transceiver features frame handlers with UARTs and FIFOs. These are designed to simplify time critical control of all IO-Link M-sequence frame types. The MAX14819 also features autonomous cycle timers, reducing the need for accurate controller timing. Integrated establish-communication sequencers also simplify wake-up management. The MAX14819 integrates two low-power sensor supply controllers with advanced current limiting, reverse current blocking, and reverse polarity protection capability to enable low-power robust solutions. The MAX14819 is available in a 48-pin (7mm × 7mm) TQFN package and is specified over the extended -40°C to +125°C temperature range. *IO-Link is a registered trademark of Profibus User Organization (PNO).*

II. Manufacturing Information

A. Description/Function:	Dual IO-Link Master Transceiver with Integrated Framers and L+ Supply Controllers
B. Process:	S18
C. Number of Device Transistors:	184828
D. Fabrication Location:	Japan
E. Assembly Location:	Taiwan
F. Date of Initial Production:	January 3, 2017

III. Packaging Information

A. Package Type:	48-pin TQFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Bondwire:	CuPd (1 mil dia.)
E. Mold Material:	Epoxy with silica filler
F. Assembly Diagram:	#05-100324
G. Flammability Rating:	Class UL94-V0
H. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
I. Single Layer Theta Ja:	36°C/W
J. Single Layer Theta Jc:	1°C/W
K. Multi Layer Theta Ja:	25°C/W
L. Multi Layer Theta Jc:	1°C/W

IV. Die Information

A. Dimensions:	145.6693X145.6693 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 78 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 14.1 \times 10^{-9}$

$\lambda = 14.1$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The RV18-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX14819ATM+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	78	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.