RELIABILITY REPORT

FOR

MAX1490BxPG

Hybrid

April 7, 2004

MAXIM INTEGRATED PRODUCTS

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Conclusion

The MAX1490B successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1490B is a complete, electrically isolated, RS-485/ RS-422 data-communications interface solution in a hybrid microcircuit. Transceivers, optocouplers, and a transformer provide a complete interface in a standard DIP package. A single +5V supply on the logic side powers both sides of the interface.

The MAX1490B features reduced slew-rate drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission at data rates up to 250kbps. The MAX1490B features full-duplex communication.

Drivers are short-circuit current limited and protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into a highimpedance state. The receiver input has a fail-safe feature that guarantees a known output (RO high) if the input is open circuit.

The MAX1490B typically withstands $1600V_{RMS}$ (1 minute) or $2000V_{RMS}$ (1 second). It's isolated outputs meet all RS-485/RS-422 specifications. The MAX1490B is available in a 24-pin DIP package.

B. Absolute Maximum Ratings

Item	Rating
Stresses With Respect to GND_	
Supply Voltage (V_{CC}_)	-0.3V to +6V
Control Input Voltage (SD, FS)	-0.3V to (V_{CC}_ + 0.3V)
Receiver Output Voltage (/RO, RO)	-0.3V to (V_{CC}_ + 0.3V)
Output Switch Voltage (D1, D2)	+12V
With Respect to ISO COM_	
Control Input Voltage (ISO DE_)	-0.3V to (ISO V_{CC}_ + 0.3V)
Driver Input Voltage (ISO DI_)	-0.3V to (ISO V_{CC}_ + 0.3V)
Receiver Output Voltage (ISO RO_)	-0.3V to (ISO V_{CC}_ + 0.3V)
Driver Output Voltage (A, B, Y, Z)	-8V to +12.5V
Receiver Input Voltage (A, B)	-8V to +12.5V
LED Forward Current (DI, DE, ISO RO LED)	50mA
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
24-Pin DIP	696mW
Derates above +70°C	
24-Pin DIP	8.7mW/°C

II. Manufacturing Information

A. Description/Function: Complete, Isolated, RS-485/RS-422 Data Interface

B. Process: S3 (SG3) – Std. 3 micron silicon gate CMOS and M5 (SMG) – Std. 5 micron metal gate CMOS (Hybrid)

C. Number of Device Transistors: 717

D. Fabrication Location: Oregon, USA

E. Assembly Location: Philippines

F. Date of Initial Production: June, 1994

III. Die Information

A. Dimensions: 54 x 80 mils (RS07 Die) and 58 x 85 mils (RS19-1 Die)

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 3 microns (as drawn)

F. Minimum Metal Spacing: 3 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 240 \times 2}$$ (Chi square value for MTTF upper limit)

(4389: Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 4.52 \times 10^{-9}$ λ = 4.52 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5152) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RS34-2 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1490BxPG

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	240	0
Moisture Testing				
Pressure Pot*	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	N/A	N/A
85/85*	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	N/A	N/A
Mechanical Stress				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	231	0

*Note 1: Moisture testing is not performed on Hybrid products.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

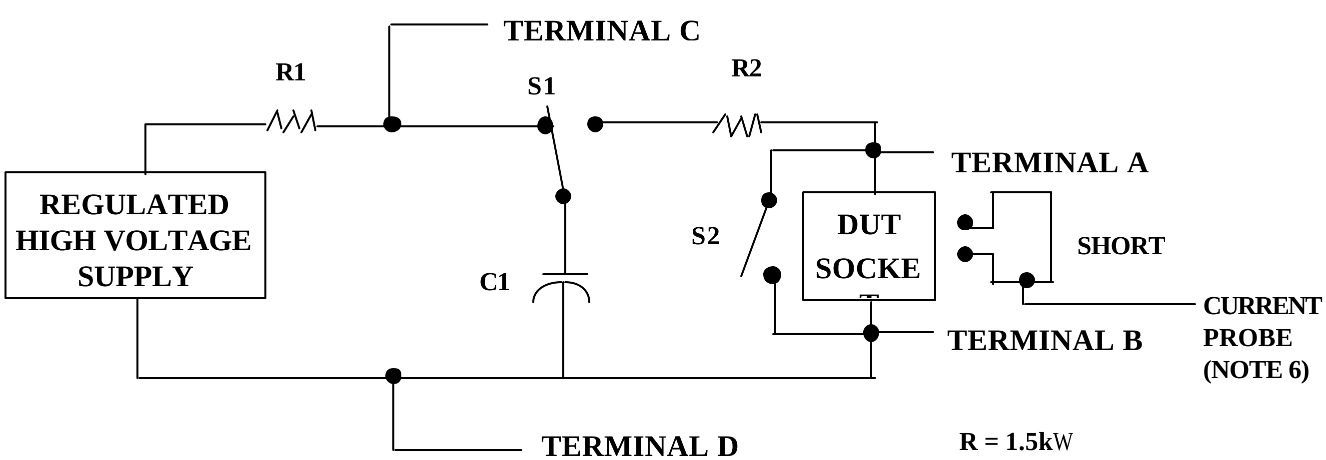
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

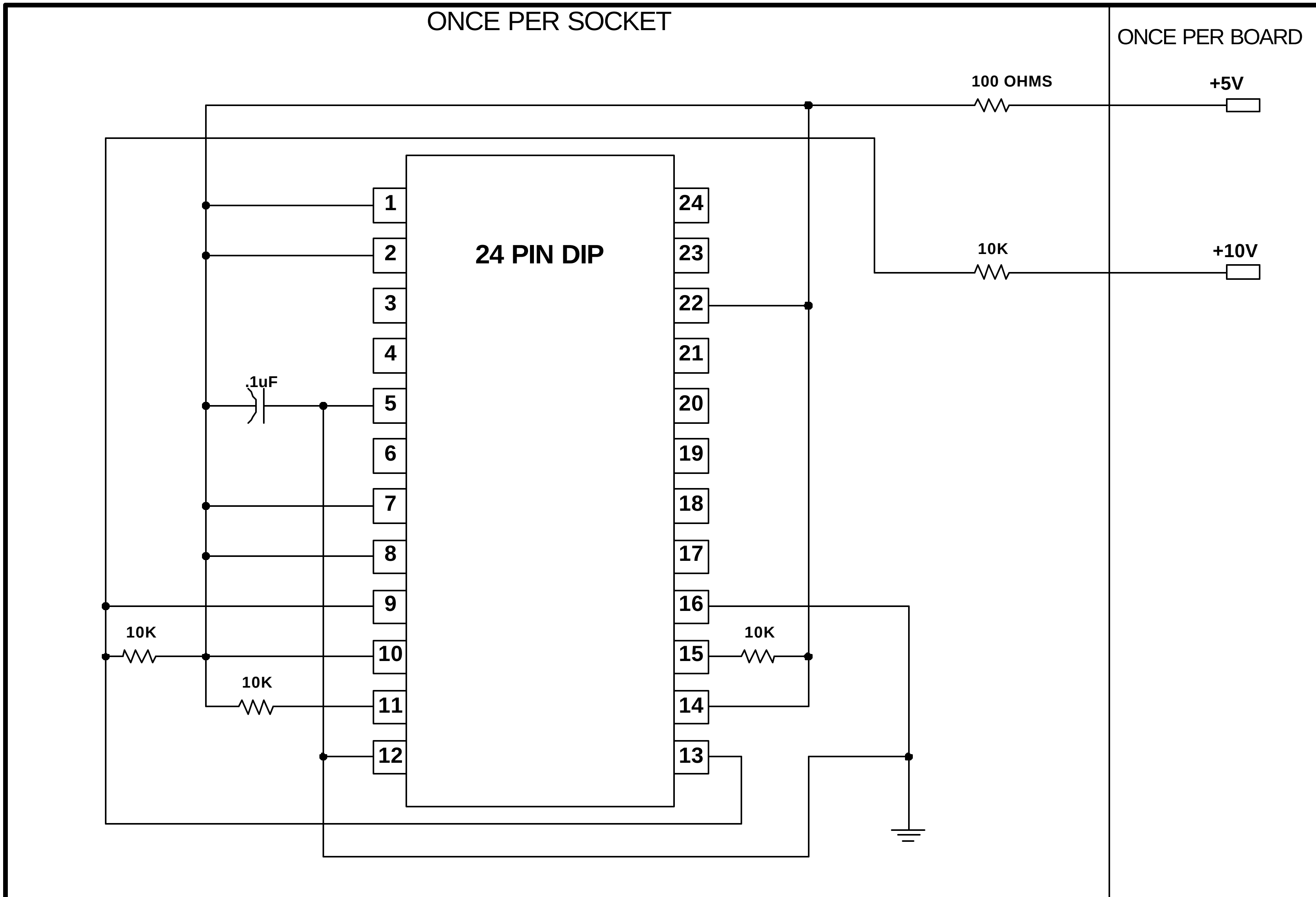
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





DEVICES: MAX 1490 A/B/E
MAX. EXPECTED CURRENT = 1 mA (+5), 0.5 mA (+10)

NOTES: +5 VOLT SUPPLY MAX CURRENT FOR "A" VERSION OF THIS PART IS 18mA.