RELIABILITY REPORT

FOR

MAX14912AKN+T

PLASTIC ENCAPSULATED DEVICES

March 27, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX14912AKN+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX14912/MAX14913 have eight 640mA smart high-side switches that can also be configured as push-pull drivers for high-speed switching. The propagation delay from input to switching of the high-side/low-side drivers is 1µs (max). Each high-side driver has a low on-resistance of 230m (max) at 500mA load current at TA = 125°C. The device is configured and controlled either through pins or the SPI interface. The SPI interface is daisy-chainable, which allows efficient cascading of multiple devices. SPI also supports command mode, for the highest detailed diagnostic information. The MAX14912 allows configuration through SPI in parallel and serial setting modes, while the MAX14913 only supports configuration through SPI in serial setting mode. Open-load detection in high-side mode detects both open-wire conditions in the switch on/off states, and LED drivers provide indication of per-channel fault and status conditions. Internal active clamps accelerate the shutdown of inductive loads fast in high-side mode. The MAX14912/MAX14913 are available in a 56-pin QFN 8mm x 8mm package.

II. Manufacturing Information

A. Description/Function:	Octal High-Speed, High-Side Switch/Push-Pull Driver
B. Process:	S18
C. Number of Device Transistors:	44000
D. Fabrication Location:	Japan
E. Assembly Location:	Taiwan
F. Date of Initial Production:	January 17, 2017

III. Packaging Information

A. Package Type:	56-pin QFN
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-100035
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	35°C/W
K. Single Layer Theta Jc:	1°C/W
L. Multi Layer Theta Ja:	21°C/W
M. Multi Layer Theta Jc:	1°C/W

IV. Die Information

A. Dimensions:	222.0472X234.2519 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The RV05-0 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 2500V per JEDEC JESD22-A114
ESD-CDM: +/- 750V per JEDEC JESD22-C101
ESD-MM: +/- 250V per JEDEC JESD22-A115

Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX14912AKN+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.