

RELIABILITY REPORT  
FOR MAX14933  
PLASTIC ENCAPSULATED DEVICES

June 24, 2016

**MAXIM INTEGRATED**

160 RIO ROBLES  
SAN JOSE, CA 95134

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## Conclusion

The MAX14933AWE+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

## Table of Contents

<b>I. ....Device Description</b>	<b>IV. ....Die Information</b>
<b>II. ....Manufacturing Information</b>	<b>V. ....Quality Assurance Information</b>
<b>III. ....Packaging Information</b>	<b>VI. ....Reliability Evaluation</b>
<b>.....Attachments</b>	

### I. Device Description

#### A. General

The MAX14933 is a two-channel, 2.75kV<sub>RMS</sub> I<sup>2</sup>C digital isolator utilizing Maxim's proprietary process technology. For applications requiring 5kV<sub>RMS</sub> of isolation, refer to the MAX14937 data sheet. The MAX14933 transfers digital signals between circuits with different power domains at ambient temperatures up to +125°C. The device offers two bidirectional, open-drain channels for applications, such as I<sup>2</sup>C, that require data to be transmitted in both directions on the same line. The device features independent 2.25V to 5.5V supplies on each side of the isolator. The device operates from DC to 1.7MHz and can be used in isolated I<sup>2</sup>C busses with clock stretching. The MAX14933 is available in both a 16-pin wide-body (10.3mm x 7.5mm) and narrow-body (9.9mm x 3.9mm) SOIC package. All devices are rated for operation at ambient temperatures of -40°C to +125°C.

## II. Manufacturing Information

A. Description/Function:	Two-Channel, 2.75kVRMS I <sup>2</sup> C Isolator
B. Process:	S18
C. Fabrication Location:	USA
D. Assembly Location:	Taiwan
E. Date of Initial Production:	May 12, 2016

## III. Packaging Information

A. Package Type:	16-pin SOIC (W)	16-pin SOIC (N)
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% Matte Sn	100% Matte Sn
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (1 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 31-4899	# 31-4909
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	N/A°C/W	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W	N/A°C/W
L. Multi Layer Theta Ja:	71°C/W	75°C/W
M. Multi Layer Theta Jc:	23°C/W	24°C/W

## IV. Die Information

A. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
B. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
C. Backside Metallization:	None
D. Minimum Metal Width:	0.23 microns (as drawn)
E. Minimum Metal Spacing:	0.23 microns (as drawn)
F. Bondpad Dimensions:	
G. Isolation Dielectric:	SiO <sub>2</sub>
H. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)  
Bryan Preeshl (Vice President of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% for all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 400 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 2.8 \times 10^{-9}$$

$$\lambda = 2.8 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maximintegrated.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.05 @ 25°C and 0.93 @ 55°C (0.8 eV, 60% UCL)

### B. E.S.D. and Latch-Up Testing

The RU66 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

**Table 1**  
Reliability Evaluation Test Results

**MAX14933AWE+**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
<b>Static Life Test</b> (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	400	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.