

RELIABILITY REPORT  
FOR  
**MAX153xxP**  
PLASTIC ENCAPSULATED DEVICES

April 12, 2003

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Reviewed by



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Executive Director

## Conclusion

The MAX153 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX153 high-speed, microprocessor ( $\mu$ P)-compatible, 8-bit analog-to-digital converter (ADC) uses a half-flash technique to achieve a 660ns conversion time, and digitizes at a rate of 1M samples per second (MSPS). It operates with single +5V or dual  $\pm$ 5V supplies and accepts either unipolar or bipolar inputs. A /POWERDOWN pin reduces current consumption to a typical value of 1 $\mu$ A (with 5V supply). The part returns from power-down to normal operating mode in less than 200ns, providing large reductions in supply current in applications with burst-mode input signals.

The MAX153 is DC and dynamically tested. Its  $\mu$ P interface appears as a memory location or input/output port that requires no external interface logic. The data outputs use latched, three-state buffered circuitry for direct connection to a  $\mu$ P data bus or system input port. The ADC's input/reference arrangement enables ratiometric operation.

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
$V_{DD}$ to GND	-0.3V to +7V
$V_{SS}$ to GND	+0.3V to -7V
Digital Input Voltage to GND	+0.3V, ( $V_{DD} + 0.3V$ )
Digital Output Voltage to GND	-0.3V, ( $V_{DD} + 0.3V$ )
VREF+ to GND	( $V_{SS} - 0.3V$ ) to ( $V_{DD} + 0.3V$ )
VREF- to GND	( $V_{SS} - 0.3V$ ) to ( $V_{DD} + 0.3V$ )
$V_{IN}$ to GND	( $V_{SS} - 0.3V$ ) to ( $V_{DD} + 0.3V$ )
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )	
20-Pin PDIP	889mW
20-Pin SO	800mW
20-Pin SSOP	600mW
Derates above +70°C	
20-Pin PDIP	11.11mW/°C
20-Pin SO	10.0mW/°C
20-Pin SSOP	8.00mW/°C

## II. Manufacturing Information

A. Description/Function:	1 Msps, $\mu$ P-Compatible, 8-Bit ADC with 1 $\mu$ A Powerdown
B. Process:	S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	1856
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Thailand
F. Date of Initial Production:	March, 1992

## III. Packaging Information

A. Package Type:	20 Lead SSOP	20-Lead DIP	20-Lead WSO
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish: Solder Plate	Solder Plate	Solder Plate	Solder Plate
D. Die Attach: Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire: Gold (1.3 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-0101-0346	# 05-0101-0249	# 05-0101-0248
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1	Level 1

## IV. Die Information

A. Dimensions:	98 x 104 mils
B. Passivation:	Si <sub>3</sub> N <sub>4</sub> /SiO <sub>2</sub> (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO <sub>2</sub>
I. Die Separation Method:	Wafer Saw

## V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Director of Reliability)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{4.04}{192 \times 4389 \times 730 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

$\Delta$  Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 3.28 \times 10^{-9} \quad \lambda = 3.28 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-3863) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The AD49-1 die type has been found to have all pins able to withstand a transient pulse of  $\pm 3000\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 150\text{mA}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX153xxP**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test (Note 1)</b>					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		730	1
<b>Moisture Testing (Note 2)</b>					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO	77	0
			PDIP	77	0
			SSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress (Note 2)</b>					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ <u>3/</u>	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.

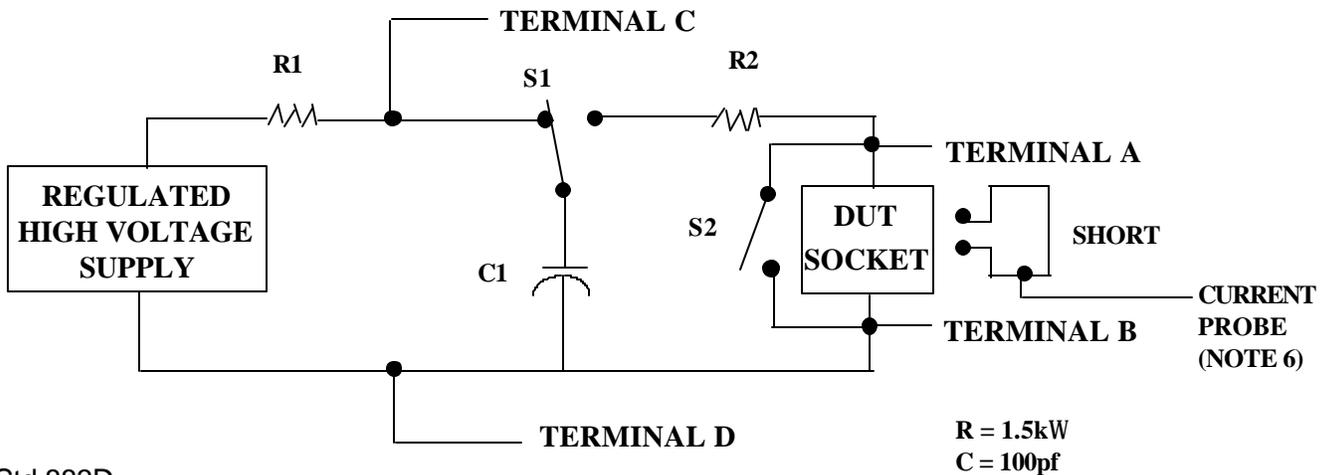
2/ No connects are not to be tested.

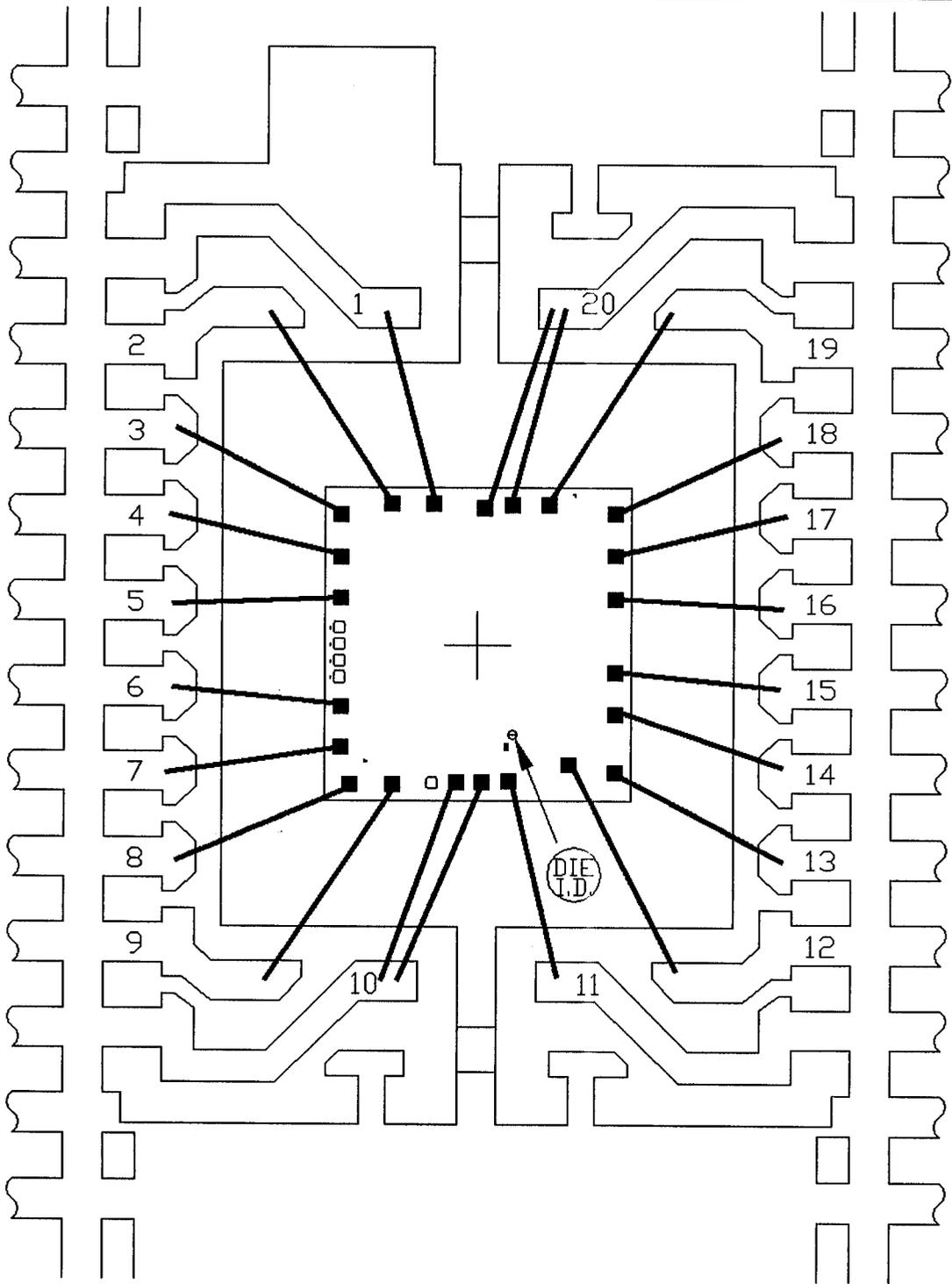
3/ Repeat pin combination I for each named Power supply and for ground

(e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ ,  $GND$ ,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



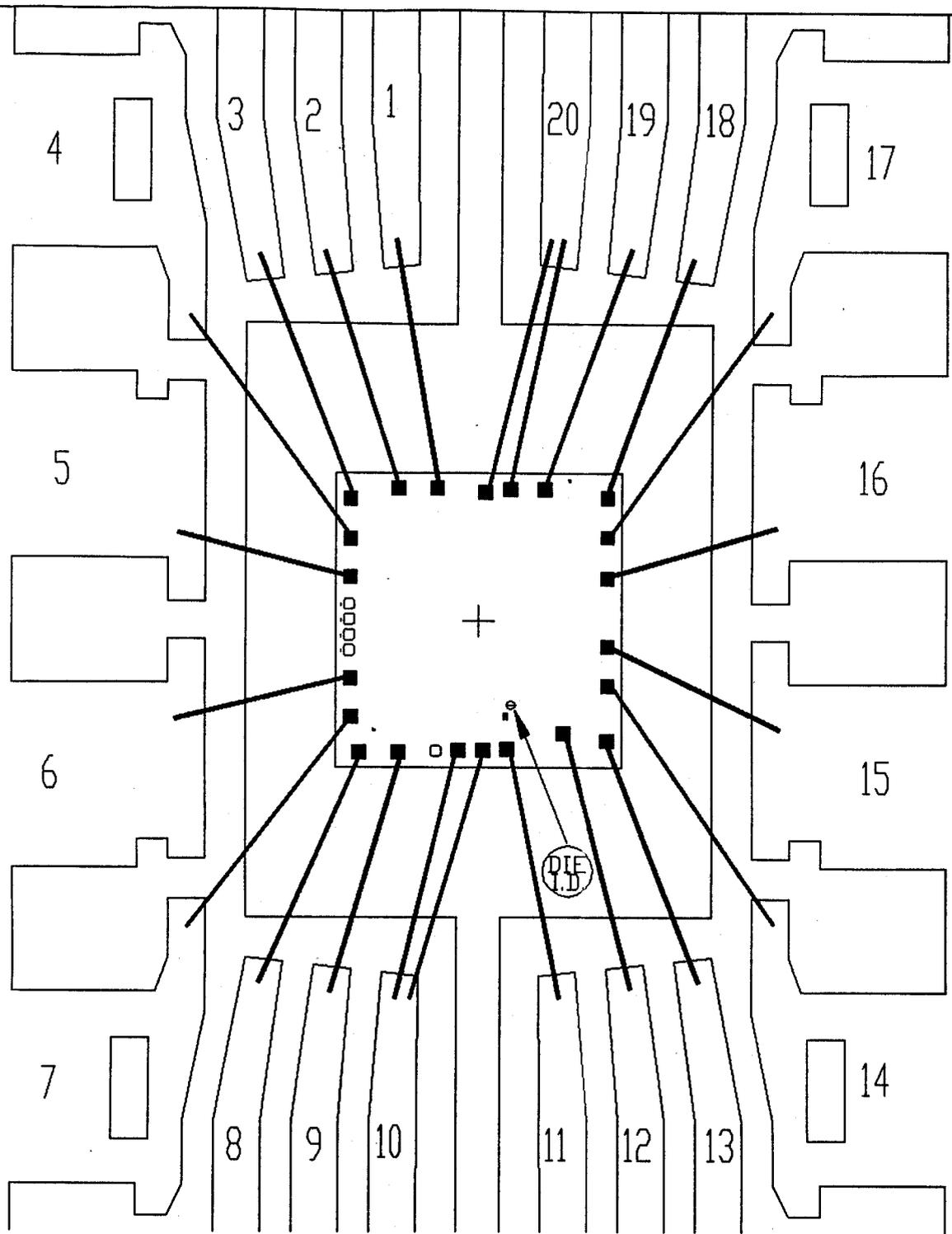


PKG.CODE: A20-1  
 CAV./PAD SIZE: 154X169

APPROVALS  
 PKG. DESIGN

DATE

**MAXIM**  
 BUILDSHEET NUMBER: 05-0101-0346  
 REV.: B



PKG.CODE: P20-3

CAV./PAD SIZE: 150 X 190

PKG.  
DESIGN

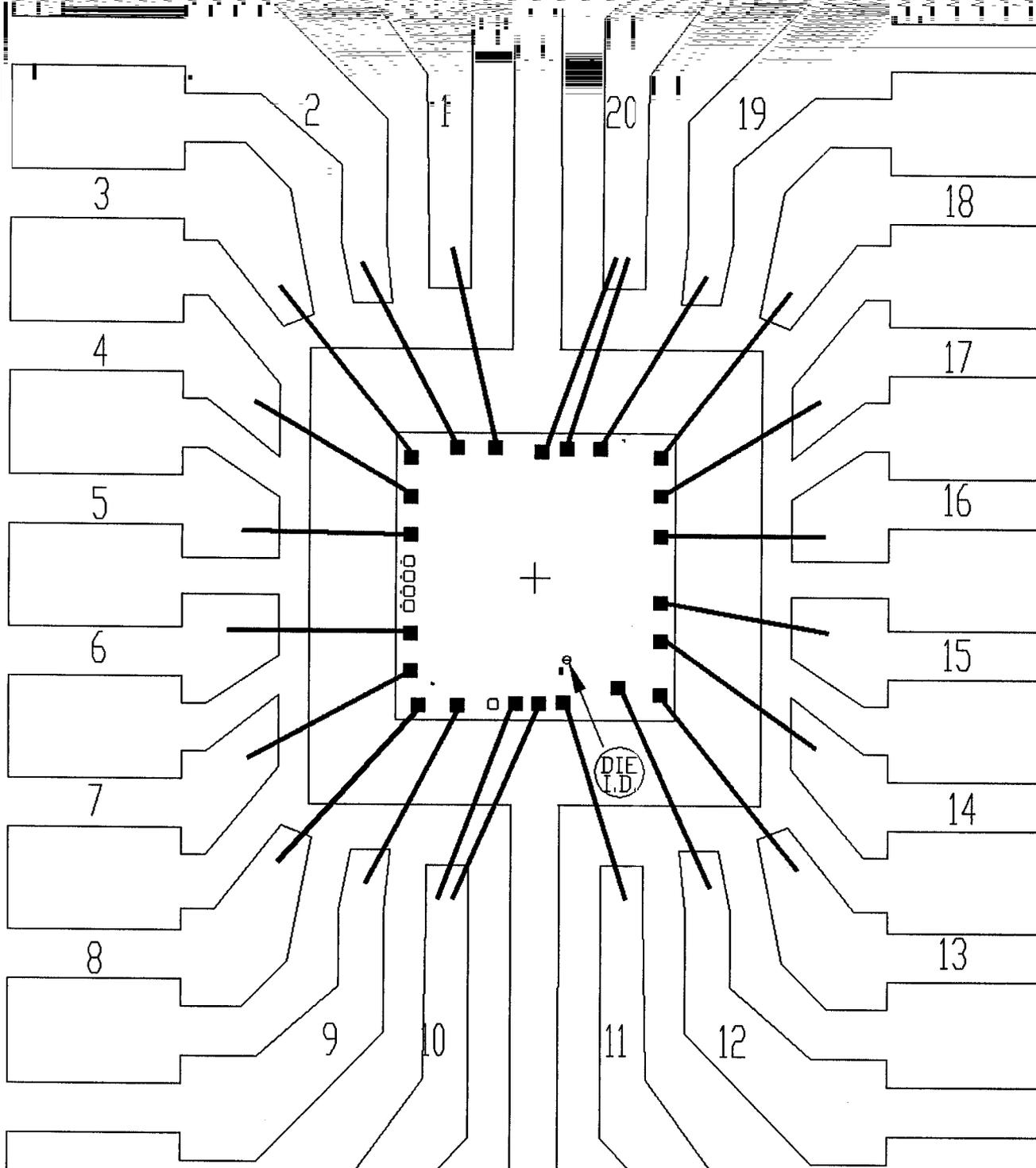
APPROVALS

DATE



BUILDSHEET NUMBER:  
05-0101-0249

REV.:  
B



PKG.CODE: W20-2  
 CAV./PAD SIZE: 150 X 150

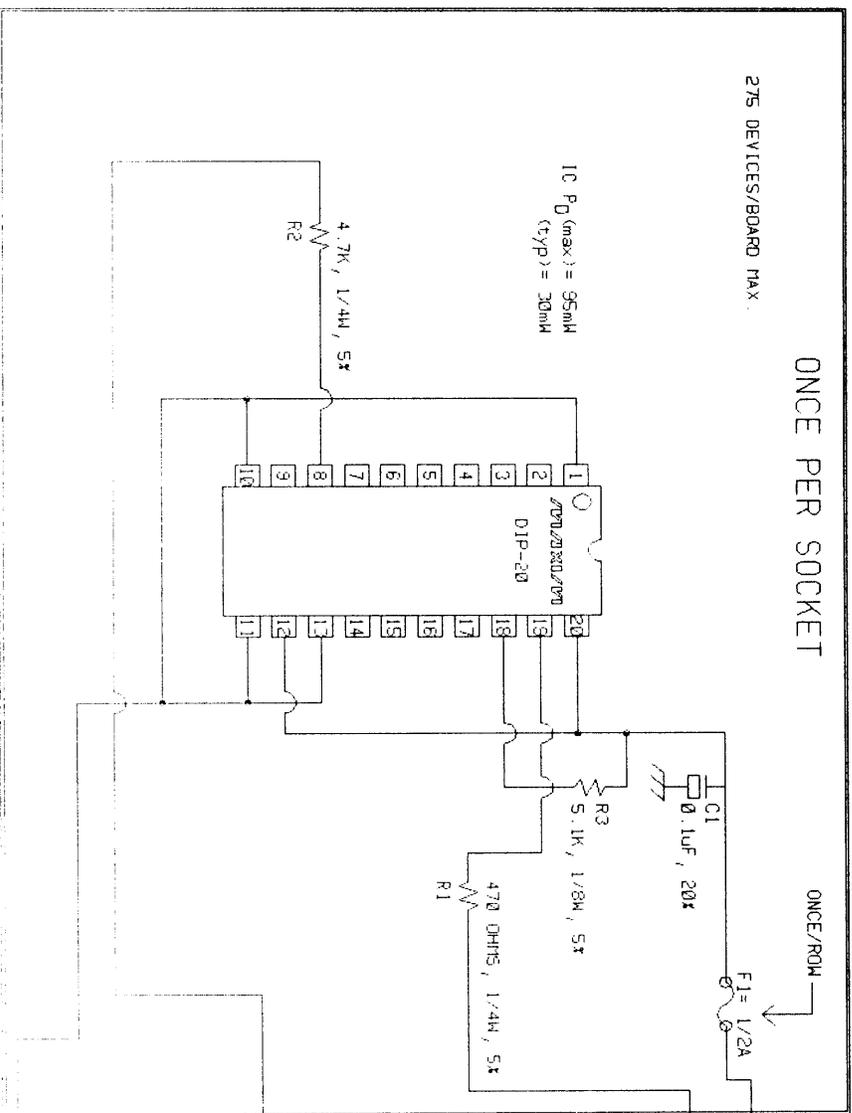
APPROVALS  
 DATE

**MAXI**  
 BUILDSHEET NUMBER:  
 05-0101-0248

PKG.  
 DESIGN

ONCE PER SOCKET

275 DEVICES/BOARD MAX.



IC P<sub>D</sub>(max) = 95mW  
(typ) = 30mW

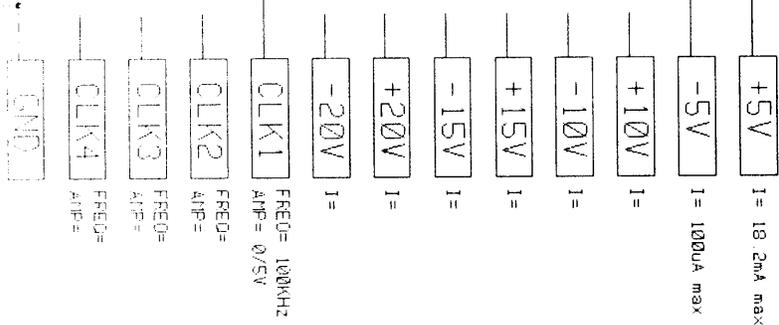
4.7k, 1/4W, 5%

0.1uF, 20%

5.1k, 1/8W, 5%

470 OHMS, 1/4W, 5%

ONCE PER BOARD



+5V I = 18.2mA max

-5V I = 100uA max

+10V I =

-10V I =

+15V I =

-15V I =

+20V I =

-20V I =

CLK1 FREQ= 100KHz AMP= 0/5V

CLK2 FREQ= AMP=

CLK3 FREQ= AMP=

CLK4 FREQ= AMP=

GND

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL [X] HR/883

STEADY STATE LIFE TEST ON MIL-STD-883 METHOD B005  
BURN-IN IS PER MIL-STD-883 METHOD B005

SPEC. NO. 06-3863 REV. B

MAX IN BURN-IN SCHEMATIC

DATE: 2/11/93

DEVICE TYPE:

MX7821, MAX152/153

DRAWN BY: