RELIABILITY REPORT

FOR

MAX1573ExE

PLASTIC ENCAPSULATED/CHIP SCALE DEVICES

September 9, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX1573 sucessfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1573 fractional charge pump drives up to four white LEDs with regulated constant current for uniform intensity. By utilizing proprietary adaptive 1x/1.5x modes and ultra-low-dropout current regulators, it maintains the highest possible efficiency over the full 1-cell Li+ battery input voltage range. The 1MHz fixed-frequency switching allows for tiny external components and the regulation scheme is optimized to ensure low EMI and low input ripple.

An external resistor sets the full-scale LED current, while two digital inputs control on/off and select amongst three levels of brightness. A pulse-width modulation (PWM) signal can also be used to modulate LED brightness, requiring no additional components.

The MAX1573 is available in the tiny chip-scale UCSP™ (4 x 4 grid) and 16-pin thin QFN packages.

B. Absolute Maximum Ratings

Item	Rating
IN, OUT, EN1, EN2 to GND	-0.3V to +6.0V
SET, LED1, LED2, LED3, LED4 to GND	-0.3V to (VIN + 0.3V)
C1N, C2N to GND	-0.3V to (VIN + 1V)
C1P, C2P to GND	-0.3V to greater of (VOUT + 1V) or (VIN + 1V)
OUT Short Circuit to GND	Continuous
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Continuous Power Dissipation (TA = +70°C)	
16-Pin Thin QFN	1349mW
14-Bump UCSP	589mW
Derates above +70°C	
16-Pin Thin QFN	16.9mW/°C
14-Bump UCSP	7.36mW/°C

II. Manufacturing Information

A. Description/Function:	White LED 1x/1.5x Charge Pump in UCSP and Thin QFN
B. Process:	S8
C. Number of Device Transistors:	3665
D. Fabrication Location:	California, USA
E. Assembly Location:	Philippines, Thailand or USA
F. Date of Initial Production:	April, 2003

III. Packaging Information

A. Package Type:	**16-Lead QFN (4 x 4)**	**14-Bump UCSP**
B. Lead Frame:	Copper	N/A
C. Lead Finish:	Solder Plate	N/A
D. Die Attach:	Silver-Filled Epoxy	N/A
E. Bondwire:	Gold (1.0 mil dia.)	N/A
F. Mold Material:	Epoxy with silica filler	N/A
G. Assembly Diagram:	# 05-9000-0658	# 05-9000-0484
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	83 x 83 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Manager, Rel Oprations)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

192 — Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 22.62 \times 10^{-9}$ $\lambda = 22.62$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-6187) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PN06 die type has been found to have all pins able to withstand a transient pulse of 2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1573ExE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		48	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uMAX UCSP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	uMAX UCSP	77 N/A	0 N/A
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010 (Note 3)	DC Parameters & functionality	uMAX UCSP	77 77	0 0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
Note 3: UCSP Temperature Cycle performed at -40°C/125°C, 1000 Cycles, ramp rate 11°C/minute, dwell=15 minutes, One cycle/hour

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

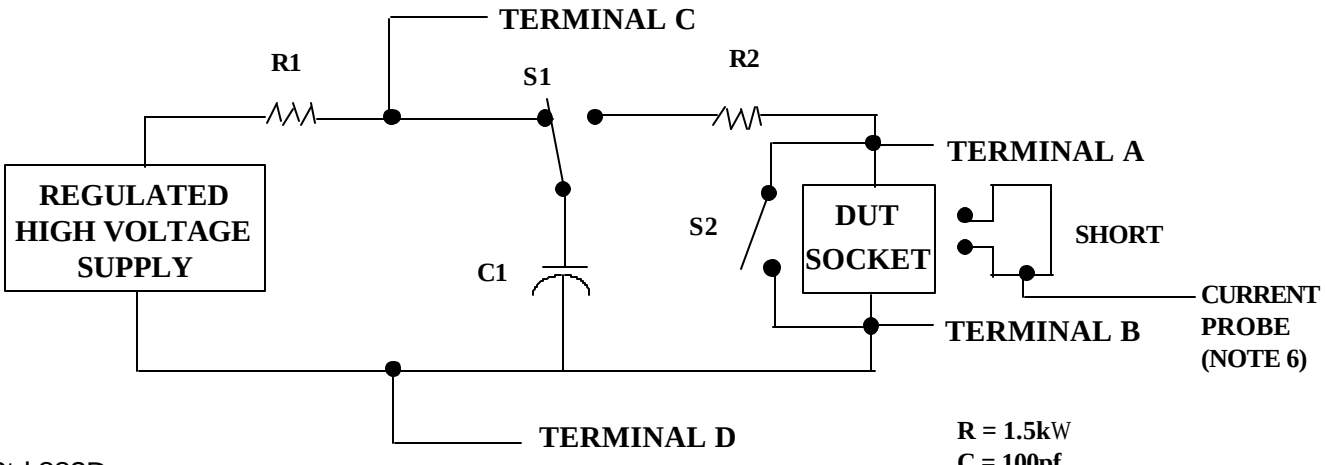
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

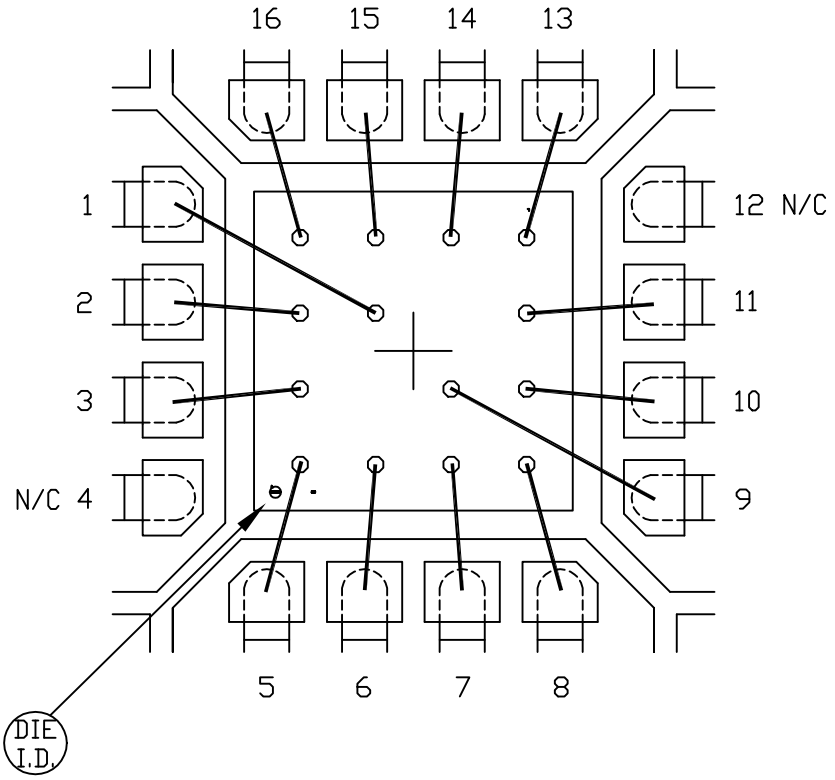
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

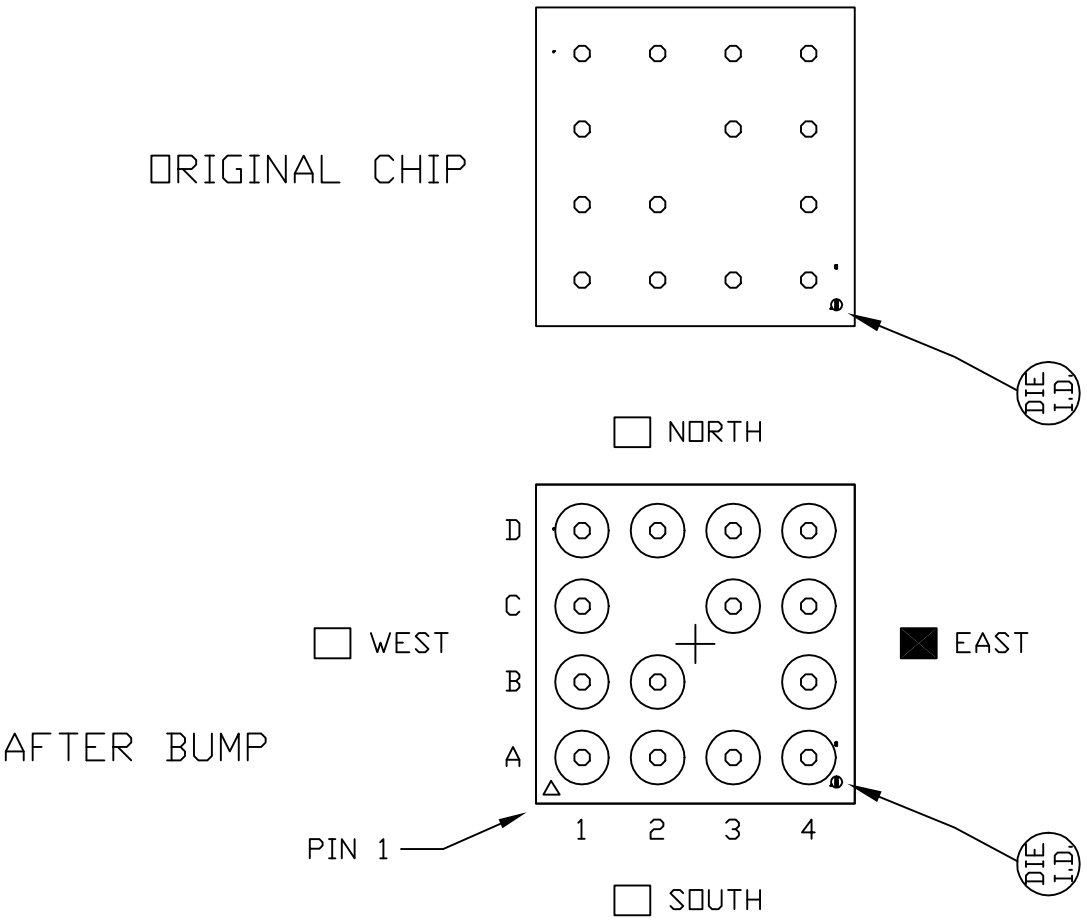
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



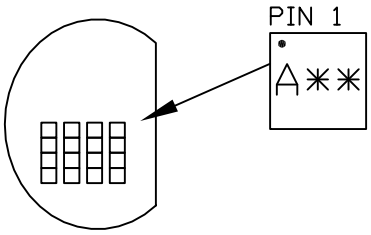
4x4x0.80mm QFN THIN PKG. EXPOSED PAD PKG.



PKG. CODE: T1644-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 98x98	PKG.			BOND DIAGRAM #: 05-9000-0658	REV: A
	DESIGN				

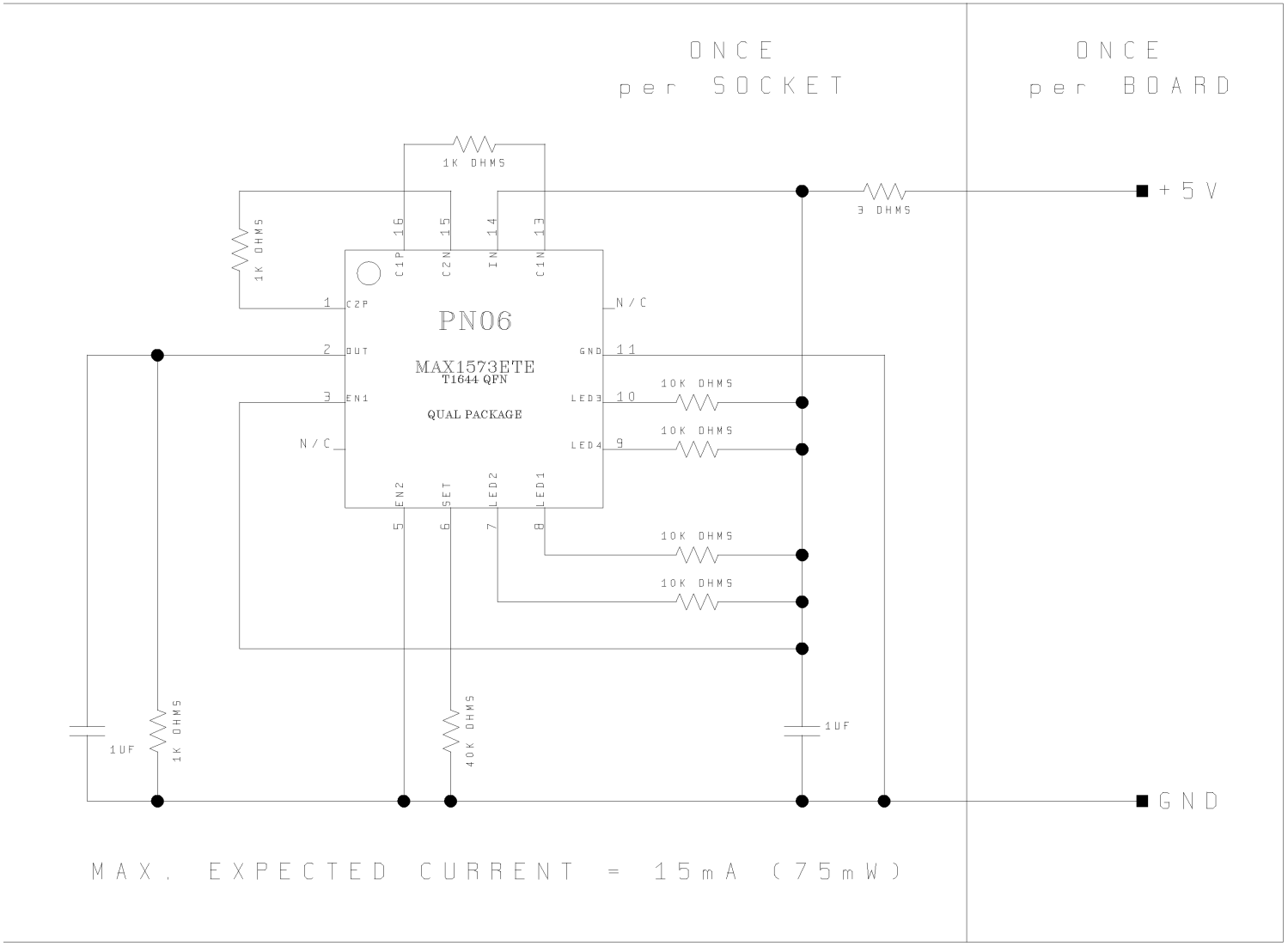


SELECT THE BOX INDICATING THE WAFER FLAT SIDE
WITH RESPECT TO PIN 1.



PART MARKING ORIENTATION
IN REFERENCE TO WAFER FLAT
(MARK IS ON WAFER BACKSIDE)

PKG. CODE: B16-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: N/A	PKG.			BOND DIAGRAM #: 05-9000-0484	REV: A
	DESIGN				



DOCUMENT I.D. 06-6187	REVISION B	*MAXIM* TITLE: **BI Circuit (MAX1573) PN06**	PAGE 2