MAX1582ETC
Rev. B

RELIABILITY REPORT

FOR

MAX1582ETC

PLASTIC ENCAPSULATED DEVICES

June 23, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by	Reviewed by
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Conclusion

The MAX1582 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1582 drives up to six white LEDs in series with a constant current to provide display backlighting for two (main and sub-) displays in cell phones and other hand-held devices. This configuration eliminates the need for ballast resistors and expensive factory calibration. The proprietary dual-output, step-up pulse-width modulation (PWM) converter includes a 30V, low RDSON N-channel MOSFET switch for high efficiency and maximum battery life.

The MAX1582 utilizes 1MHz current-mode PWM control to allow small input and output capacitors and a small inductor, while minimizing ripple on the input supply and avoiding interference to sensitive circuitry in the equipment. Integrated overvoltage protection eliminates the need for an external zener diode to protect the IC from open circuit. Flexible dimming control utilizes either an analog control signal or direct digital PWM control without external RC filtering. This also increases dimming accuracy at low brightness levels. The PWM dimming signal can be any frequency from 200Hz to 200kHz. Soft-start eliminates inrush current during startup.

The MAX1582 is available in tiny 4 x 4 chip-scale (UCSP™) and 12-pin thin QFN packages

B. Absolute Maximum Ratings

Item	Rating
V+, VP, CTRL to GND	-0.3V to +6.0V
PGND to GND	-0.3V to +0.3V
LX, OUT1 to GND	-0.3V to +30V
OUT2 to GND	-0.3V to +14V
COMP, CS, EN1, EN2 to GND	-0.3V to (VV+ + 0.3V)
ILX	1ARMS
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
12-Pin QFN	1349mW
16-Pin UCSP	518mW
Derates above +70°C	
12-Pin QFN	16.9mW/°C
16-Pin UCSP	6.5mW/°C

II. Manufacturing Information

A. Description/Function: High-Efficiency, 26V Step-Up Converter for White LED Main and Subdisplay Backlighting

B. Process: S8 - Standard 8 micron silicon gate CMOS

C. Number of Device Transistors: 2546

D. Fabrication Location: California, USA

E. Assembly Location: Thailand or Hong Kong

F. Date of Initial Production: March, 2003

III. Packaging Information

A. Package Type: **12-Lead QFN (4x4)**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: Buildsheet # 05-9000-0436

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity
per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 83 X 83 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: TiW/ AlCu/ TiWN

D. Backside Metallization: None

E. Minimum Metal Width: .8 microns (as drawn)

F. Minimum Metal Spacing: .8 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times \underset{\uparrow}{4389} \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.62 \times 10^{-9}$ $\lambda = 22.62$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-6144) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**) located on the Maxim website at http://www.maxim-ic.com .

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PM99 die type has been found to have all pins able to withstand a transient pulse of ±400V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1

Reliability Evaluation Test Results

MAX1582ETC

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

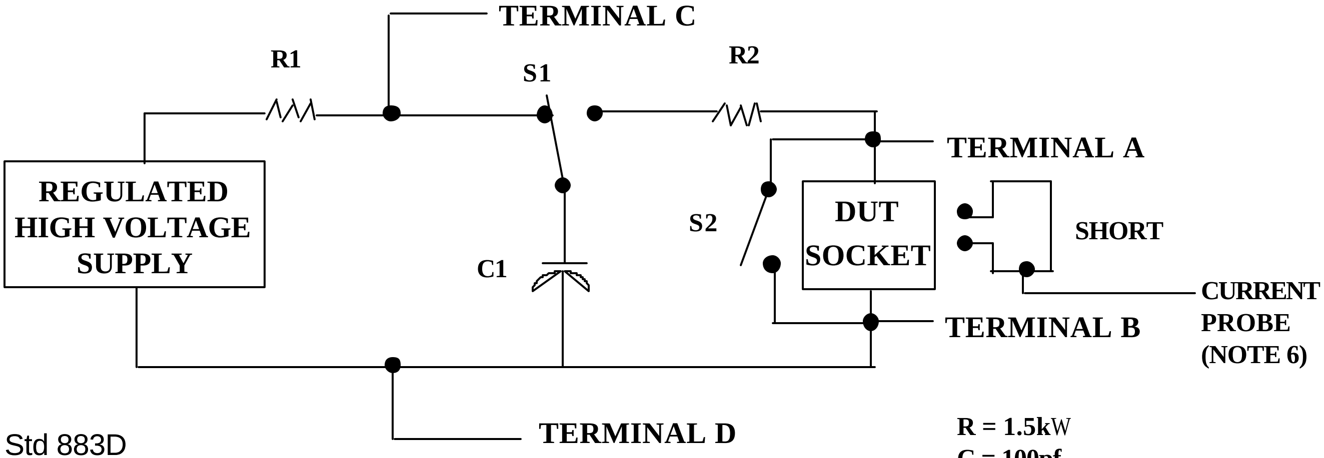
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

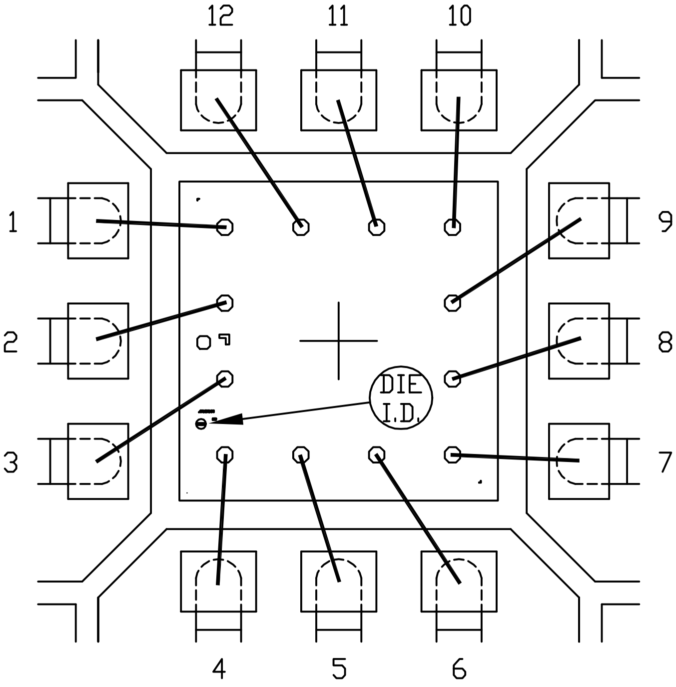
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



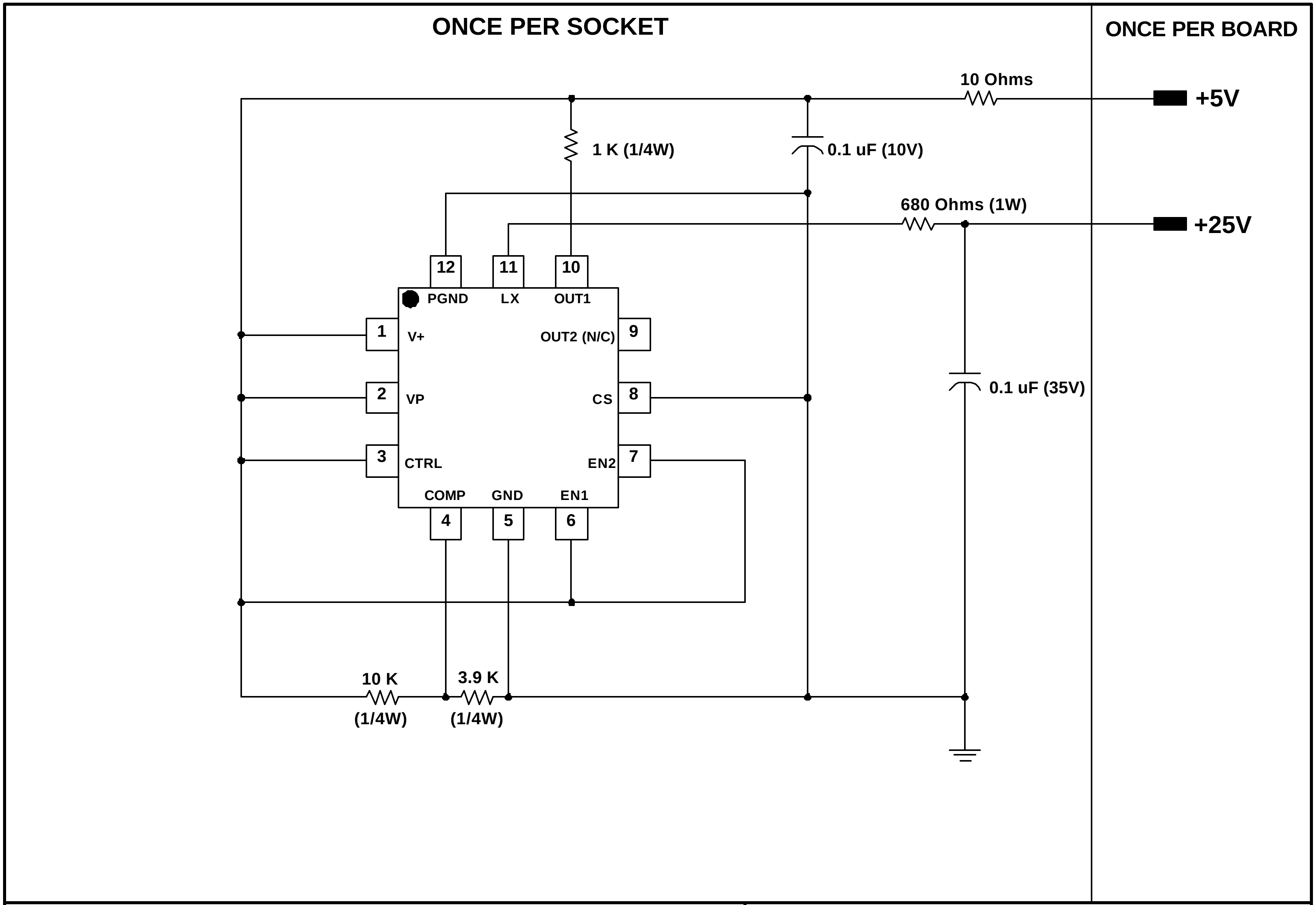
R = 1.5kW
C = 100pf

4x4x0.8 MM QFN THIN PKG.

EXPOSED PAD PKG.



PKG. CODE: T1244-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 98x98	PKG.			BOND DIAGRAM #: 05-9000-0436	REV: A
	DESIGN				



DEVICES: MAX 1582 (PM99)
PACKAGE: 12-QFN (4x4)
MAX. EXPECTED CURRENT = 5mA (+5V), 18mA (+25V).

DRAWN BY: TEK TAN
NOTES: