RELIABILITY REPORT

FOR

MAX16046CETN+T

PLASTIC ENCAPSULATED DEVICES

September 25, 2014

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX16046CETN+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX16046C EEPROM-configurable system managers monitor, sequence, track, and margin multiple system voltages. The device manages up to 12 system voltages simultaneously, and integrates an analog-to-digital converter (ADC) for monitoring supply voltages, digital-to analog converters (DAC) for adjusting supply voltages, and configurable outputs for sequencing and tracking supplies (during power-up and power-down). Nonvolatile EEPROM registers are configurable for storing upper and lower voltage limits, setting timing and sequencing requirements, and for storing critical fault data for readback following failures. An internal 1% accurate 10-bit ADC measures each input and compares the result to one upper, one lower, and one selectable upper or lower limit. A fault signal asserts when a monitored voltage falls outside the set limits. Up to three independent fault output signals are configurable to assert under various fault conditions. The integrated sequencer/tracker allows precise control over the power-up and power-down order of up to 12 power supplies. Four channels (EN_OUT1–EN_OUT4) support closed-loop tracking using external series MOSFETs. Six outputs (EN_OUT1–EN_OUT6) are configurable with charge-pump outputs to directly drive MOSFETs without closed-loop tracking. The device includes 12 integrated 8-bit DAC outputs for margining power supplies when connected to the trim input of a point-of-load (POL) module. The device includes six programmable general-purpose inputs/outputs (GPIOs). GPIOs are EEPROM configurable as dedicated fault outputs, as a watchdog input or output (WDI/WDO), as a manual reset (MR), or as margin control inputs. The device features two methods of fault management for recording information during system shutdown events. The fault logger records a failure in the internal EEPROM and sets a lock bit protecting the stored fault data from accidental erasure. An I^2C or a JTAG serial interface configures the MAX16046C, which is offered in a 56-pin 8mm x 8mm TQFN package and is fully specified from -40°C to +85°C.

II. Manufacturing Information

A. Description/Function:	12-/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers
B. Process:	EB8
C. Number of Device Transistors:	153726
D. Fabrication Location:	USA
E. Assembly Location:	USA, Taiwan, China, Thailand
F. Date of Initial Production:	September 17, 2014

III. Packaging Information

A. Package Type:	56-pin TQFN 8x8
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2780
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	35°C/W
K. Single Layer Theta Jc:	1°C/W
L. Multi Layer Theta Ja:	21°C/W
M. Multi Layer Theta Jc:	1°C/W

IV. Die Information

A. Dimensions:	258 X 235 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	3.0 microns (as drawn)
F. Minimum Metal Spacing:	3.0 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 48 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 22.9 \times 10^{-9}$

$\lambda = 22.9$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the EB8 Process results in a FIT Rate of 0.09 @ 25°C and 1.58 @ 55°C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot TATU5A080G, D/C 1423)

The MT07-1 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/-2500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 100mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX16046CETN+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	TATU5A080F, D/C 1423

Note 1: Life Test Data may represent plastic DIP qualification lots.