

RELIABILITY REPORT
FOR
MAX1623EAP
PLASTIC ENCAPSULATED DEVICES

December 16, 2002

MAXIM INTEGRATED PRODUCTS

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SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX1623 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1623 switch-mode buck regulator with synchronous rectification provides local CPU and bus-termination power in notebook and desktop computers. An internal 55m(typ), 3A PMOS power switch and 60m(typ), 3A NMOS synchronous-rectifier switch deliver continuous load currents up to 3A from a 5V supply with 95% typical efficiency. Output accuracy is $\pm 1\%$, including line and load regulation. The MAX1623 features constant-off-time, current-mode pulse-width-modulation (PWM) control with switching frequencies as high as 350kHz. An external resistor at the TOFF pin sets the off-time, allowing optimum design flexibility in terms of switching frequency, output switching noise, and inductor size. This device is available in a space-saving 20-pin SSOP package.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
IN to PGND	0V to 6V
V _{CC} to GND	-0.3V to 6V
PGND to GND	$\pm 0.5V$
IN to V _{CC}	$\pm 0.5V$
LX Current (Note 1)	$\pm 5.5A$
/SHDN to GND	-0.3V to 6V
REF, FBSEL, COMP, FB, TOFF to GND	0.3V to (V _{CC} + 0.3V)
REF Short to GND	Continuous
Continuous Power Dissipation (TA = +70°C) (with part mounted on 1 sq. inch of one ounce copper)	
20-Pin SSOP	1.3W
Derates above +70°C	
20-Pin SSOP	22mW/°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Note 1: LX has internal clamp diodes to PGND and IN. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

II. Manufacturing Information

- A. Description/Function: 3A, Low-Voltage, Step-Down Regulator with Synchronous Rectification and Internal Switches
- B. Process: S12 (Standard 1.2 micron silicon gate CMOS)
- C. Number of Device Transistors: 1220
- D. Fabrication Location: Oregon, USA
- E. Assembly Location: Philippines, Thailand or Malaysia
- F. Date of Initial Production: April, 1999

III. Packaging Information

- A. Package Type: **20-Pin SSOP**
- B. Lead Frame: Copper
- C. Lead Finish: Solder Plate
- D. Die Attach: Silver-filled Epoxy
- E. Bondwire: Gold (2 mil dia.)
- F. Mold Material: Epoxy with silica filler
- G. Assembly Diagram: # 05-1701-0346
- H. Flammability Rating: Class UL94-V0
- I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

- A. Dimensions: 100 x 179 mils
- B. Passivation: $\text{Si}_3\text{N}_4/\text{SiO}_2$ (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 1.2 microns (as drawn)
- F. Minimum Metal Spacing: 1.2 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric: SiO_2
- I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 160 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

▲
Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 6.79 \times 10^{-9}$$

$$\lambda = 6.79 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5184) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PW74X die type has been found to have all pins able to withstand a transient pulse of $\pm 1000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$ and/or $\pm 20\text{V}$.

Table 1
Reliability Evaluation Test Results

MAX1623EAP

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	SSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.

Note 2: Generic Package/Process data

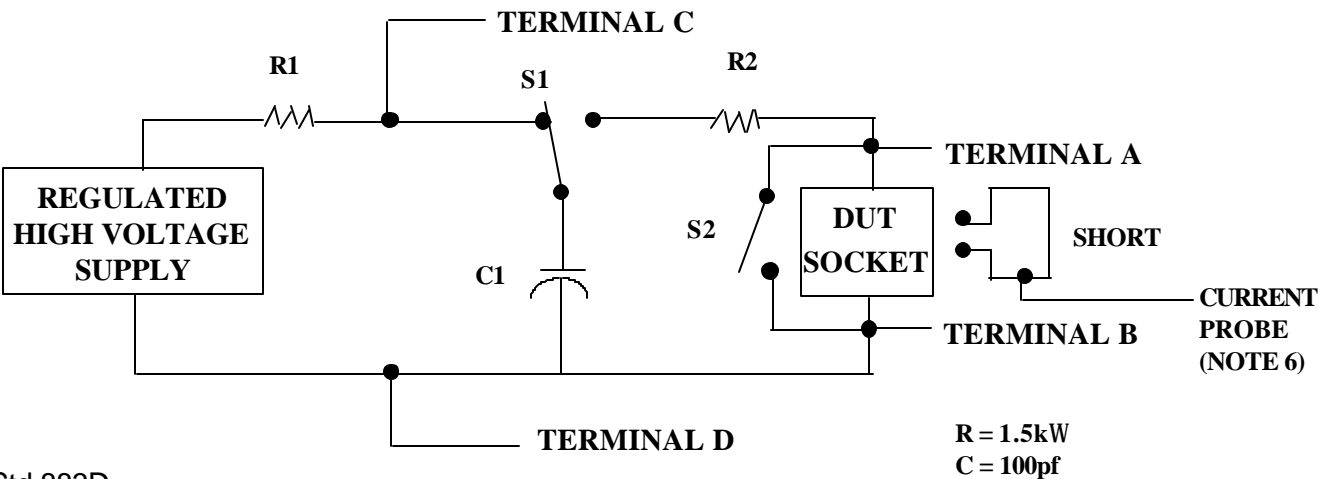
TABLE II. Pin combination to be tested. 1/ 2/

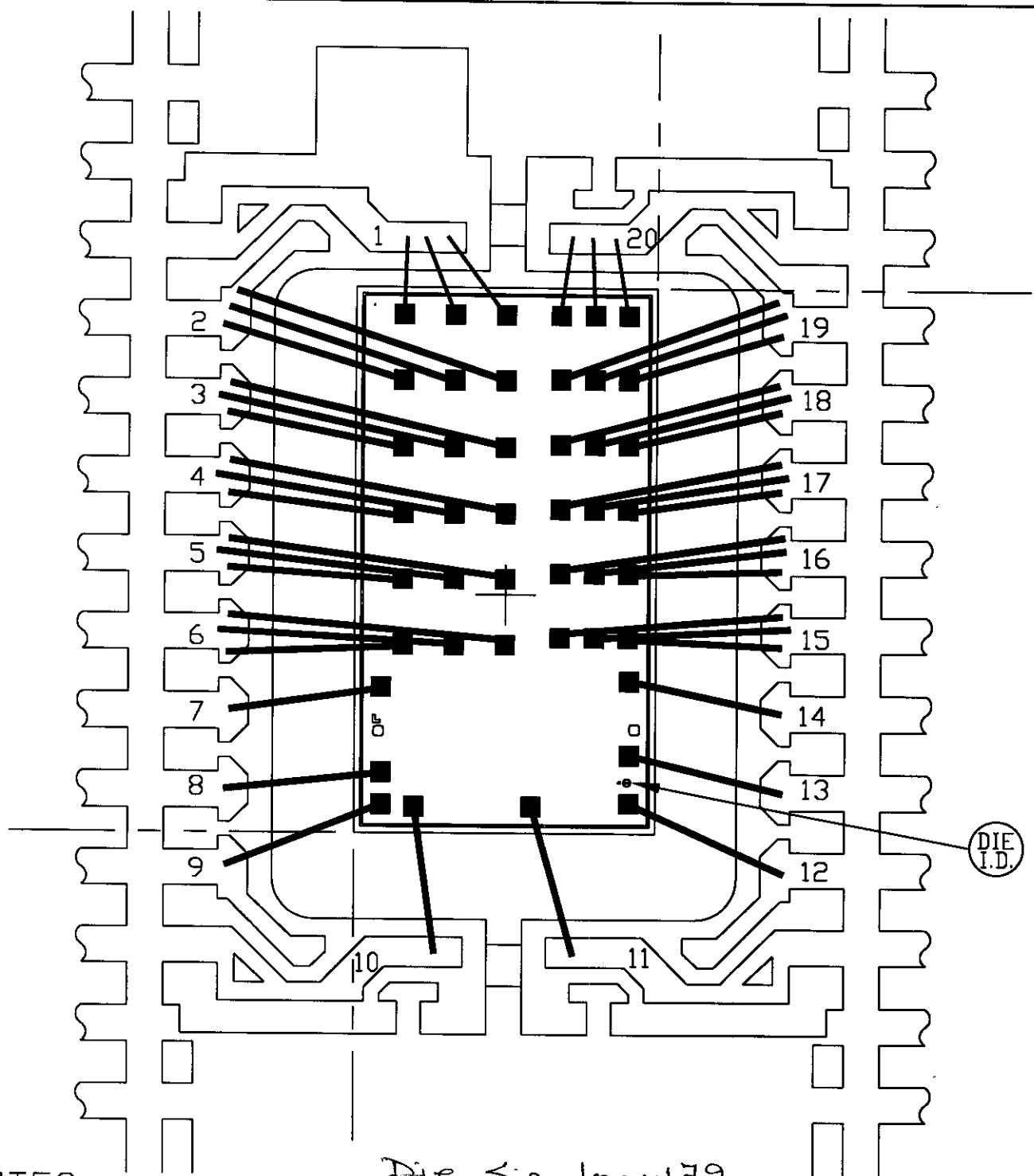
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





NOTES:

Die Size 100x179.

1. Needs 2 mil gold wire.
2. Use J loop bonding on in-board bond pins
or
use cross bonding to support long wires
with short wires.

PKG.CODE: A20-2		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 154X213	PKG. DESIGN			BUILDSHEET NUMBER: 05-1701-0346	REV.: A

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-- STEADY STATE LINE TEST IS PER MIL-STO-003 METHOD 1005
-- BURN-IN IS PER MIL-STO-003 METHOD 1015. COND. B

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SPEC. NO.: 06-5184 REV.: A

MAX IN BURN-IN SCHEMATIC

1. TEMPERATURE: 1250 OR EQUIVALENT
 2. TIME: 150 HOURS MIN. OR EQUIVALENT
 3. ALL COMPONENTS AND MATERIAL MUST STAND 15000 CONTINUOUS
 4. APPROVED FOR EXO COMMERCIAL.
- EXI HR/883

DATE: 3/04/98

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03/24/2014

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