MAX1655ExE Rev. A

RELIABILITY REPORT

FOR

MAX1655ExE

PLASTIC ENCAPSULATED DEVICES

May 6, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX1655 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1655 is a high-efficiency, pulse-width-modulated (PWM), step-down DC-DC controller in a small QSOP packages and also comes in a 16-pin narrow S) package that is pin-compatible to the popular MAX797. Improvements include higher duty-cycle operation for better dropout, lower quiescent supply currents for better light-load efficiency, and an output voltage down to 1V.

The MAX1655 achieves up to 96% efficiency and deliver up to 10A using a unique Idle Mode[™] synchronous-rectified PWM control scheme. These devices automatically switch between PWM operation at heavy loads and pulse-frequency-modulated (PFM) operation at light loads to optimize efficiency over the entire output current range. The MAX1655 also features logic-controlled, forced PWM operation for noise-sensitive applications.

The device operates with a selectable 150kHz/300kHz switching frequency, which can also be synchronized to an external clock signal. Both external power switches are inexpensive N-channel MOSFETs, which provide low resistance while saving space and reducing cost.

The MAX1655 has a 4.5V to 30V input voltage range. The MAX1655's output range is 1V to 5.5V.

B. Absolute Maximum Ratings

<u>ltem</u>	Rating
V+ to GND	-0.3V to +36V
GND to PGND	-0.3V to +0.3V
VL to GND	-0.3V to +6V
BST to GND	-0.3V to +36V
DH to LX	-0.3V to (BST + 0.3V)
LX to BST	-6V to + 0.3V
/SHDN to GND	-0.3V to (V+ + 0.3V)
SYNC, SS, REF, SECFB, /SKIP, FB to GND	-0.3V to (VL + 0.3V)
DL to PGND	-0.3V to (VL + 0.3V)
CSH, CSL to GND	-0.3V to +6V
VL Short Circuit to GND	Momentary
REF Short Circuit to GND	Continuous
VL Output Current	+50mA to -1mA
REF Output Current	+5mA to -1mA
Operating Temp.	-40°C to +85°C
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation	
16-Pin QSOP	667mW
16-Pin NSO	696mW
Derates above +70°C	
16-Pin NSO	8.3mW/°C
16-Pin NSO	8.7mW/°C

II. Manufacturing Information

A. Description/Function:	High-Efficiency, PWM, Stept-Down DC-DC Controller
B. Process:	S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	1990
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia, Philippines, Korea or Thailand
F. Date of Initial Production:	April, 1998

III. Packaging Information

A. Package Type:	16-Lead QSOP	16-Lead NSO
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1701-0312	Buildsheet # 05-1701-0311
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	107 x 80 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

Α.	Quality Assurance Contacts:	Jim Pedicord (Reliability Lab Manager)
		Bryan Preeshl (Executive Director of QA)
		Kenneth Huening (Vice President)

- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \frac{1}{\text{MTTF}} = \frac{4.04}{192 \times 4389 \times 80 \times 2}$ (Chi square value for MTTF upper limit) Temperature Acceleration factor assuming an activation energy of 0.8eV $\lambda = 29.97 \times 10^{-9}$ $\lambda = 29.97 \text{ F.I.T.}$ (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5048) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PW86-3 die type has been found to have all pins able to withstand a transient pulse of \pm 400, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of \pm 250mA and/or \pm 20V.

Table 1 Reliability Evaluation Test Results

MAX1655ExE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION		SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test	(Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	1
Moisture Testin	ig (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP NSO	700 340	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stre	ess (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

Attachment #1

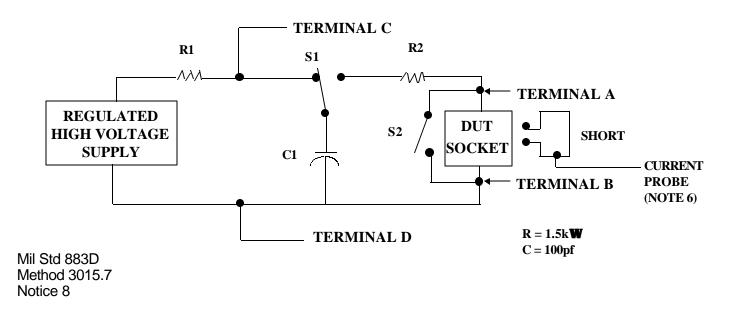
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} <u>3/</u>	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

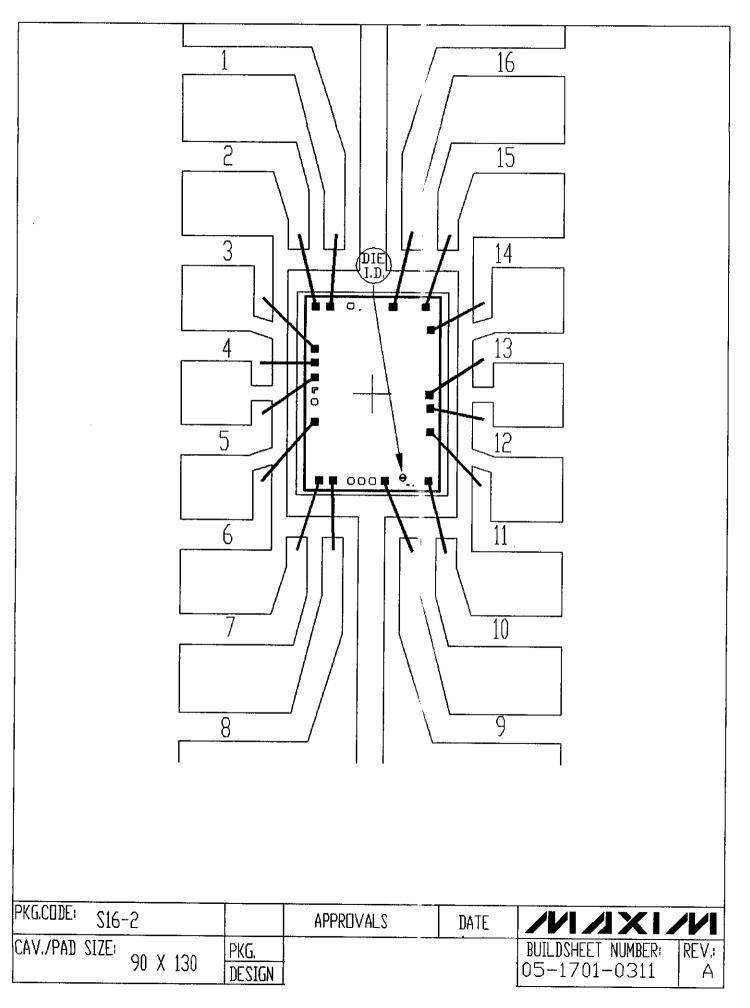
TABLE II. Pin combination to be tested. 1/2/

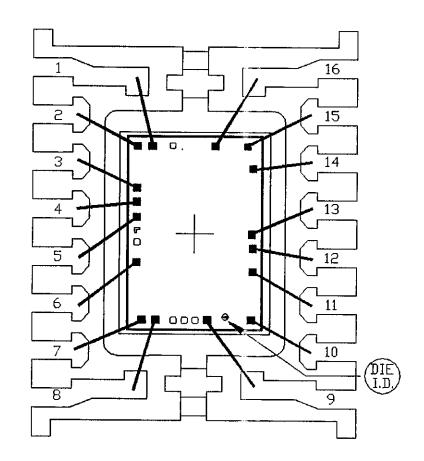
- 1/ Table II is restated in narrative form in 3.4 below.
- $\overline{2/}$ No connects are not to be tested.
- $\overline{3/}$ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, + V_{S} , - V_{S} , V_{REF} , etc).

- 3.4 <u>Pin combinations to be tested.</u>
 - a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
 - b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
 - c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.







PKG.CODE: E16-1		APPROVALS	DATE	MAXI	11
CAV./PAD SIZE:	PKG.			BUILDSHEET NUMBER:	REV.
<u>96X130</u>	DESIGN			05-1701-0312	A

