RELIABILITY REPORT

FOR

MAX1664EUP+T

PLASTIC ENCAPSULATED DEVICES

February 15, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX1664EUP+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1664 integrates power-supply and backplane drive circuitry for active-matrix thin-film-transistor (TFT) liquid crystal displays. Included are a single-output, pulse-width-modulation boost converter (0.25 switch), a dual-output (positive and negative) gate-driver supply using one inductor, an LCD backplane driver, and a simple phase-locked loop to synchronize all three outputs. High switching frequency (1MHz nominal) and phase-locked operation allow the use of small, minimum-height external components while maintaining low output noise. A +2.8V to +5.5V input voltage range allows operation with any logic supply. Output voltages are adjustable to +5.5V (DC-DC 1) and to +28V and-10V (DC-DC 2). The negative output voltage can be adjusted to -20V with additional components. Also included are a logic-level shutdown and a "Ready" output (RDY) that signals when all three outputs are in regulation. The boost-converter operating frequency can be set at 16, 24, or 32 times the backplane clock. This flexibility allows a high DC-DC converter frequency to be used with LCD backplane clock rates ranging from 20kHz to 72kHz. The MAX1664 is supplied in a 1.1mm-high TSSOP package.

II. Manufacturing Information

A. Description/Function:	Active Matrix Liquid Crystal Display (AMLCD) Supply
B. Process:	S12
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon, California or Texas
E. Assembly Location:	Philippines, Thailand, Malaysia
F. Date of Initial Production:	July 24, 1998

III. Packaging Information

A. Package Type:	20-pin TSSOP
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-1101-0067
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	91°C/W
K. Single Layer Theta Jc:	20°C/W
L. Multi Layer Theta Ja:	73.8°C/W
M. Multi Layer Theta Jc:	20°C/W

IV. Die Information

A. Dimensions:	84 X 141 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135¿C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S12 Process results in a FIT Rate of 0.17 @ 25C and 3.00 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot NL4ACQ001B D/C 9813)

The PX22 die type has been found to have all pins able to withstand a HBM transient pulse of +/-800V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX1664EUP+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	NL4ACX001F, D/C 9821

Note 1: Life Test Data may represent plastic DIP qualification lots.