RELIABILITY REPORT

FOR

MAX17017GTM+

PLASTIC ENCAPSULATED DEVICES

August 7, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Ken Wendel
Quality Assurance
Director, Reliability Engineering

Conclusion

The MAX17017GTM+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX17017 is a quad output controller for ultra-mobile portable computers (UMPCs) that rely on a low-power architecture. The MAX17017 provides a compact, low-cost controller capable of providing four independent regulatorsâ€"a main stage, a 3AP-P internal step-down, a 5AP-P internal step-down, and a 2A source/sink linear regulator. The main regulator can be configured as either a step-down converter (for 2 to 4 Li+ cell applications) or as a step-up converter (for 1 Li+ cell applications). The internal switching regulators include 5V synchronous MOSFETs that can be powered directly from a single Li+ cell or from the main 3.3V/5V power stages. Finally, the linear regulator is capable of sourcing and sinking 2A to support DDR termination requirements or to generate a fixed-output voltage. The step-down converters use a peak current-mode, fixed-frequency control schemeâ€"an easy to implement architecture that does not sacrifice fast-transient response. This architecture also supports peak current-limit protection and pulse-skipping operation to maintain high efficiency under light-load conditions. Separate enable inputs and independent open-drain power-good outputs allow flexible power sequencing. A soft-start function gradually ramps up the output voltage to reduce the inrush current. Disabled regulators enter high-impedance states to avoid negative output voltage created by rapidly discharging the output through the low-side MOSFET. The MAX17017 also includes output undervoltage, output overvoltage, and thermal-fault protection. The MAX17017 is available in a 48-pin, 6mm x 6mm Thin QFN package.

II. Manufacturing Information

A. Description/Function:	Quad Output Controller for Low-Power Architecture
B. Process:	S45
C. Number of Device Transistors:	
D. Fabrication Location:	California, Texas or Japan
E. Assembly Location:	Thailand
F. Date of Initial Production:	7/25/2008

III. Packaging Information

A. Package Type:	48-pin TQFN 6x6
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (2 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2804
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	38°C/W
K. Single Layer Theta Jc:	1.4°C/W
L. Multi Layer Theta Ja:	27°C/W
M. Multi Layer Theta Jc:	1.4°C/W

IV. Die Information

A. Dimensions:	115 X 150 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{AfT \times DevHrs \times 2}$$ (Chi square value for MTTF upper limit for zero failures)

Where:
AfT = 4445 = Temperature Acceleration factor assuming an activation energy of 0.8eV)
DevHrs = 38317 (@135°C)

$\lambda = 0.54 \times 10^{-9}$

$\lambda = 0.54$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the S45 Process results in a FIT Rate of 0.09 @ 25C and 1.16 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The PE30 die type has been found to have all pins able to withstand a HBM transient pulse of +/-3000 V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX17017GTM+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = Mixed hrs	DC Parameters & functionality	516	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data