MAX1708EEE Rev. A

RELIABILITY REPORT

FOR

MAX1708EEE

PLASTIC ENCAPSULATED DEVICES

July 7, 2006

MAXIM INTEGRATED PRODUCTS

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Written by

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Conclusion

The MAX1708 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1708 sets a new standard of space savings for high-power, step-up DC-DC conversion. It delivers up to 10W at a fixed (3.3V or 5V) or adjustable (2.5V to 5.5V) output, using an on-chip power MOSFET from a +0.7V to +5V supply.

Fixed-frequency PWM operation ensures that the switching noise spectrum is constrained to the 600kHz fundamental and its harmonics, allowing easy postfiltering for noise reduction. External clock synchronization capability allows for even tighter noise spectrum control. Quiescent power consumption is less than 1mW to extend operating time in battery-powered systems.

Two control inputs (ONA, ONB-bar) allow simple push-on, push-off control through a single momentary pushbutton switch, as well as conventional on/off logic control. The MAX1708 also features programmable soft-start and current limit for design flexibility and optimum performance with batteries. The maximum RMS switch current rating is 5A. For a device with a higher (10A) switch current rating, refer to the MAX1709 data sheet.

B. Absolute Maximum Ratings	Rating
ONA, ONB, OUT, SS/LIM, 3.3/5 to GND LX to PGND FB, CLK, REF to GND PGND to GND	-0.3V to +6.0V -0.3V to +6.0V -0.3V to (VOUT + 0.3V) -0.3V to +0.3V
Continuous Power Dissipation (TA = +70°C) 16-Pin QSOP (derate 8.30mW/°C above +70°C) Operating Temperature Range Junction Temperature Storage Temperature Range Lead Temperature (soldering, 10s)	667mW -40°C to +85°C +150°C -65°C to +150°C +300°C

II. Manufacturing Information

A. Description/Function: High-Frequency, High-Power, Low-Noise, Step-Up DC-DC Converter

B. Process:	B12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	1,112
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia, Philippines or Thailand
F. Date of Initial Production:	July, 2001
III. Packaging Information	

A. Package Type:	16 QSOP
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate or 100% Matte Tin
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	# 05-1101-0096
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C:	Level 1

IV. Die Information

A. Dimensions:	86 x 120 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

- A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations) Bryan Preeshl (Managing Director of QA)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 130 \times 2}$ (Chi square value for MTTF upper limit) Temperature Acceleration factor assuming an activation energy of 0.8eV

 $\lambda = 8.46 \times 10^{-9}$

 $\lambda = 8.46$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Attached Burn-In Schematic (Spec. # 06-5330) shows the static Burn-In circuit. Maxim performs failure analysis on any lot that exceeds this reliability control level. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1N**). Current monitor data for the B8/S8 Process results in a FIT rate of 0.10 @ 25° C and 1.78 @ 55° C (eV = 0.8, UCL = 60%).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PX34 die type has been found to have all pins able to withstand a transient pulse of ± 2500 V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ± 250 mA.

Table 1 Reliability Evaluation Test Results

MAX1708EEE

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Tes	t (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		130	0
Moisture Testi	ng (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	16 QSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical St	ress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots. Note 2: Generic Package/Process data

Attachment #1

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V _{PS1} 3/	All V _{PS1} pins
2.	All input and output pins	All other input-output pins

TABLE II. Pin combination to be tested. 1/2/

- 1/ Table II is restated in narrative form in 3.4 below.
- $\frac{32}{2}$ No connects are not to be tested. $\frac{32}{2}$ Repeat pin combination I for each named Power supply and for ground

(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{RFF} , etc).

3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected a. to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination b. of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of C. all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





