RELIABILITY REPORT

FOR

MAX1718EEI

PLASTIC ENCAPSULATED DEVICES

April 20, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX1718 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1718 step-down controller is intended for core CPU DC-DC converters in notebook computers. It features a dynamically adjustable output, ultra-fast transient response, high DC accuracy, and high efficiency needed for leading-edge CPU core power supplies. Maxim's proprietary Quick-PWM™ quick-response, constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides 100ns "instant-on" response to load transients while maintaining a relatively constant switching frequency.

The output voltage can be dynamically adjusted through the 5-bit digital-to-analog converter (DAC) over a 0.6V to 1.75V range. The MAX1718 has an internal multiplexer that accepts three unique 5-bit VID DAC codes corresponding to Performance, Battery, and Suspend modes. Precision slew-rate control† provides "just-in-time" arrival at the new DAC setting, minimizing surge currents to and from the battery.

The internal DAC of the MAX1718B is synchronized to the slew-rate clock for improved operation under aggressive power management of newer chipsets and operating systems that can make incomplete mode transitions.

A pair of complementary offset control inputs allows easy compensation for IR drops in PC board traces or creation of a voltage-positioned power supply. Voltage-positioning modifies the load-transient response to reduce output capacitor requirements and total system power dissipation.

Single-stage buck conversion allows these devices to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, two-stage conversion (stepping down the 5V system supply instead of the battery) at a higher switching frequency allows the minimum possible physical size.

The MAX1718 is available in a 28-pin QSOP package.

B. Absolute Maximum Ratings (Note 1)

Item	Rating
V+ to GND	-0.3V to +30V
VCC, VDD to GND	-0.3V to +6V
D0–D4, ZMODE, VGATE, OVP, SUS, to GND	-0.3V to +6V
SKP/SDN to GND	-0.3V to +16V
ILIM, CC, REF, POS, NEG, S1, S0, TON, TIME to GND	-0.3V to (VCC + 0.3V)
DL to GND	-0.3V to (VDD + 0.3V)
BST to GND	-0.3V to +36V
DH to LX	-0.3V to (BST + 0.3V)
LX to BST	-6V to +0.3V
REF Short Circuit to GND	Continuous
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
28-Pin QSOP	860mW
Derates above +70°C	
28-Pin QSOP	10.8W/°C

II. Manufacturing Information

A. Description/Function: Notebook CPU Step-Down Controller for Intel Mobile Voltage Positioning (IMVP-II)

B. Process: S12 (Standard 1.2 micron silicon gate CMOS)

C. Number of Device Transistors: 7190

D. Fabrication Location: Oregon or California, USA

E. Assembly Location: Malaysia, Thailand or Philippines

F. Date of Initial Production: January, 2001

III. Packaging Information

A. Package Type: **28-Pin QSOP**

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: # 05- 2301-0015

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: Level 1

IV. Die Information

A. Dimensions: 83 x 141 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°Cbiased (static) life test are shown in **Table 1** Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 155 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 6.21 \times 10^{-9}$

$\lambda = 6.21$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5667) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The PY03-1 die type has been found to have all pins able to withstand a transient pulse of ±400V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±200mA.

Table 1
Reliability Evaluation Test Results

MAX1718EEI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		155	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

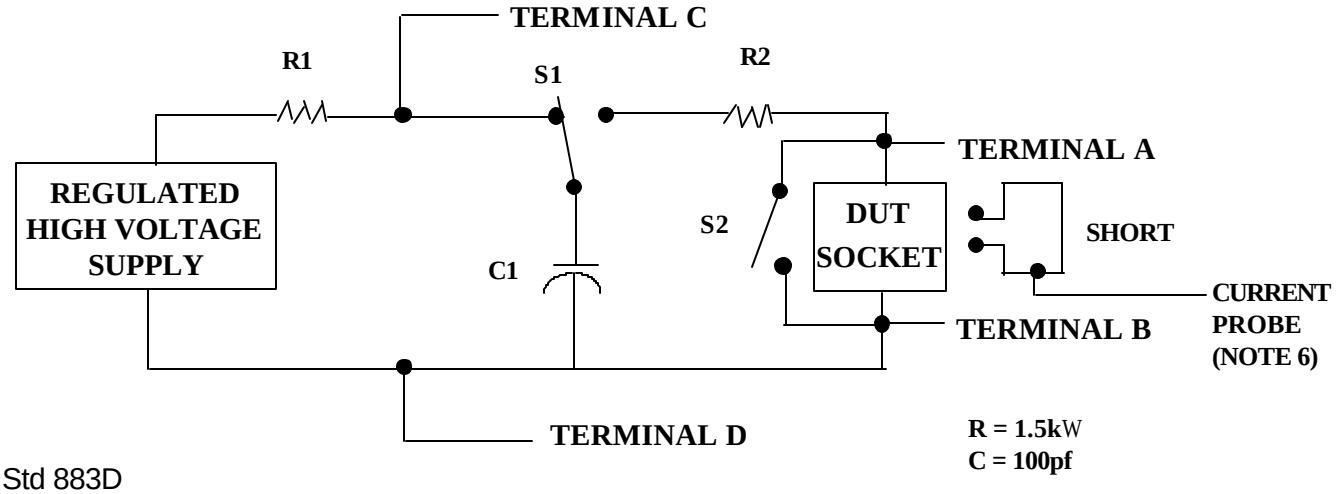
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

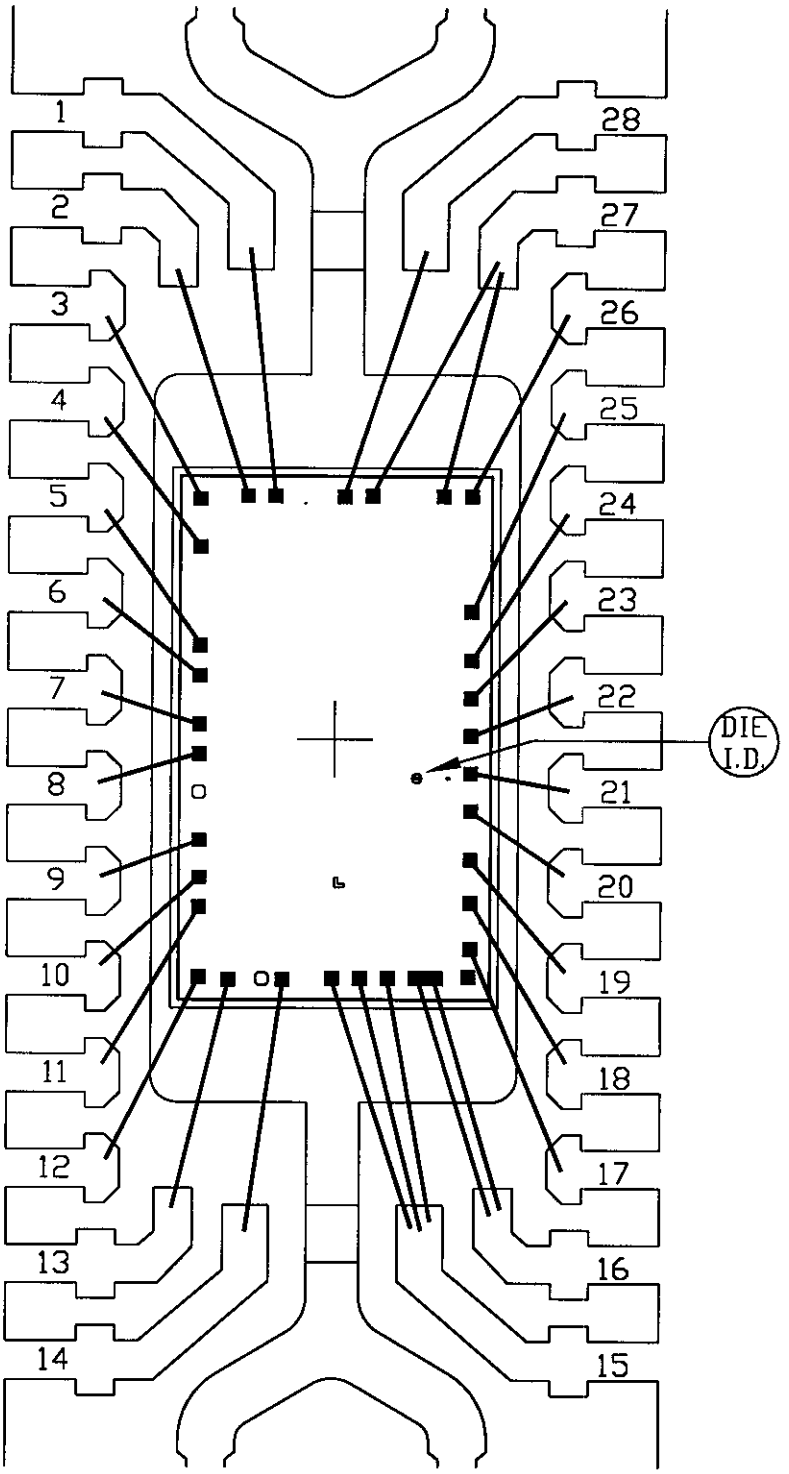
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

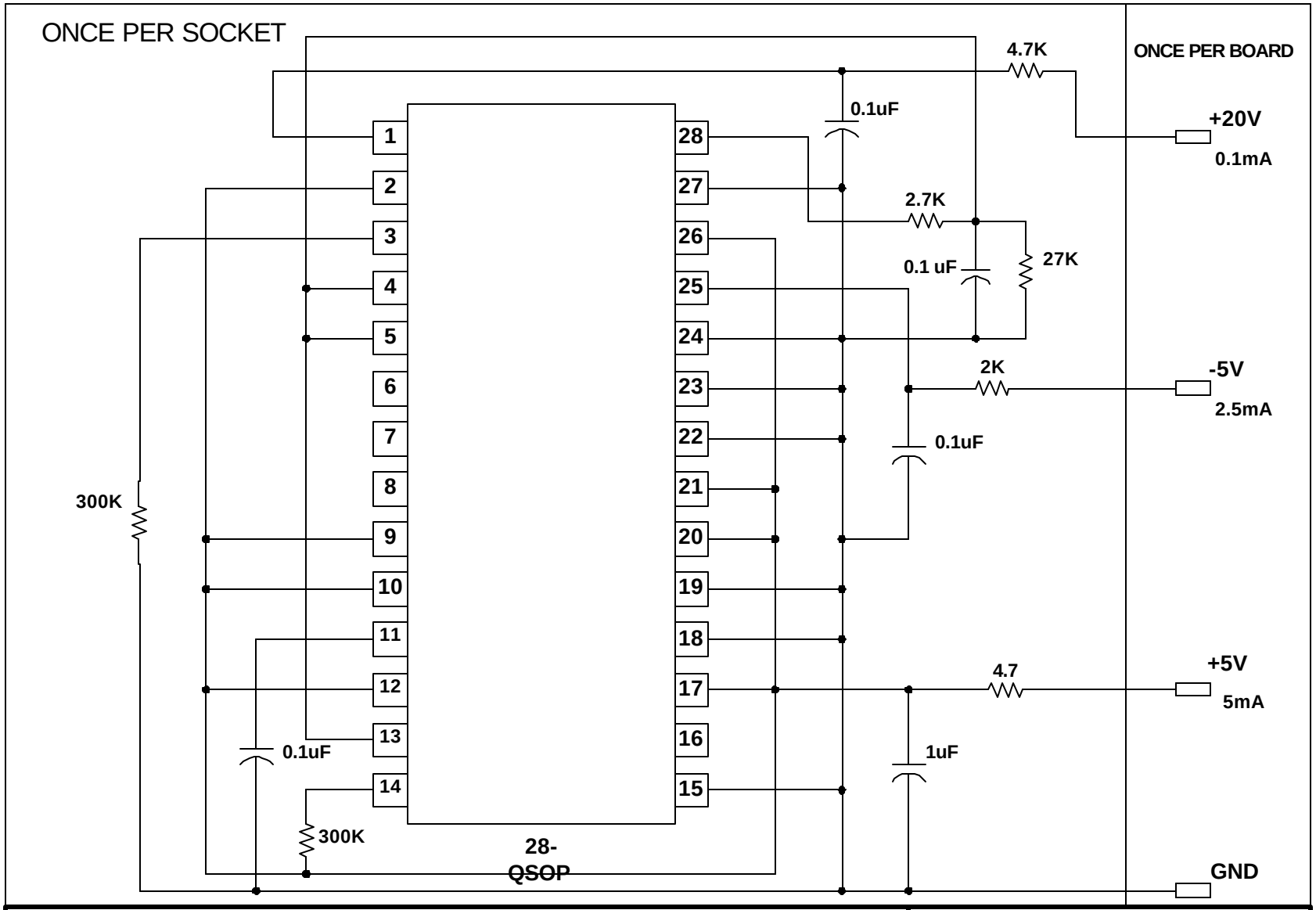
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



PKG. CODE: E28-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 96X190	PKG. DESIGN			BOND DIAGRAM #: 05-2301-0015 / REV: B



DEVICES: MAX 1718

MAX. EXPECTED CURRENT = 0.1mA (+20V) 2.5mA (-5V) 5mA (+5V)

DRAWN BY: HAK TAN

NOTES