RELIABILITY REPORT

FOR

MAX17222ENT+T

WAFER LEVEL DEVICES

June 4, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

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Conclusion

The MAX17222ENT+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX17220-MAX17225 is a family of ultra-low quiescent current boost (step-up) DC-DC converters with a 225mA/0.5A/1A peak inductor current limit and True Shutdown™. True Shutdown disconnects the output from the input with no forward or reverse current. The output voltage is selectable using a single standard 1% resistor. The 225mA (MAX17220), 500mA (MAX17222/MAX17223), and 1A (MAX17224/MAX17225) peak inductor current limits allow flexibility when choosing inductors. The MAX17220/MAX17222/MAX17224 versions have post-startup enable transient protection (ETP), allowing the output to remain regulated for input voltages down to 400mV, depending on load current. The MAX17220-MAX17225 offer ultra-low quiescent current, small total solution size, and high efficiency throughout the entire load range. The MAX17220-MAX17225 are ideal for battery applications where long battery life is a must.

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II. Manufacturing Information

A. Description/Function:	400mV to 5.5V Input, nanoPower Synchronous Boost Converter with True Shutdown
B. Process:	S18
C. Number of Device Transistors:	10551
D. Fabrication Location:	USA
E. Assembly Location:	Taiwan
F. Date of Initial Production:	January 6, 2017

III. Packaging Information

A. Package Type:	6-bump thin WLP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	None
G. Assembly Diagram:	#05-100494
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	95.15°C/W
M. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Dimensions:	57.0866X36.2205 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Eric Wright (Reliability Engineering)
Brian Standley (Manager, Reliability)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% for all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 79 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.9 \times 10^{-9}$

λ = 13.9 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The CP03-4 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX17222ENT+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	79	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.

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