RELIABILITY REPORT

FOR

MAX174ACWI+

PLASTIC ENCAPSULATED DEVICES

February 7, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
Sokhom Chum
Quality Assurance
Reliability Engineer

Conclusion

The MAX174AEWI+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX174 and the MX574A!MX674A are complete 12-bit a 'lalog-to-dlgital CO'lverters (ADCs) that combine high speed, low-power consumption, and on-chip ClOCK and voltage reference, The maximum conversior, times are 81ls (MAX174), 151ls (MX674A) and 25118 (MX574A) Maxim's SiCMOS construction reduces power dissipation 3 flrles (150mW) over corrparable devices The internal buried zener reference provides low-drift and low-noise performance, External component requirerrents are limited to only decoupling capacitors and fixed resistors. The versatile analog input structure allows for OV to + 1 OV or OV to +20V unipolar or ±5V or ±1 OV bipolar input ranges with pin strapping.

The MAX174/MX574A/MX674A use standard microprocessor -merface architectures and can be interfaced to 8-, 12- and 16-bit wide buses. Three-state data outouts are controlled by CS, CE and RIC logic inputs.

II. Manufacturing Information

A. Description/Function:	Industry-Standard, 12-Bit ADC with Reference
B. Process:	SG5
C. Number of Device Transistors:	
D. F abrication Location:	Oregon
E. Assembly Location:	Malaysia, Philippines
F. Date of Initial Production:	Pre 1997

III. Packaging Information

A. Package Type:	28-pin SOIC (W)
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-0101-0215
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	80°C/W
K. Single Layer Theta Jc:	18°C/W
L. Multi Layer Theta Ja:	59°C/W
M. Multi Layer Theta Jc:	18°C/W

IV. Die Information

A. Dimensions:	144 X 163 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	5.0 microns (as drawn)
F. Minimum Metal Spacing:	5.0 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. S ampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 320 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 3.4 \times 10^{-9}$

λ = 3.4 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the SG5 Process results in a FIT Rate of 0.12 @ 25C and 2.04 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (ESD lot NTCCSA006C D/C 9932, Latch-up lot NTCCC3050A D/C 0317)

The AD55-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX174AEWI+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	80	0	NTCAT3011C, D/C 9950
	Biased	& functionality	80	0	NTCBSA004B, D/C 9913
	Time = 192 hrs.		80	0	XTCCJQ001Q, D/C 9136
			80	0	XTCBJQ001Q, D/C 9130

Note 1: Life Test Data may represent plastic DIP qualification lots.