RELIABILITY REPORT

FOR MAX17651AZT+T

PLASTIC ENCAPSULATED DEVICES

February 28, 2017

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

 Eric Wright Reliability Engineer	 Brian Standley Manager, Reliability

Conclusion

The MAX17651AZT+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX17651 ultra-low quiescent current, high-voltage linear regulator is ideal for use in industrial and battery-operated systems. The device operates from a 4V to 60V input voltage, delivers up to 100mA of load current, and consumes only 8µA of quiescent current at no load. The device consumes only 0.9µA current when in shutdown. Output voltage is adjustable in the 0.6V to 59V voltage range. Feedback voltage accuracy is ±2% over temperature.

An open-drain, active-low PGOOD pin provides a power-good signal to the system upon achieving successful regulation of the output voltage. The device also incorporates an enable pin (EN) that allows the user to turn the part on or off. The MAX17651 has a thermal shutdown feature that shuts down the part when the die temperature exceeds 165°C. The MAX17651 operates over the -40°C to +125°C industrial temperature range and is available in a 6 lead, compact Thin-SOT (TSOT) package.

II. Manufacturing Information

A. Description/Function:	60V, 100mA, Ultra-Low Quiescent Current, Linear Regulator
B. Process:	S18
C. Number of Device Transistors:	6557
D. Fabrication Location:	USA
E. Assembly Location:	Philippines, Thailand
F. Date of Initial Production:	December 10, 2014

III. Packaging Information

A. Package Type:	6-pin TSOT
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-5846
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	365.1°C/W
K. Single Layer Theta Jc:	75°C/W
L. Multi Layer Theta Ja:	110°C/W
M. Multi Layer Theta Jc:	50°C/W

IV. Die Information

A. Dimensions:	33.8583X43.7008 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5% Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns (as drawn)
F. Minimum Metal Spacing:	0.23 microns (as drawn)
G. Isolation Dielectric:	SiO_2
H. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Eric Wright (Reliability Engineering) Brian Standley (Manager, Reliability) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 125C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The PI34 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM: +/- 2500V per JEDEC JESD22-A114
ESD-CDM: +/- 750V per JEDEC JESD22-C101
Latch-Up testing has shown that this device withstands a current of +/-100mA and overvoltage per JEDEC JESD78.

Table 1

Reliability Evaluation Test Results

MAX17651AZT+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 125C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	

Note 1: Life Test Data may represent plastic DIP qualification lots.