RELIABILITY REPORT

FOR

MAX1809Exx

PLASTIC ENCAPSULATED DEVICES

January 28, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX1809 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

The MAX1809 is a reversible energy flow, constant-off-time, pulse-width-modulated (PWM), stepdown DC-DC converter. It is ideal for use in notebook and subnotebook computers that require +1.1V to +5V active termination power supplies. This device features an internal PMOS power switch and internal synchronous rectifier for high efficiency and reduced component count. The internal 90mΩ PMOS power switch and 70mΩ NMOS synchronous-rectifier switch easily deliver continuous load currents up to 3A. The MAX1809 accurately tracks an external reference voltage, produces an adjustable output from +1.1V to V_{IN}, and achieves efficiencies as high as 93%.

The MAX1809 uses a unique current-mode, constant-off-time, PWM control scheme that allows the output to source or sink current. This feature allows energy to return to the input power supply that otherwise would be wasted. The programmable constant-off-time architecture sets switching frequencies up to 1MHz, allowing the user to optimize performance trade-offs between efficiency, output switching noise, component size, and cost. The MAX1809 features an adjustable soft-start to limit surge currents during startup, a 100% duty-cycle mode for low-dropout operation, and a low-power shutdown mode that disables the power switches and reduces supply current below 1µA. The MAX1809 is available in a 28-pin QFN package with an exposed backside pad or a 16-pin QSOP package.

B. Absolute Maximum Ratings

Item	Rating
VCC, IN to Gnd	-0.3V to +6V
IN to VCC	+/-0.3V
GND to PGND	+/-0.3V
/SHDN, SS, FB, TOFF,RREF, EXTREF to GND	-0.3V to (VCC + 0.3V)
LX Current (Note 1)	+/-4.7A
REF Short Circuit to GND Duration	Continous
Operating Temp Range	-40^0C to $+85^0$C
Storage Temp Range	-65^0C to $+150^0$C
Junction Temperature	$+150^0$C
Lead Temp Range (soldering, 10s)	$+300^0$C
Continuous Power Dissipation (TA = $+70^0$)	
28-Pin QFN (part mounted on $1in^2$ of 1oz copper)	1.6W
16-Pin QSOP (part mounted on $1in^2$ of 1oz copper)	1.0W
Derates above +70°C	
28-Pin QFN	20mW/°C
16-Pin QSOP	12.5mW/°C

Note 1: LX has clamp diodes to PGND and IN. If continuous current is applied through these diodes, thermal limits must be observed

II. Manufacturing Information

A. Description/Function:	3A, 1MHz, DDR Memory Termination Supply
B. Process:	S8
C. Number of Device Transistors:	3662
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines, Malaysia or Thailand
F. Date of Initial Production:	July, 2001

III. Packaging Information

A. Package Type:	**28-Pin QFN**	**16-Pin QSOP**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled epoxy	Silver-filled epoxy
E. Bondwire:	Gold (1.2 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1101-0161	Buildsheet # 05-1101-0135
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity Per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	108 x 86 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliablity Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 239 \times 2}$$ (Chi square value for MTTF upper limit)

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 4.54 \times 10^{-9}$ λ= 4.54 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5498) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PX56 die type has been found to have all pins able to withstand a transient pulse of ±600V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX1809Exx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		239	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN QSOP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the uMax package.
Note 2: Generic package/process data

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

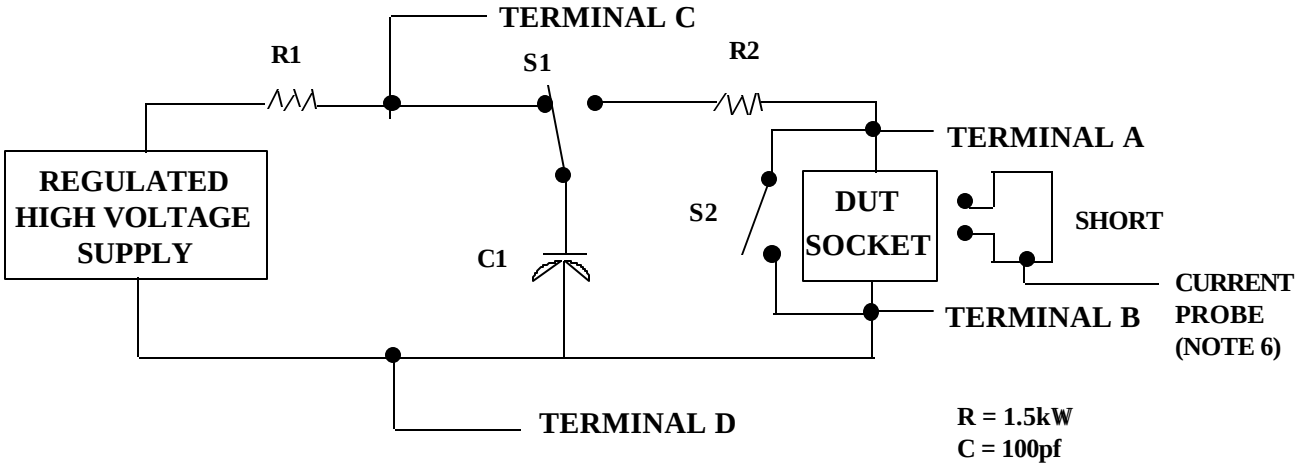
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

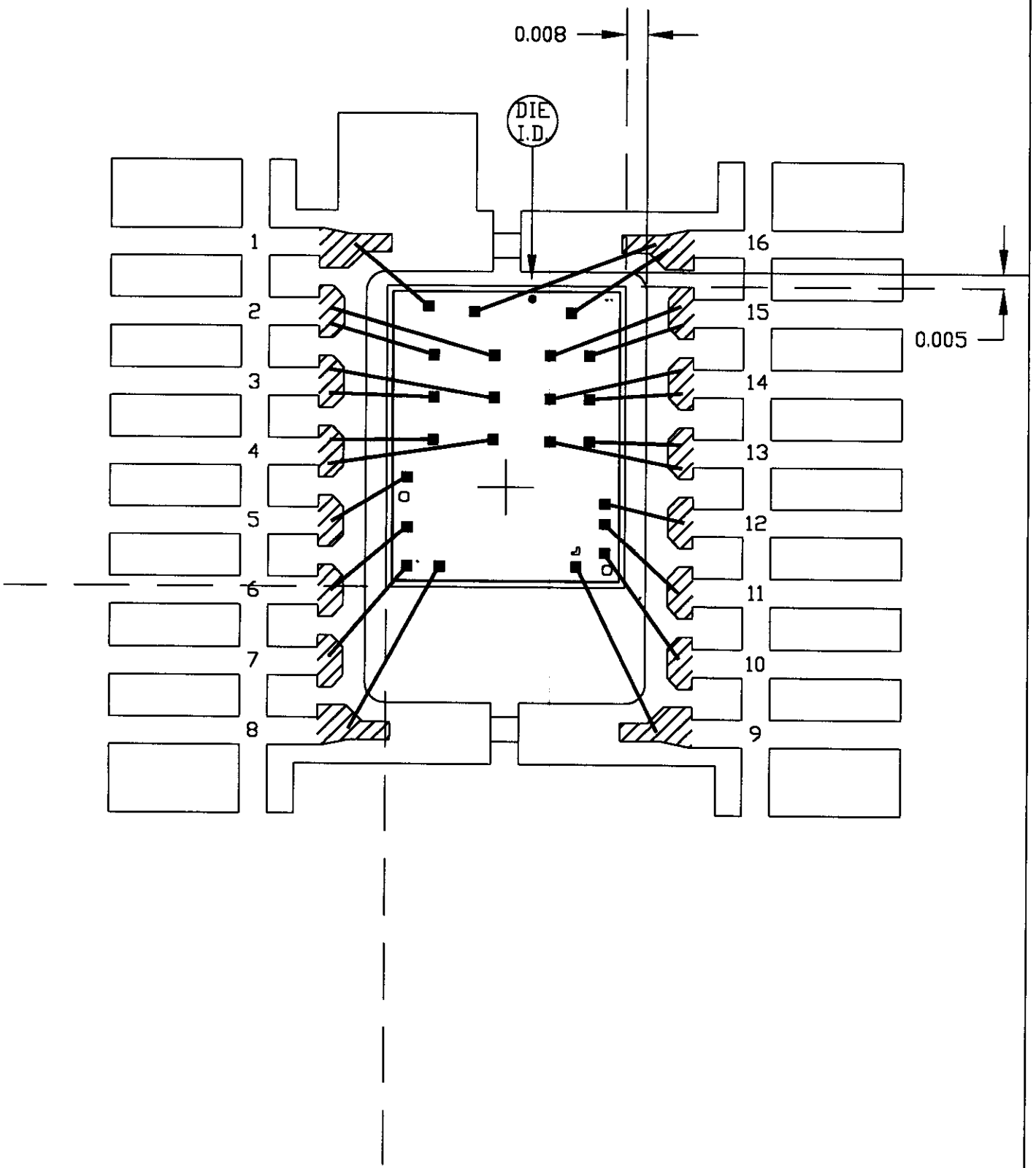
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

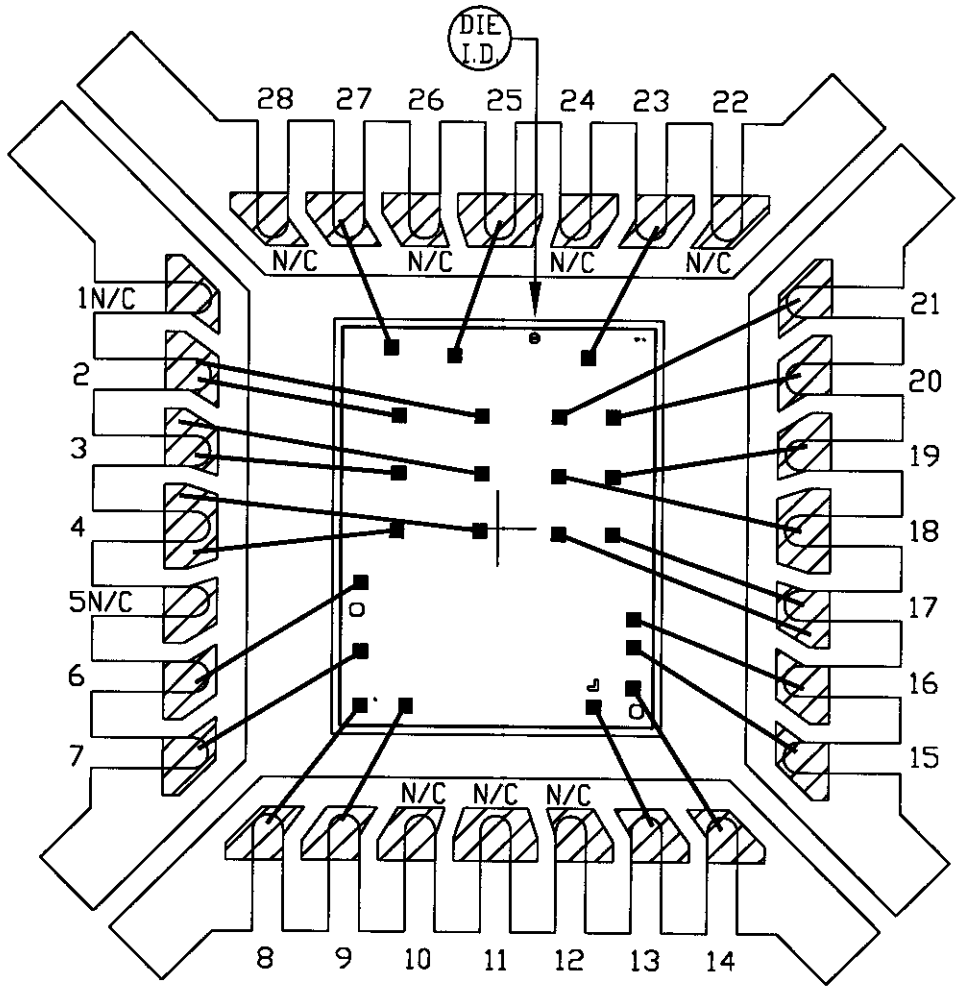
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: E16-5		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 101x154	PKG. DESIGN			BUILDSHEET NUMBER: 05-1101-0135 / REV.: A



NOTES:

1. WIRES 18 AND 19 ALLOWED TO TOUCH EACH OTHER.
2. WIRES 20 AND 21 ALLOWED TO TOUCH EACH OTHER.

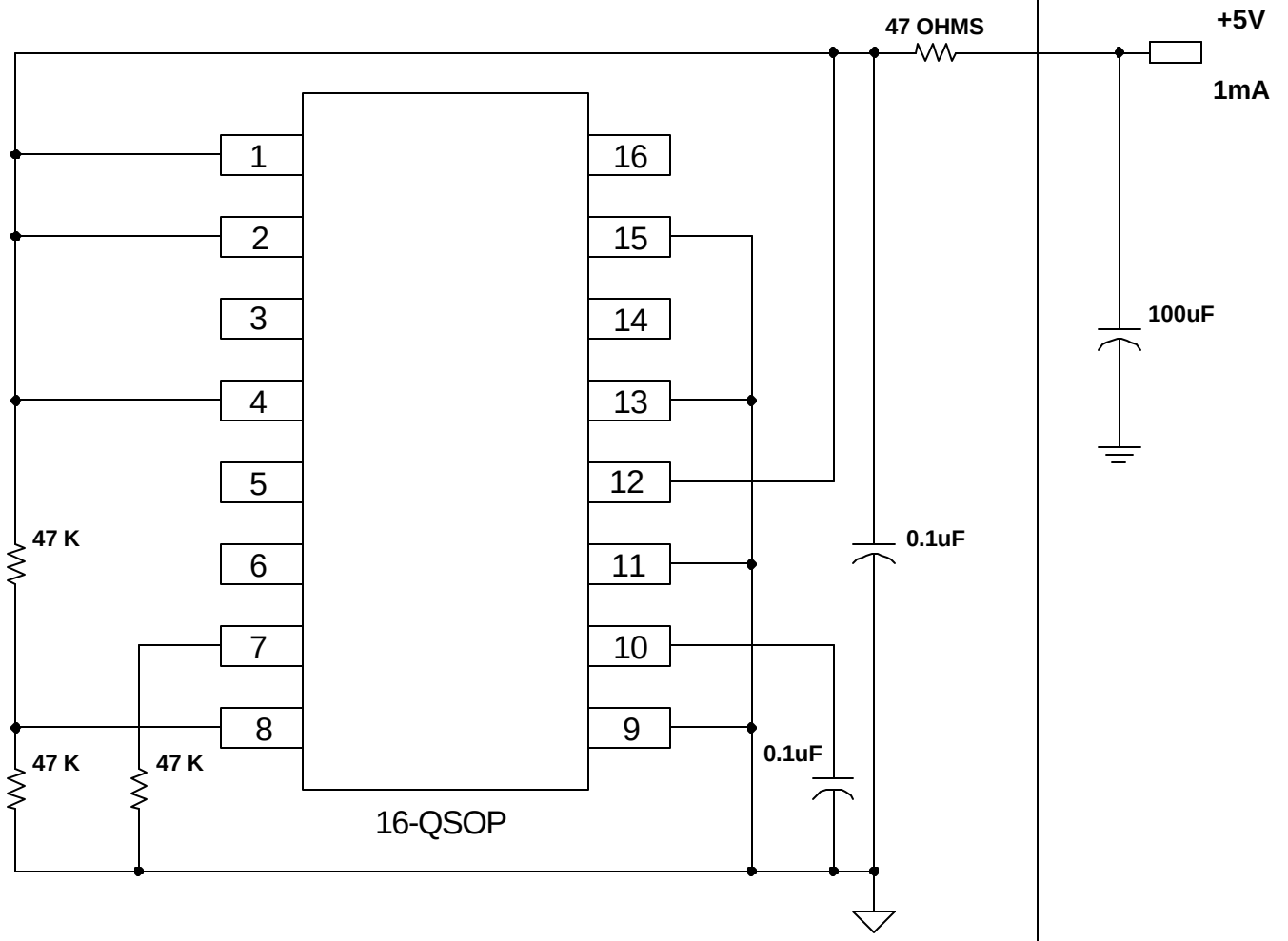
BONDABLE AREA

PKG. BODY SIZE: 5x5 mm

PKG. CODE: G2855-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 130x130	PKG. DESIGN			BOND DIAGRAM #: 05-1101-0161	REV: B

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX1742 / 1842

MAX. EXPECTED CURRENT = 1mA

DRAWN BY: HAK TAN

NOTES: