RELIABILITY REPORT

FOR

MAX1818EUT

PLASTIC ENCAPSULATED DEVICES

November 12, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX1818 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX1818 low-dropout linear regulator operates from a +2.5V to +5.5V supply and delivers a guaranteed 500mA load current with low 120mV dropout. The high-accuracy (±1%) output voltage is preset at an internally trimmed voltage (see Selector Guide) or can be adjusted from 1.25V to 5.0V with an external resistive divider.

An internal PMOS pass transistor allows the low 125µA supply current to remain independent of load, making this device ideal for portable battery-operated equipment such as personal digital assistants (PDAs), cellular phones, cordless phones, base stations, and notebook computers.

Other features include an active-low open-drain reset output that indicates when the output is out of regulation, a 0.1µA shutdown, short-circuit protection, and thermal shutdown protection. The device is available in a miniature 800mW 6-pin SOT23 package.

B. Absolute Maximum Ratings

Item	Rating
IN, SHDN , POK, SET to GND	-0.3V to +6V
OUT to GND	-0.3V to (VIN + 0.3V)
Output Short-Circuit Duration	1min
Continuous Power Dissipation (TA = +70°C) (Note 1)	
6-Pin SOT23 (derate 10mW/°C above +70°C)	800mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s) (Note 2)	+300°C
Continuous Power Dissipation (TA = +70°C)	
10-Pin uMAX	444mW
Derates above +70°C	
10-Pin uMAX	5.6mW/°C

Note 1: Thermal properties are specified with product mounted on PC board with one square-inch of copper area and still air. With minimal copper, the SOT23 package dissipates 712mW at +70°C. With a quarter square inch of copper, it will dissipate 790mW at +70°C. Copper should be equally shared between the IN, OUT, and GND pins.

Note 2: This device is constructed using a unique set of packaging techniques that imposes a limit on the thermal profile to which the device can be exposed during board-level solder attach and rework. The limit permits only the use of the solder profiles recommended in the industry standard specification, IPC JEDEC- J-STD-020A, paragraph 7.6, Table 3 for the IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not allowed.

II. Manufacturing Information

A. Description/Function:	500mA Low-Dropout Linear Regulator in SOT23
B. Process:	S8 - Standard 8 micron silicon gate CMOS
C. Number of Device Transistors:	845
D. Fabrication Location:	California, USA
E. Assembly Location:	Malaysia or USA
F. Date of Initial Production:	October, 2000

III. Packaging Information

A. Package Type:	**6-Lead SOT Flip-Chip**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	None
E. Bondwire:	6 mil dia. ball
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-2301-0052
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	90 X 45 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	TiW/ AlCu/ TiWN
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	2.7 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 317 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 3.43 \times 10^{-9}$ $\lambda = 3.43$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-5597) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**) located on the Maxim website at http://www.maxim-ic.com .

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PY69 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1818EUT

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	317	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

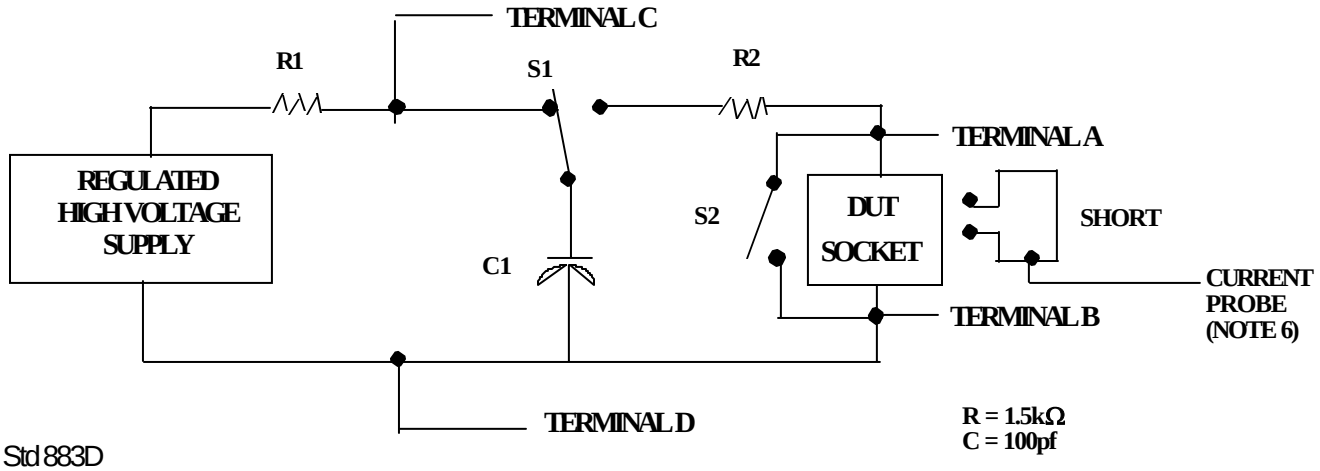
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

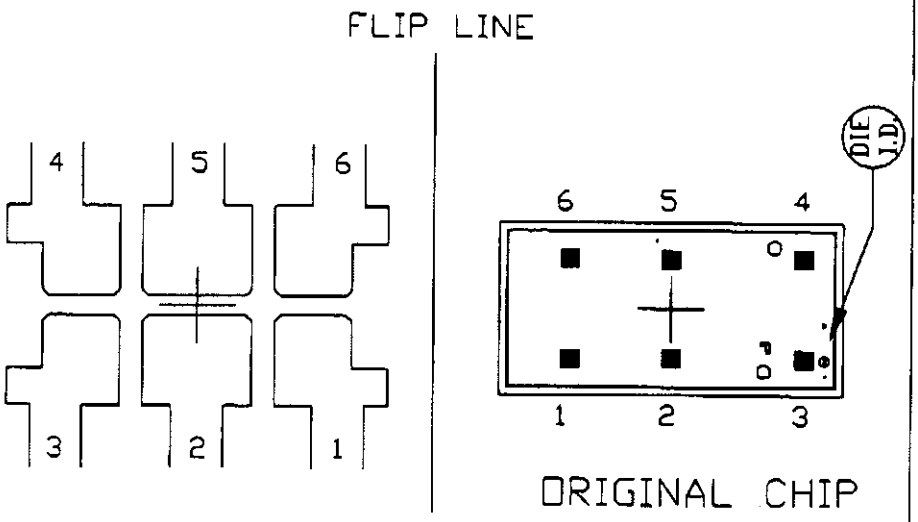
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8

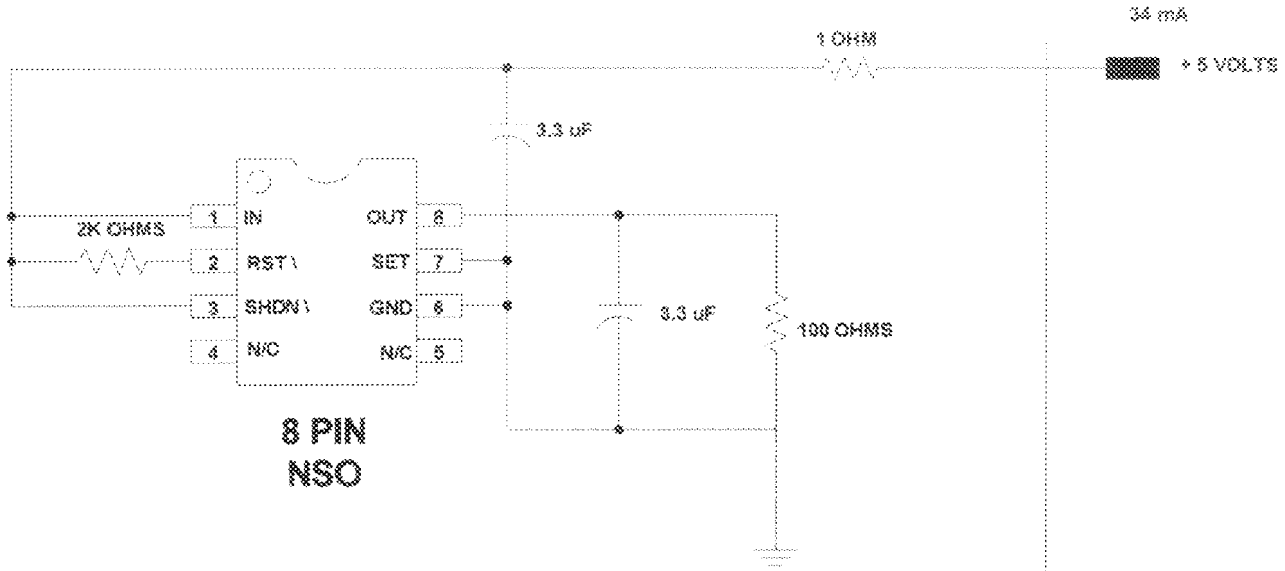
FLIP CHIP PKG.



PKG. CODE: U6F-6		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: FLIP CHIP	PKG.		3/21/00	BOND DIAGRAM #: 05-2301-0052	REV: A
	DESIGN		3/21/00		

ONCE PER SOCKET

ONCE PER BOARD



MAXIM BURN-IN SCHEMATIC SPEC 06-5597 REV. A DATE: 3 / 23 / 2000	DEVICES: MAX 1818 MAX. EXPECTED CURRENT = 34 mA	DRAWN BY: CHRIS JAMBARO NOTES: