RELIABILITY REPORT

FOR

MAX1840EUB+

PLASTIC ENCAPSULATED DEVICES

May 8, 2015

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX1840EUB+ successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX1840/MAX1841 subscriber identity module (SIM)/smart card level translators provide level shifting and electrostatic discharge (ESD) protection for SIM and smart card ports. These devices integrate two unidirectional level shifters for the reset and clock signals, a bidirectional level shifter for the serial data stream, and ±10kV ESD protection on all card contacts. The MAX1840 includes a SHDN control input to aid insertion and removal of SIM and smart cards, while the MAX1841 includes a system-side data driver to support system controllers without open-drain outputs. The logic supply voltage range is +1.4V to +5.5V for the "controller side" and +1.7V to +5.5V for the "card side." Total supply current is 1.0µA. Both devices automatically shut down when either power supply is removed. For a complete SIM card interface, combine the MAX1840/MAX1841 with the MAX1686H 0V/3V/5V regulated charge pump. The MAX1840/MAX1841 are available in ultra-small 10-pin µMAX packages that are only 1.09mm high and half the area of an 8-pin SO. The MAX1840/MAX1841 are compliant with GSM test specifications 11.11 and 11.12.

II. Manufacturing Information

A. Description/Function:	Low-Voltage SIM/Smart-Card Level Translators in µMAX
B. Process:	S12
C. Number of Device Transistors:	
D. Fabrication Location:	Oregon, California or Texas
E. Assembly Location:	Philippines, Thailand, Malaysia
F. Date of Initial Production:	April 22, 2000

III. Packaging Information

A. Package Type:	10-pin uMAX
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-2301-0042
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	180°C/W
K. Single Layer Theta Jc:	41.9°C/W
L. Multi Layer Theta Ja:	113.1°C/W
M. Multi Layer Theta Jc:	41.9°C/W

IV. Die Information

A. Dimensions:	35X54 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% for all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 160 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 6.87 \times 10^{-9}$

$\lambda = 6.87$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S12 Process results in a FIT Rate of 0.01 @ 25C and 0.32 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot S72ACQ001C, D/C 0410)

The PY60 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500V per Mil-Std 883 Method 3015.7. Latch-Up testing has shown that this device withstands a current of +/-250mA.

Table 1
Reliability Evaluation Test Results

MAX1840EUB+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	80	0	N72BBA004A, D/C 0209
	Biased	& functionality	80	0	I72AAQ001A, D/C 0011
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.