RELIABILITY REPORT

FOR

MAX1848ExA

PLASTIC ENCAPSULATED DEVICES

November 25, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX1848 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

The MAX1848 drives white LEDs with a constant current to provide backlight in cell phones, PDAs, and other hand-held devices. The step-up converter topology allows series connection of the white LEDs so that the LED currents are identical for uniform brightness. This configuration eliminates the need for ballast resistors and expensive factory calibration. Other benefits include greater simplicity, lower cost, higher efficiency, and greater reliability.

This step-up PWM converter includes an internal, high-voltage, low R_{DSON} N-channel MOSFET switch for high efficiency and maximum battery life. A single analog voltage Dual Mode™ input provides a simple means of brightness adjustment and on/off control. Fast 1.2MHz current-mode PWM control allows for small input and output capacitors and a small inductor while minimizing ripple on the input supply/battery. Programmable soft-start eliminates inrush current during startup.

The MAX1848 is available in a space-saving, 8-pin SOT23 package.

B. Absolute Maximum Ratings

Item	Rating
V+ to Gnd	-0.3V to +6V
PGND to GND	-0.3V to +0.3V
LX, OUT to GND	-0.3V to +14V
LX to Out	-14V to +0.3V
CTRL to GND	-0.3V to +6.0V or (V+ +2V)
COMP, CS to GND	-0.3V to (V+ +2V)
Continuous LX Output Current	0.45A rms
Operating Temp Range	-40^0C to $+85^0$C
Storage Temp Range	-60^0C to $+150^0$C
Junction Temperature	$+150^0$C
Continuous Power Dissipation (TA = $+70^0$)	
8-Pin SOT23	777mW
8-Pin QFN(3x3)	1951mW
Derates above +70°C	
8-Pin SOT23	9.7mW/°C
8-Pin QFN(3x3)	24.1mW/°C

II. Manufacturing Information

A. Description/Function:	White LED Step-Up Converter
B. Process:	S8
C. Number of Device Transistors:	1290
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	USA, Malaysia or Thailand
F. Date of Initial Production:	April, 2001

III. Packaging Information

A. Package Type:	**8-Lead SOT**	**8-Lead QFN (3x3)**
B. Lead Frame:	Flip-Chip	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled epoxy	Silver-filled epoxy
E. Bondwire:	6.0 mil dia. Solder-ball	Gold (1.3 mil dia)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-3501-0004	Buildsheet # 05-3501-0042
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity Per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	88 x 45 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Copper/Silicon
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliablity Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 13.57 \times 10^{-9}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5761) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PM03 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±200mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX1848ExA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN SOT	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

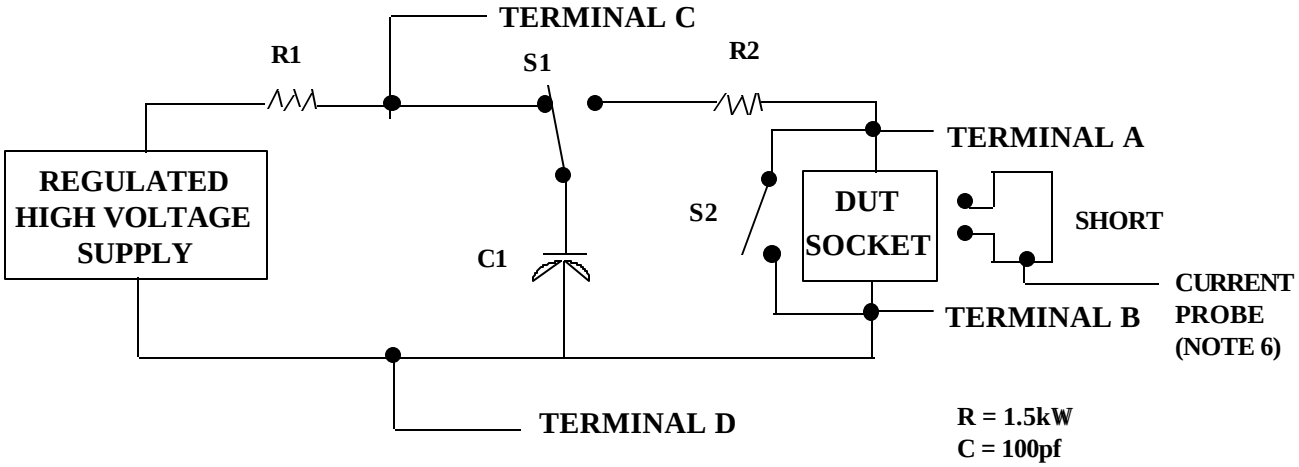
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

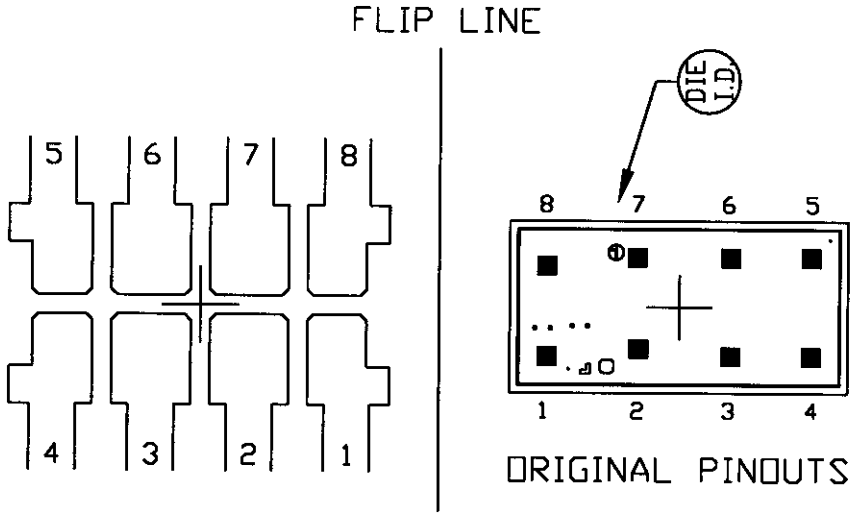
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



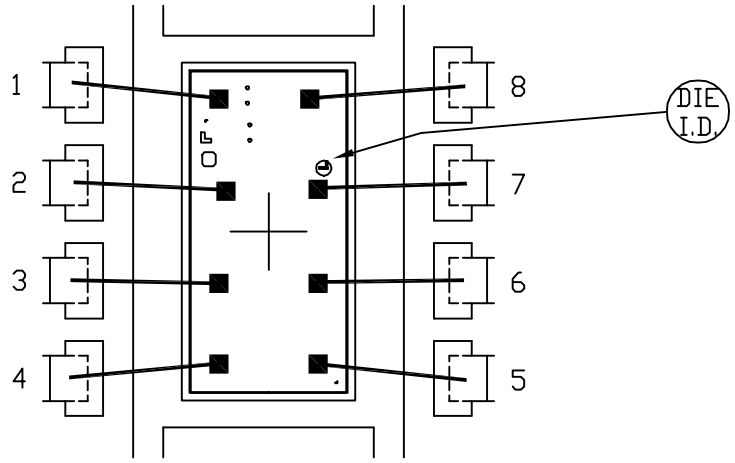
FLIP CHIP PKG.



NOTE: CAVITY DOWN

PKG.CODE: K8F-4		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: FLIP CHIP	PKG. DESIGN			BUILDSHEET NUMBER: 05-3501-0004 / REV.: A

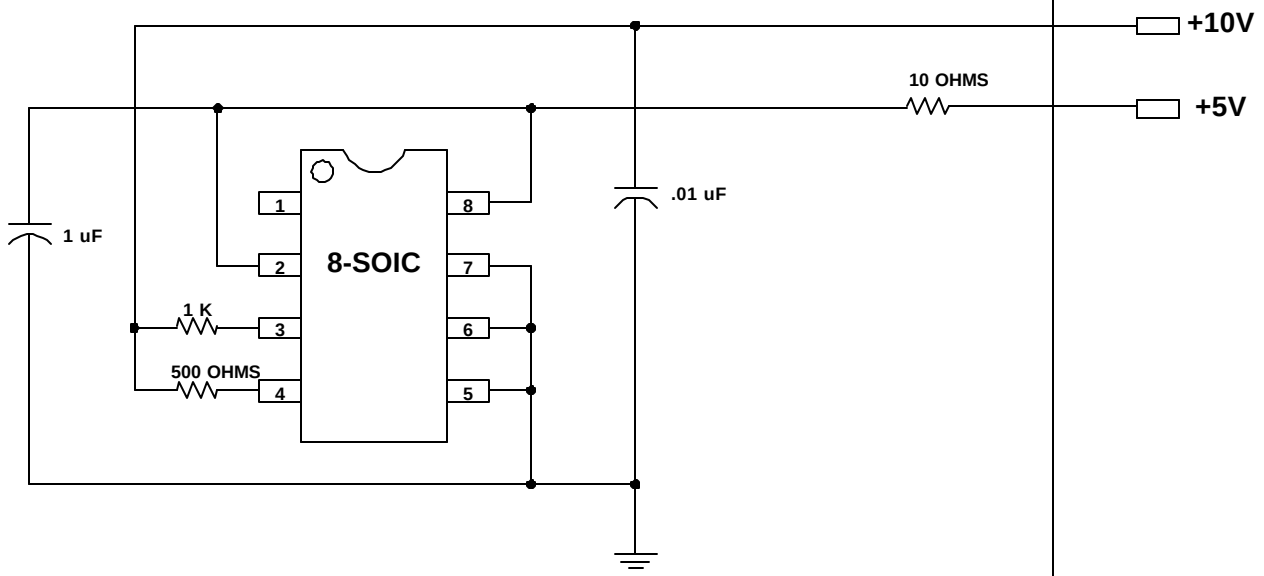
3x3x0.8 MM QFN THIN PKG. EXPOSED PAD PKG.



PKG. CODE: T833-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 71x102	PKG.			BOND DIAGRAM #: 05-3501-0042 REV: B
	DESIGN			

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 1848

MAX. EXPECTED CURRENT = +5V(5mA),+10V(22mA)

DRAWN BY: HAK TAN

NOTES: