RELIABILITY REPORT

FOR

MAX1856EUB

PLASTIC ENCAPSULATED DEVICES

March 25, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX1856 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1856 offers a low-cost solution for generating a SLIC (ringer and off-hook) power supply. Using standard off-the-shelf transformers from multiple vendors, the MAX1856 generates various output voltages: -24V and -72V (dual output) for both ringer and off-hook supplies for voice-enabled broadband consumer premises equipment (CPE), -48V for IP phones and routers, -5V and -15V (single or dual output) for DSL CO line drivers, or negative voltages as high as -185V for MEMS bias supplies. The output voltages are adjusted with an external voltage divider.

Due to its wide operating voltage range, the MAX1856 operates from a low-cost, unregulated DC power supply for cost-sensitive applications like xDSL, cable modems, set-top boxes, LMDS, MMDS, WLL, and FTTH CPE. The MAX1856 provides low audio-band noise for talk battery and a sturdy output capable of handling the ring trip conditions for ring battery.

The operating frequency can be set between 100kHz and 500kHz with an external resistor in free-running mode. For noise-sensitive applications, the MAX1856's operating frequency can be synchronized to an external clock over its operating frequency range.

The flyback topology allows operation close to 50% duty cycle, offering high transformer utilization, low ripple current, and less stress on input and output capacitors. Internal soft-start minimizes startup stress on the input capacitor, without any external components.

The MAX1856's current-mode control scheme does not require external loop compensation. The low-side current-sense resistor provides accurate current-mode control and overcurrent protection.

B. Absolute Maximum Ratings

Item	Rating
V_{CC}, SYNC/SHDN to GND	-0.3V to +30V
PGND to GND	-0.3V to +0.3V
LDO, FREQ, FB, CS to GND	-0.3Vto +6.0V
EXT,REF to GND	-0.3V to (VLDO + 0.3V)
LDO Output Current	-1mA to +20mA
REF Short Circuit to GND	Continuous
Storage Temp.	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
10-Pin uMAX	444mW
Derates above +70°C	
10-Pin uMAX	5.6mW/°C

II. Manufacturing Information

A. Description/Function:	Wide Input Range, Synchronizable, PWM SLIC Power Supply
B. Process:	S12 – Silicon Gate 1.2 micron CMOS
C. Number of Device Transistors:	1538
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Malaysia or Philippines
F. Date of Initial Production:	March, 2001

III. Packaging Information

A. Package Type:	**10-Lead uMAX**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Bonding Diagram	05-2301-0088
H. Flammability Rating:	Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions:	58 x 81 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 80 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.58 \times 10^{-9}$ $\lambda = 13.58$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5679) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PY98 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX1856EUB

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uMAX	419	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

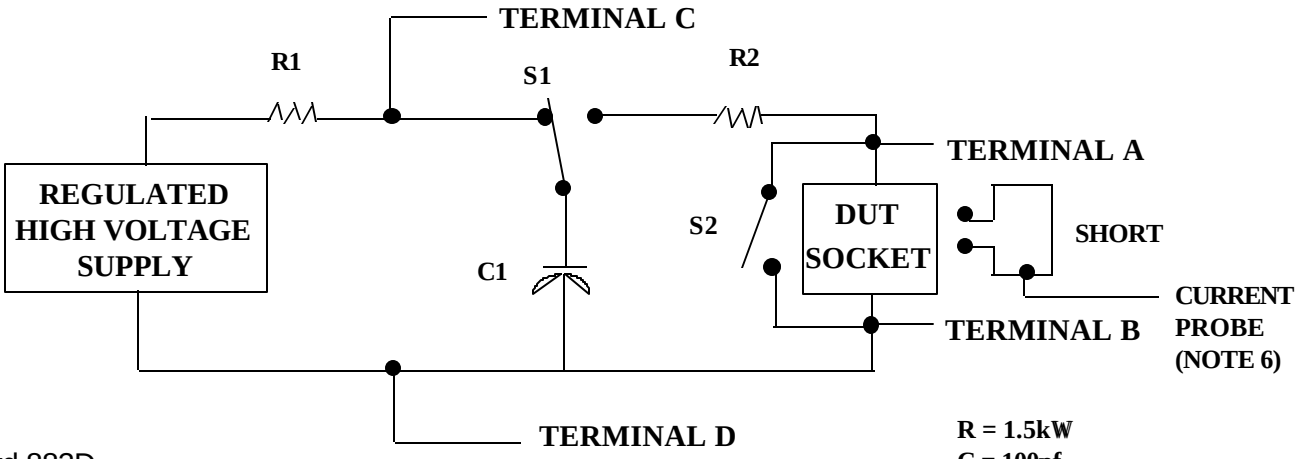
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

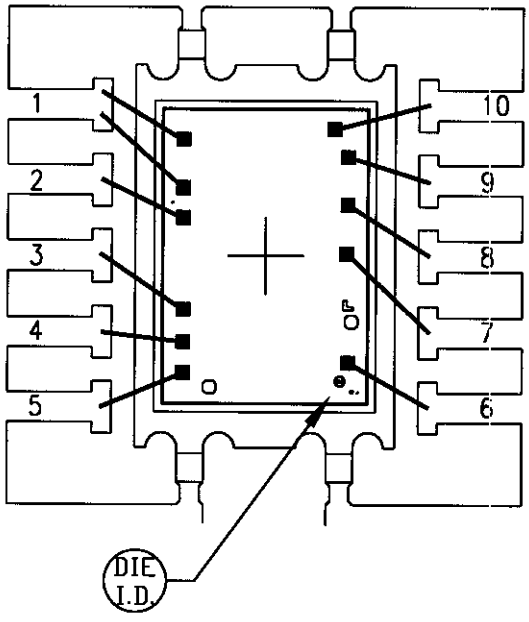
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

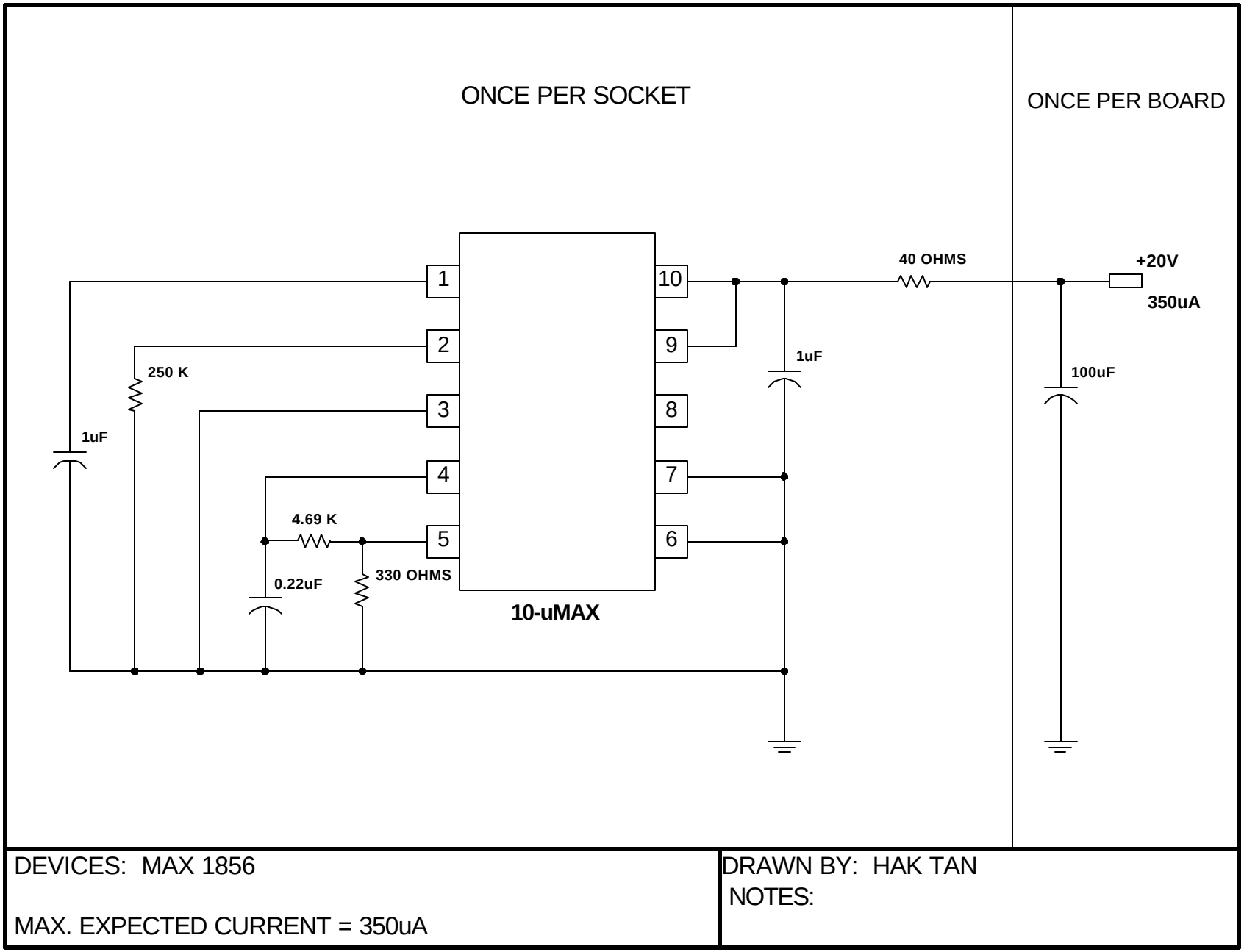
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



PKG. CODE: U10-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY
CAV./PAD SIZE: 68x94	PKG.			BOND DIAGRAM #: 05-2301-0088 REV: A
	DESIGN			



DEVICES: MAX 1856

MAX. EXPECTED CURRENT = 350uA

DRAWN BY: HAK TAN

NOTES: