RELIABILITY REPORT

FOR

MAX1939EEI

PLASTIC ENCAPSULATED DEVICES

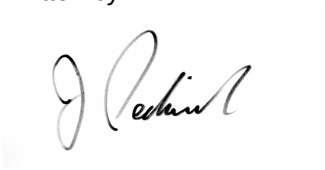
July 9, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX1939 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1939 is a two-phase, step-down controller capable of delivering load currents up to 60A. The controller utilizes Quick-PWM™ control architecture in conjunction with active load-current voltage positioning. Quick-PWM control provides instantaneous load-step response, while programmable voltage positioning allows the converter to utilize full transient regulation limits, reducing the output capacitance requirement. The two phases operate 180° out-of-phase with an effective 500kHz switching frequency, thus reducing input and output current ripple, as well as reducing input filter capacitor requirements.

The MAX1939 is compliant with AMD Hammer, Intel®, Voltage-Regulator Module (VRM) 9.0/9.1, and AMD Athlon™ Mobile VID code specifications (see Table 1 for VID codes). The internal DAC provides ultra-high accuracy of ±0.75%. A controlled VID voltage transition is implemented to minimize both undervoltage and overvoltage overshoot during VID input change.

Remote sensing is available for high output-voltage accuracy. The MOSFET switches are driven by a 6V gate-drive circuit to minimize switching and crossover conduction losses to achieve efficiency as high as 90%. The MAX1939 features cycle-by-cycle current limit to ensure that the current limit is not exceeded. Crowbar protection is available to protect against output overvoltage.

B. Absolute Maximum Ratings

Item	Rating
VCC to GND	-0.3V to +28V
VDD, PWRGD, ILIM, FB to GND	-0.3V to +6V
EN, GNDS, VPOS, REF, VID_, TIME to GND	0.3V to VVDD + 0.3V
PGND to GND	-0.3V to +0.3V
CS1, CS2 to GND	-2V to +28V
VLG to GND	-0.3V to +7V
BST1, BST2 to GND	-0.3V to +35V
LX1 to BST1	-7V to +0.3V
LX2 to BST2	-7V to +0.3V
DH1 to LX1	-0.3V to VBST1 + 0.3V
DH2 to LX2	-0.3V to VBST2 + 0.3V
DL1, DL2 to PGND	-0.3V to VVLG + 0.3V
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
28-Pin QSOP	860.2mW
Derates above +70°C	
28-Pin QSOP	20.8mW/°C

II. Manufacturing Information

A. Description/Function: Two-Phase Desktop CPU Core Supply Controller with Controlled VID Change

B. Process: S12 (Standard 1.2 micron silicon gate CMOS)

C. Number of Device Transistors: 6243

D. Fabrication Location: Oregon, or California

E. Assembly Location: Philippines or Thailand, USA

F. Date of Initial Production: October, 2002

III. Packaging Information

A. Package Type: 28-Pin QSOP

B. Lead Frame: Copper

C. Lead Finish: Solder Plate

D. Die Attach: Silver-filled Epoxy

E. Bondwire: Gold (1.3 mil dia.)

F. Mold Material: Epoxy with silica filler

G. Assembly Diagram: 05-3501-0039

H. Flammability Rating: Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 86 x 175 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 45 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 24.13 \times 10^{-9}$ $\lambda = 24.13$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5995) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PM46-1 die type has been found to have all pins able to withstand a transient pulse of ±400V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA.

Table 1
Reliability Evaluation Test Results

MAX1939EEI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION		SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		45	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QSOP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

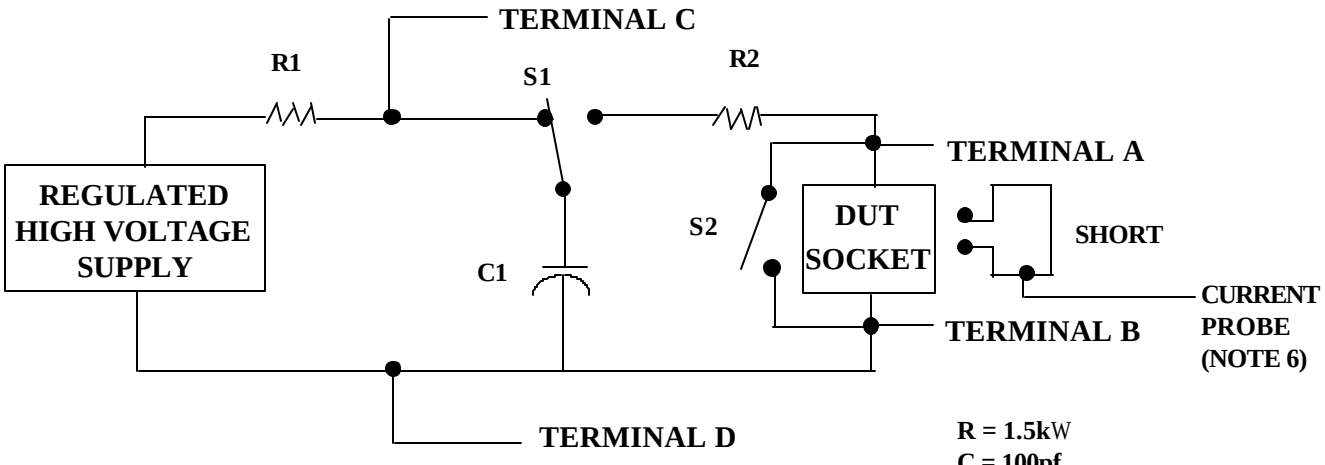
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

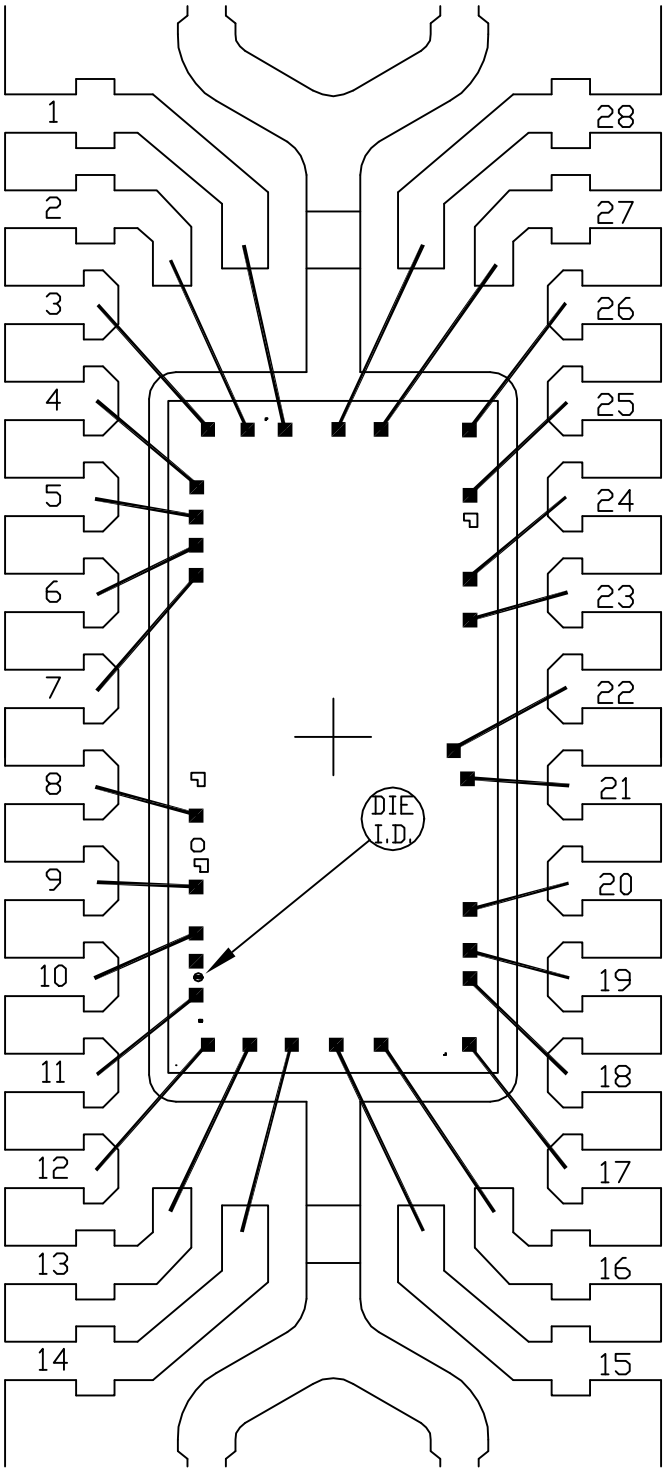
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



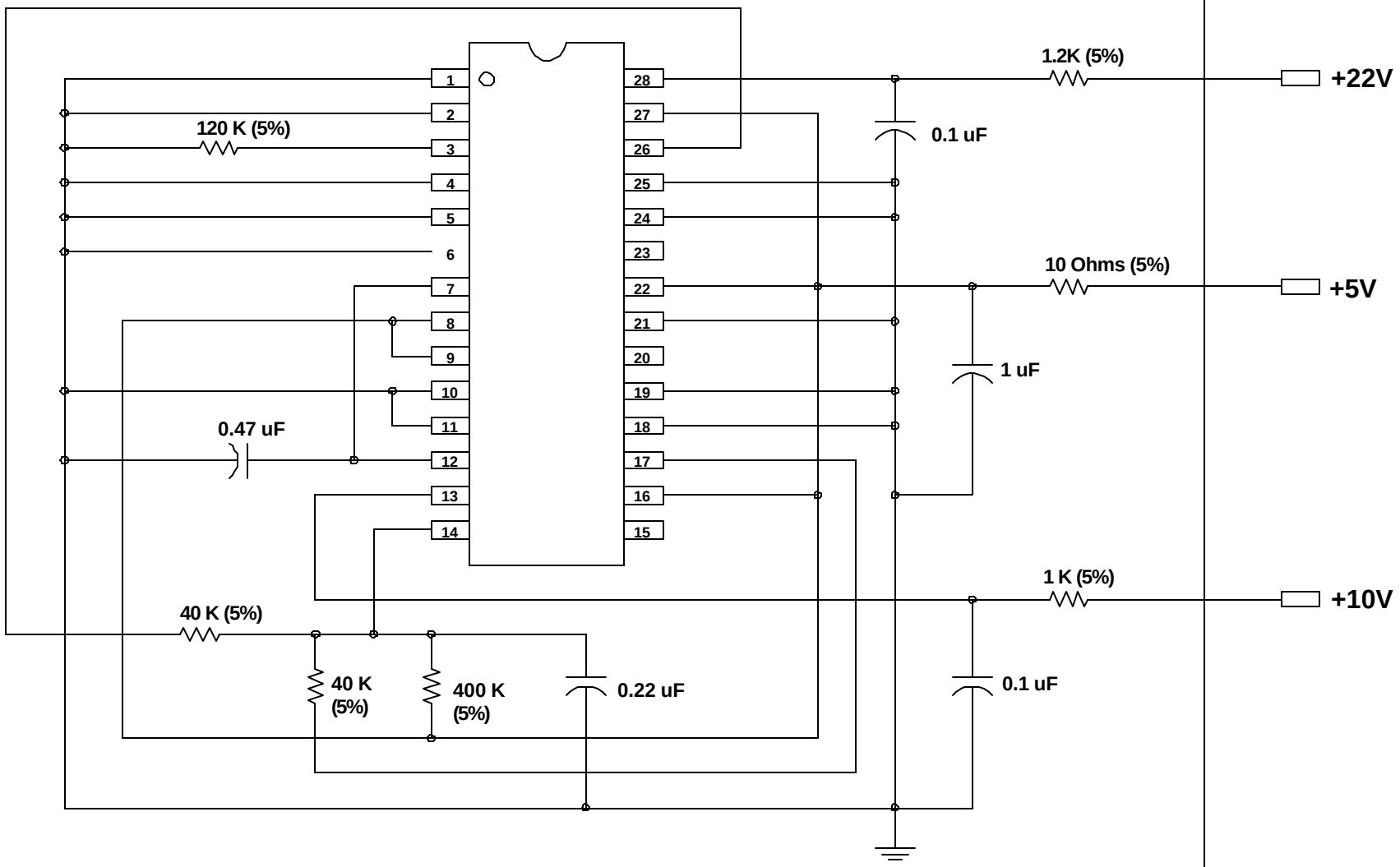
Mil Std 883D
Method 3015.7
Notice 8



PKG. CODE: E28-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 96X190	PKG.			BOND DIAGRAM #: 05-3501-0039	REV: A
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX1937/8/9
PACKAGE: 28-QSOP
MAX. EXPECTED CURRENT = 10mA (+5V), 0.5mA (+10V), 0.2mA (+22V).

DRAWN BY: TEK TAN
NOTES: