RELIABILITY REPORT

FOR

MAX19713ETN+

PLASTIC ENCAPSULATED DEVICES

April 20, 2009

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

The MAX19713ETN+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim"s continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim"s quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX19713 is an ultra-low-power, highly integrated mixed-signal analog front-end (AFE) ideal for wideband communication applications operating in full-duplex (FD) mode. Optimized for high dynamic performance and ultra-low power, the device integrates a dual 10-bit, 45Msps receive (Rx) ADC; dual 10-bit, 45Msps transmit (Tx) DAC; three fast-settling 12-bit aux-DAC channels for ancillary RF front-end control; and a 10-bit, 333ksps housekeeping aux-ADC. The typical operating power in FD mode is 91.8mW at a 45MHz clock frequency. The Rx ADCs feature 54dB SINAD and 72.2dBc SFDR at 5.5MHz input frequency with a 45MHz clock frequency. The analog I/Q input amplifiers are fully differential and accept 1.024VP-P full-scale signals. Typical I/Q channel matching is ±0.03 phase and ±0.02dB gain. The Tx DACs feature 70.3dBc SFDR at fOUT = 2.2MHz and fCLK = 45MHz. The analog I/Q full-scale output voltage range is ±400mV differential. The output DC common-mode voltage is selectable from 0.71V to 1.06V. The I/Q channel offset is adjustable to optimize radio lineup sideband/carrier suppression. Typical I/Q channel matching is ±0.01dB gain and ±0.05° phase. Two independent 10-bit parallel, high-speed digital buses used by the Rx ADC and Tx DAC allow full-duplex operation for frequency-division duplex applications. The Rx ADC and Tx DAC can be disabled independently to optimize power management. A 3-wire serial interface controls power-management modes, the aux-DAC channels, and the aux-ADC channels. The MAX19713 operates on a single 2.7V to 3.3V analog supply and 1.8V to 3.3V digital I/O supply. The MAX19713 is specified for the extended (-40°C to +85°C) temperature range and is available in a 56-pin, thin QFN package. The Selector Guide at the end of the data sheet lists other pin-compatible versions in this AFE family. For time-division duplex (TDD) applications, refer to the MAX19705-MAX19708 AFE family of products.

II. Manufacturing Information

A. Description/Function:	10-Bit, 45Msps, Full-Duplex, Analog Front-End
B. Process:	TS352P4M
C. Number of Device Transistors:	
D. Fabrication Location:	Taiwan
E. Assembly Location:	UTL Thailand
F. Date of Initial Production:	April 21, 2006

III. Packaging Information

A. Package Type:	56-pin TQFN 7x7
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2172
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	36°C/W
K. Single Layer Theta Jc:	0.8°C/W
L. Multi Layer Theta Ja:	25°C/W
M. Multi Layer Theta Jc:	0.8°C/W

IV. Die Information

A. Dimensions:	146 X 169 mils
B. Passivation:	Silicon Dioxide/Silicon Nitride
C. Interconnect:	Al/Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35 um
F. Minimum Metal Spacing:	0.35 um
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	Silicon Dioxide
I. Die Separation Method:	Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Ken Wendel (Director, Reliability Engineering) Bryan Preeshl (Managing Director of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 50 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 21.5 \times 10^{-9}$

$\lambda = 21.5$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly 1000 hour life test monitors on its processes. This data is published in the Product Reliability Report found at http://www.maxim-ic.com/. Current monitor data for the TS352P4M Process results in a FIT Rate of 0.43 @ 25C and 7.50 @ 55C (0.8 eV, 60% UCL)

B. Moisture Resistance Tests

The industry standard 85°C/85%RH or HAST testing is monitored per device process once a quarter.

C. E.S.D. and Latch-Up Testing

The CA23-2 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2500 V per JEDEC JESD22-A114-D. Latch-Up testing has shown that this device withstands a current of +/-250 mA.

Table 1
Reliability Evaluation Test Results

MAX19713ETN+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	50	0
Moisture Testing (Note 2)				
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data