RELIABILITY REPORT

FOR

MAX1996AEGI

PLASTIC ENCAPSULATED DEVICES

May 28, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX1996A successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX1996A integrated controller is optimized to drive cold-cathode fluorescent lamps (CCFLs) using synchronized full-bridge inverter architecture. Synchronized drive provides near sinusoidal waveforms over the entire input range to maximize the life of CCFLs. The controller also operates over a wide input-voltage range with high efficiency and broad dimming range.

The MAX1996A includes safety features that limit the transformer secondary voltage and protect against single-point fault conditions including lamp-out and short-circuit faults.

The MAX1996A regulates the CCFL brightness in three ways: linearly controlling the lamp current, digital pulse-width modulating (DPWM) the lamp current, or using both methods simultaneously to achieve the widest dimming range (>30:1). CCFL brightness can be controlled with either an analog voltage or a 2-wire SMBus™-compatible interface. The MAX1996A directly drives the four external N-channel power MOSFETs of the full bridge inverter. An internal 5.3V linear regulator powers the MOSFET drivers, the synchronizable DPWM oscillator, and most of the internal circuitry.

The MAX1996A has the same pin configuration as the MAX1895, but with modified SMBus slave address (0x58) and command bytes. In addition, the lamp-out protection timer has been reduced to approximately 1s and the DPWM frequency is guaranteed from 200Hz to 220Hz over the operating temperature range without external components or trimming. The MAX1996A is available in the space-saving 28-pin QFN package and operates over a -40°C to +85°C temperature range.

B. Absolute Maximum Ratings

Item	Rating
BATT to GND	-0.3V to +30V
BST1,BST2 to GND	-0.3V to +36V
BST1 to LX1, BST2 to LX2	-0.3V to +6V
GH1 to LX1	-0.3V to (BST1 + 0.3V)
GH2 to LX2	-0.3V to (BST2 + 0.3V)
VCC,VDD to GND	-0.3V to +6V
REF,ILIM to GND	-0.3V to (VCC + 0.3V)
GL1,GL2 to GND	-0.3V to (VDD +0.3V)
MINDAC,IFB,CCV,CCI to GND	-0.3V to +6V
MODE to GND	-6V to +12V
VFB to GND	-6V to +6V
CRF/SDA,CTL/SCL,SH/SUS to GND	-0.3V to +6V
PGND to GND	-0.3V to +0.3V
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA = +70°C)	
28-Pin QFN	1667mW
Derates above +70°C	
28-Pin QFN	20.48mW/°C

II. Manufacturing Information

A. Description:	High-Efficiency, Wide Brightness Range, CCFL Backlight Controller
B. Process:	S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	7364
D. Fabrication Location:	Oregon or California, USA
E. Assembly Location:	Korea
F. Date of Initial Production:	January, 2002

III. Packaging Information

A. Package Type:	**28-Lead QFN**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-3801-0001
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	120 x 120 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{4.04}{192 \times 4389 \times 78 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 30.73 \times 10^{-9}$ $\lambda = 30.73$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5788) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The PD04-1 die type has been found to have all pins able to withstand a transient pulse of +/-600V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1

Reliability Evaluation Test Results

MAX1996AEGI

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	78	1
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

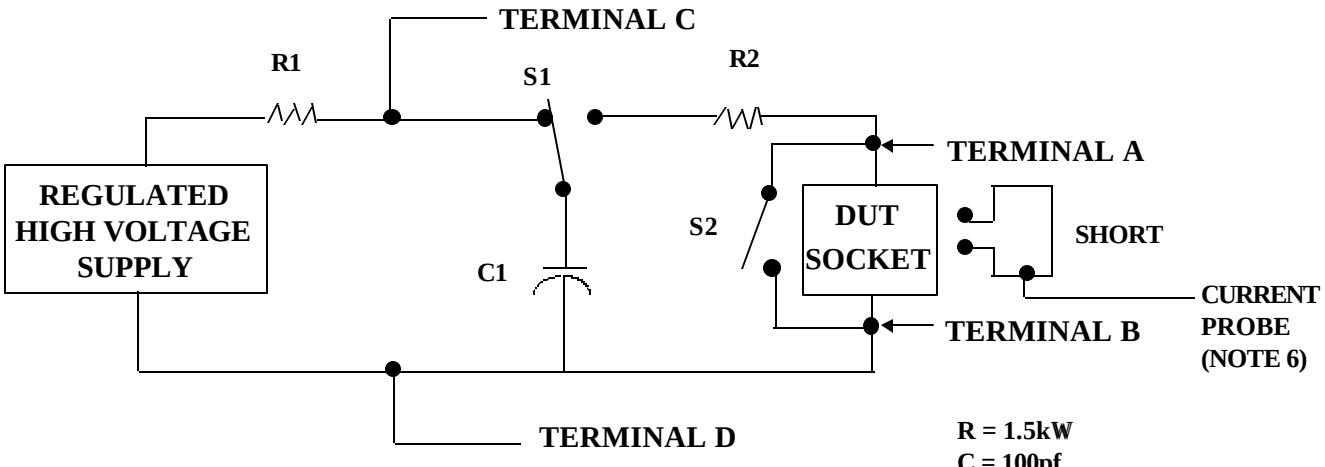
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

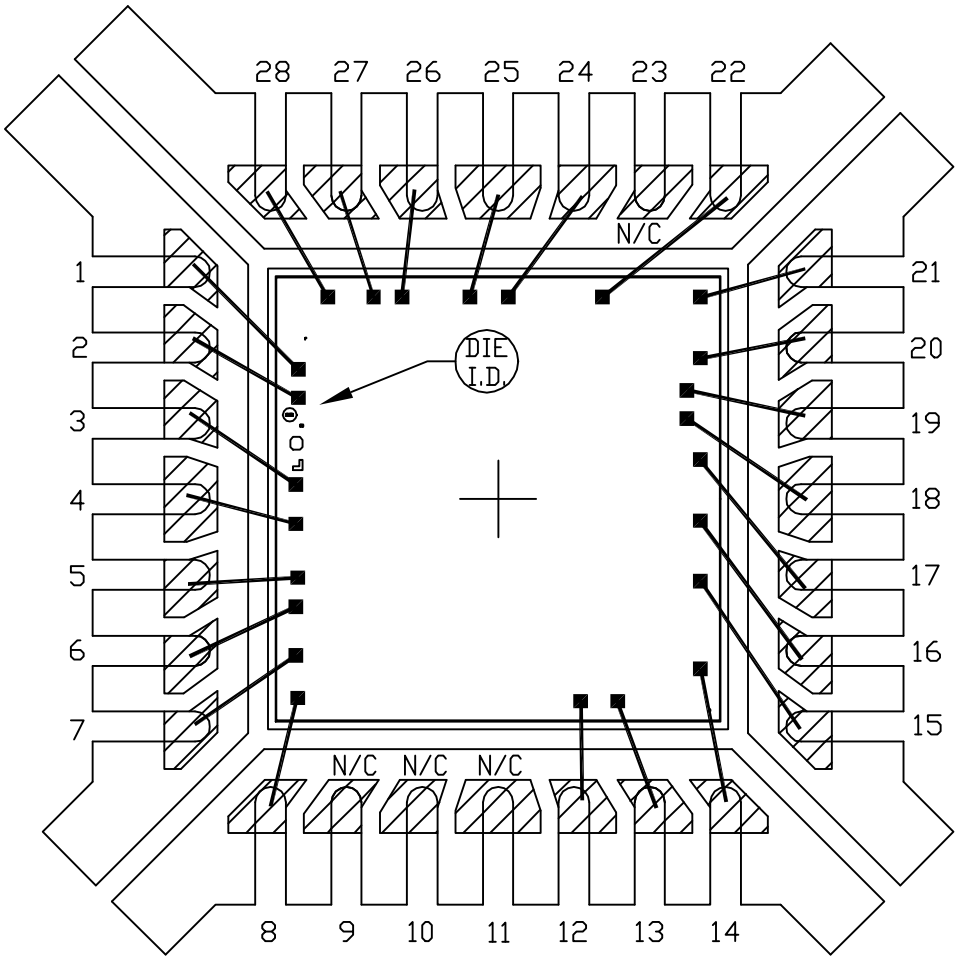
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8

EXPOSED PAD PKG.



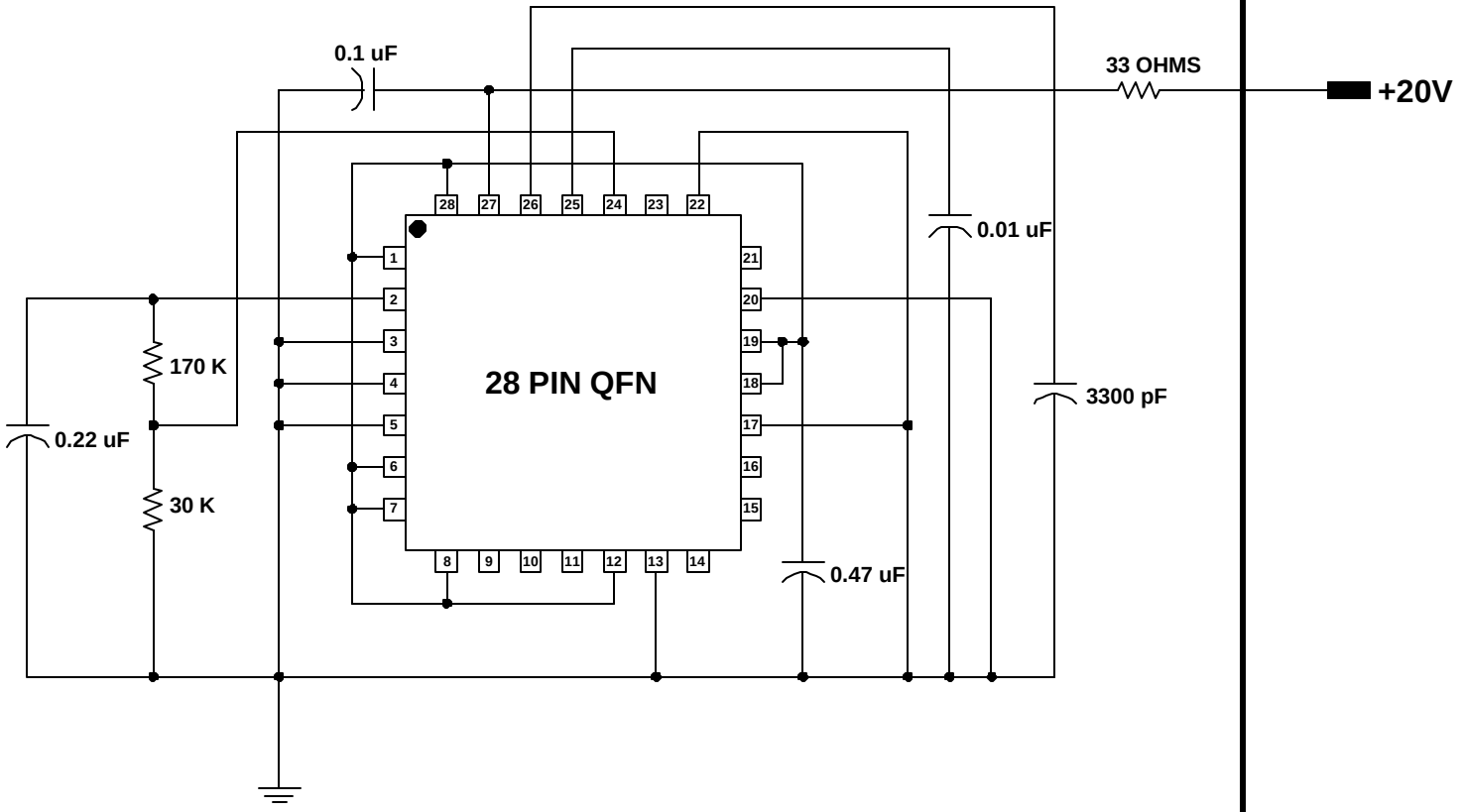
BONDABLE AREA

PKG. BODY SIZE: 5x5 mm

PKG. CODE: G2855-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 130x130	PKG.		3/15/01	BOND DIAGRAM #: 05-3801-0001	REV: A
	DESIGN		3/16/01		

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 1895

MAX. EXPECTED CURRENT = 6mA

DRAWN BY: TEK TAN

NOTES: Package Body 5mm X 5mm.