RELIABILITY REPORT

FOR

MAX20310AEWE+T

WAFER LEVEL DEVICES

January 27, 2017

**MAXIM INTEGRATED**

160 RIO ROBLES

SAN JOSE, CA 95134

| **Approved by** |
| --- |
| Eric Wright |
| Quality Assurance |
| Reliability Engineer |

## Conclusion

The MAX20310AEWE+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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## I. Device Description

A. General

The MAX20310 is a compact power management solution for space-constrained, battery-powered applications where size and efficiency are critical. The device combines two buck-boosted outputs with two LDOs and other system power management features like a push-button monitor and sequencing controller.

The device includes a dual-output, programmable, micro-IQ high-efficiency switching converter. The MAX20310 operates with battery voltages down to 0.7V for use with Zinc Air or Alkaline batteries. The architecture allows for output voltages above or below the battery voltage.

Additionally, the MAX20310 has two programmable low-dropout (LDO) linear regulators. The linear regulators can also operate as power switches that can disconnect the quiescent load of system peripherals. The MAX20310 includes a programmable power controller that allows the device to be configured for use in applications that require a true off state or for always-on applications. This controller provides a delayed reset signal, voltage sequencing, and customized button timing for on/off control and recovery hard reset. The device also features a multiplexer for monitoring the power inputs and outputs of each function. The MAX20310 is available in a 16-bump 0.4mm pitch 1.63mm x 1.63mm wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | Power Management Solution |
| B. Process: | S18 |
| C. Number of Device Transistors: | 71327 |
| D. Fabrication Location: | USA |
| E. Assembly Location: | Taiwan |
| F. Date of Initial Production: | October 26, 2016 |

## III. Packaging Information

| | |
|---|---|
| A. Package Type: | 16-bump WLP |
| B. Lead Frame: | N/A |
| C. Lead Finish: | N/A |
| D. Die Attach: | None |
| E. Bondwire: | N/A (N/A mil dia.) |
| F. Mold Material: | None |
| G. Assembly Diagram: | #05-100330 |
| H. Flammability Rating: | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C | Level 1 |
| J. Single Layer Theta Ja: | N/A°C/W |
| K. Single Layer Theta Jc: | N/A°C/W |
| L. Multi Layer Theta Ja: | 58°C/W |
| M. Multi Layer Theta Jc: | N/A°C/W |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 64.9606X64.9606 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Al/0.5%Cu with Ti/TiN Barrier |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 0.23 microns (as drawn) |
| F. Minimum Metal Spacing: | 0.23 microns (as drawn) |
| G. Isolation Dielectric: | $SiO_2$ |
| H. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

| | |
|---|---|
| A. Quality Assurance Contacts: | Eric Wright (Reliability Engineering)<br>Bryan Preeshl (Vice President of QA) |
| B. Outgoing Inspection Level: | 0.1% for all electrical parameters guaranteed by the Datasheet.<br>0.1% for all Visual Defects. |
| C. Observed Outgoing Defect Rate: | < 50 ppm |
| D. Sampling Plan: | Mil-Std-105D |

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate ($\lambda$) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

$\lambda = 13.7$ F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The AL98-0 die type has been found to have all pins able to withstand an HBM transient pulse of +/-2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.

**Table 1**
Reliability Evaluation Test Results

**MAX20310AEWE+T**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | SAMPLE SIZE | NUMBER OF FAILURES | COMMENTS |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | 80 | 0 | |

Note 1: Life Test Data may represent plastic DIP qualification lots.