RELIABILITY REPORT

FOR

MAX2207EBS+T

CHIP SCALE PACKAGE

January 15, 2013

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX2207EBS+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX2205-MAX2208 wideband (800MHz to 2GHz) power detectors are ideal for GSM/EDGE (MAX2206), TDMA (MAX2207), and CDMA (MAX2205/MAX2208) applications. The MAX2206/MAX2207/MAX2208 take an RF signal from a directional coupler at the input, and output a highly repeatable voltage. The output voltage increases monotonically with increasing input power. The output is compensated for temperature and process shifts, reducing the worst-case variation to less than ±1dB at full power and ±2.5dB at the lowest power. The MAX2206 features 40dB dynamic range, making it ideally suited to GSM/EDGE applications. The MAX2207 offers reduced current consumption for TDMA applications. The MAX2205/MAX2208 each have an integrated filter to allow for average power detection of CDMA signals over a 25dB dynamic range. The MAX2206/MAX2207/MAX2208 offer internal 50Ω termination for interfacing with a directional coupler. The MAX2205 has a high-impedance input to provide a low-loss resistive tap in CDMA applications. All devices allow the user to control the averaging time constant externally. The MAX2205-MAX2208 come in a space-saving 2 x 2, 0.5mm-pitch UCSP™; and require only three external components.

II. Manufacturing Information

A. Description/Function:	RF Power Detectors in UCSP
B. Process:	GST2
C. Number of Device Transistors:	344
D. Fabrication Location:	USA
E. Assembly Location:	USA
F. Date of Initial Production:	April 28, 2001

III. Packaging Information

A. Package Type:	4-pin UCSP
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A
F. Mold Material:	None
G. Assembly Diagram:	#05-3201-0008
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	335°C/W
M. Multi Layer Theta Jc:	°C/W

IV. Die Information

A. Dimensions:	40 X 40 mils
B. Passivation:	Si_3N_4 (Silicon nitride)
C. Interconnect:	Au
D. Backside Metallization:	None
E. Minimum Metal Width:	2 microns (as drawn)
F. Minimum Metal Spacing:	2 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering) Don Lipps (Manager, Reliability Engineering) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9706 \times 155 \times 2}$$ (Chi square value for MTTF upper limit)

(where 9706 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 3.2 \times 10^{-9}$

λ = 3.2 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the GST2 Process results in a FIT Rate of 0.03 @ 25C and 0.48 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing

The WC15-2 die type has been found to have all pins able to withstand a transient pulse of:

ESD-HBM:	+/- 2000V per Mil-Std 883 Method 3015.7 (lot N272AQ001A, D/C 0131)
ESD-CDM:	+/- 750V per JEDEC JESD22-C101 (lot N272EA042A, D/C 0932)

Latch-Up testing has shown that this device withstands a current of 250mA (lot N272AQ001A, D/C 0131).

Table 1

Reliability Evaluation Test Results

MAX2207EBS+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality	77 78	0 0	N273EA383B, D/C 0740 N273EA495B, D/C 0740

Note 1: Life Test Data may represent plastic DIP qualification lots.