RELIABILITY REPORT

FOR

MAX2870ETJ+T

PLASTIC ENCAPSULATED DEVICES

November 12, 2012

MAXIM INTEGRATED

160 RIO ROBLES

SAN JOSE, CA 95134

Approved by
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Quality Assurance
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Conclusion

The MAX2870ETJ+T successfully meets the quality and reliability standards required of all Maxim Integrated products. In addition, Maxim Integrated's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim Integrated's quality and reliability standards.

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I. Device Description

A. General

The MAX2870 is an ultra-wideband phase-locked loop (PLL) with integrated voltage controlled oscillators (VCOs) capable of operating in both integer-N and fractional-N modes. When combined with an external reference oscillator and loop filter, the MAX2870 is a high-performance frequency synthesizer capable of synthesizing frequencies from 23.5MHz to 6.0GHz while maintaining superior phase noise and spurious performance. The ultra-wide frequency range is achieved with the help of multiple integrated VCOs covering 3000MHz to 6000MHz, and output dividers ranging from 1 to 128. The device also provides dual differential output drivers, which can be independently programmable to deliver -4dBm to +5dBm output power. Both outputs can be muted by either software or hardware control. The MAX2870 is controlled by a 3-wire serial interface and is compatible with 1.8V control logic. The device is available in a lead-free, RoHS-compliant, 5mm x 5mm, 32-pin TQFN package, and operates over an extended -40°C to +85°C temperature range.

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II. Manufacturing Information

A. Description/Function:	23.5MHz to 6000MHz Fractional/Integer-N Synthesizer/VCO
B. Process:	MB3
C. Number of Device Transistors:	58954
D. Fabrication Location:	USA
E. Assembly Location:	China, Taiwan and Thailand
F. Date of Initial Production:	March 30, 2012

III. Packaging Information

A. Package Type:	32-pin TQFN 5x5
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4465
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	47°C/W
K. Single Layer Theta Jc:	1.7°C/W
L. Multi Layer Theta Ja:	29°C/W
M. Multi Layer Theta Jc:	2.7°C/W

IV. Die Information

A. Dimensions:	100.00 X 90.94 mils
B. Passivation:	BCB
C. Interconnect:	Al with top layer 100% Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.23 microns as drawn
F. Minimum Metal Spacing:	0.23 microns as drawn
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 13.7 \times 10^{-9}$

λ = 13.7 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim Integrated's reliability monitor program. Maxim Integrated performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maximintegrated.com/qa/reliability/monitor. Cumulative monitor data for the MB3 Process results in a FIT Rate of 0.08 @ 25C and 1.33 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SADK2Q002B, D/C 1207)

The WV29 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

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Table 1
Reliability Evaluation Test Results

MAX2870ETJ+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	0	SADK2Q002B, D/C 1207

Note 1: Life Test Data may represent plastic DIP qualification lots.

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