

RELIABILITY REPORT FOR MAX3108EWA+ WAFER LEVEL PRODUCT

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MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR. SUNNYVALE, CA 94086

Approved by			
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Quality Assurance			
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Conclusion

The MAX3108EWA+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX3108 small form factor universal asynchronous receiver-transmitter (UART) with 128 words each of receive and transmit FIFOs is controlled through a serial I²C or SPI(tm) controller interface. Auto-sleep and shutdown modes help reduce power consumption during periods of inactivity. A low 500µA (max) supply current and tiny 25-bump WLP (2.1mm x 2.1mm) package make the MAX3108 ideal for low-power portable devices. The MAX3108 operates from a low supply voltage of 1.71V to 3.6V. Baud rates up to 24Mbps make the MAX3108 suitable for todayâ€[™]s high data rate applications. A phase-locked loop (PLL), predivider, and fractional baud-rate generator allow high-resolution baud-rate programming and minimize the dependency of baud rate on reference clock frequency. Four GPIOs can be used as inputs, outputs, or interrupt inputs. When configured as outputs, they can be programmed to be open-drain outputs and sink up to 20mA of current. The MAX3108 is ideal for portable and handheld devices, is available in a 25-bump (2.1mm x 2.1mm) 0.4mm pitch WLP package, and is specified over the -40°C to +85°C extended temperature range.



II. Manufacturing Information

A. Description/Function:SPI/I²C UART with 128-Word FIFOs in WLPB. Process:TS18C. Number of Device Transistors:265000D. Fabrication Location:TaiwanE. Assembly Location:JapanF. Date of Initial Production:December 22, 2010

III. Packaging Information

A. Package Type:	25-bump WLP 5x5 array
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-4248 / A
H. Flammability Rating:	Class UL94-V0
 Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C 	1
J. Single Layer Theta Ja:	N/A°C/W
K. Single Layer Theta Jc:	N/A°C/W
L. Multi Layer Theta Ja:	52°C/W
M. Multi Layer Theta Jc:	N/A°C/W

IV. Die Information

A. Dimensions:	84.25 X 84.25 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18µm
F. Minimum Metal Spacing:	0.18µm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw



/ .	Quality	Assurance	Inf	formation	
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A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Engineering)
	Don Lipps (Manager, Reliability Engineering)
	Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet.0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

 $\lambda = \underbrace{1}_{\text{MTTF}} = \underbrace{1.83}_{\text{192 x 4340 x 48 x 2}} \text{ (Chi square value for MTTF upper limit)}$ $\lambda = 22.9 \text{ x } 10^{-9}$ $\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the TS18 Process results in a FIT Rate of 0.24 @ 25C and 4.14 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot QS1ZBQ001A D/C 1103)

The RU52-1 die type has been found to have all pins able to withstand a HBM transient pulse of +/-2000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA and overvoltage per JEDEC JESD78.



Table 1 Reliability Evaluation Test Results

MAX3108EWA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (N	lote 1) Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	QS1ZBQ001A, D/C 1103

Note 1: Life Test Data may represent plastic DIP qualification lots.