RELIABILITY REPORT

FOR

**MAX3323ExxE**

PLASTIC ENCAPSULATED DEVICES

April 18, 2003

# MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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**Conclusion**

The MAX3323E successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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## I. Device Description

A. General

The MAX3323E 3.0V to 5.5V powered EIA/TIA-232 and V.28/V.24 communications interface is designed for multidrop applications with low power requirements, high data-rate capabilities, and enhanced electrostatic discharge (ESD) protection. All RS-232 inputs and outputs are protected to ±15kV using the IEC 1000-4-2 Air-Gap Discharge method, ±8kV using the IEC 1000-4-2 Contact Discharge method, and ±15kV using the Human Body Model. The MAX3323E has pin-selectable 5kΩ /high-impedance RS-232 receivers. The device ais capable of receiving data in high-impedance mode. In multidrop applications, one receiver has a 5kΩ input resistance, while the other receivers are high impedance to ensure the RS-232 standard is observed. Logic control permits selection of the functional mode: high impedance or RS-232 standard load. The transmitters are enabled by logic control to allow the multiplexing of the inputs to a single UART.

A proprietary low-dropout transmitter output stage enables true RS-232 performance from a 3.0V to 5.5V supply with a dual charge pump. The charge pump requires only four small 0.1µF capacitors for operation from a 3.3V supply. The MAX3323E is capable of running at data rates up to 250kbps while maintaining RS-232-compliant output levels. The MAX3323E has a unique $V_L$ pin that allows operation in mixed-logic voltage systems. Both input and output logic levels are pin programmable through the $V_L$ pin.

The MAX3323E is a 1Tx/1Rx device for hardware handshaking in standard RS-232 mode, required in most multidrop applications. The MAX3323E is offered in 16-pin DIP and space-saving TSSOP packages.

B. Absolute Maximum Ratings

| Item | Rating |
|---|---|
| All Voltages Referenced to GND | |
| VCC, VL | -0.3V to +6V |
| V+ (Note 1) | (VCC - 0.3V) to +7V |
| V- (Note 1) | +0.3V to -7V |
| V+ + \|V-\| (Note 1) | +13V |
| Input Voltages | |
| TIN_, RENABLE, TXENABLE, SHDN | -0.3V to +6V |
| RIN_ | ±25V |
| Output Voltages | |
| TOUT_ | ±13.2V |
| ROUT_ | -0.3V to (VL + 0.3V) |
| Short-Circuit Duration TOUT_ to GND | Continuous |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Continuous Power Dissipation (TA = +70°C) | |
| 16-Pin DIP | 842mW |
| 16-Pin TSSOP | 755mW |
| Derates above +70°C | |
| 16-Pin DIP | 10.5mW/°C |
| 16-Pin TSSOP | 9.4mW/°C |

**Note 1:** V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

## II. Manufacturing Information

| | |
|---|---|
| A. Description/Function: | ±15kV ESD-Protected, RS-232 Transceivers for Multidrop Applications |
| B. Process: | S3 (Standard 3 micron silicon gate CMOS) |
| C. Number of Device Transistors: | 1294 |
| D. Fabrication Location: | Oregon, USA |
| E. Assembly Location: | Philippines, Malaysia or Thailand |
| F. Date of Initial Production: | January, 2002 |

## III. Packaging Information

| | **16-Pin DIP** | **16-Pin TSSOP** |
|---|---|---|
| A. Package Type: | | |
| B. Lead Frame: | Copper | Copper |
| C. Lead Finish: | Solder Plate | Solder Plate |
| D. Die Attach: | Silver-Filled Epoxy | Silver-Filled Epoxy |
| E. Bondwire: | Gold (1 mil dia.) | Gold (1 mil dia.) |
| F. Mold Material: | Epoxy with silica filler | Epoxy with silica filler |
| G. Assembly Diagram: | # 05-9000-0307 | # 05-9000-0309 |
| H. Flammability Rating: | Class UL94-V0 | Class UL94-V0 |
| I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112: | Level 1 | Level 1 |

## IV. Die Information

| | |
|---|---|
| A. Dimensions: | 108 x 144 mils |
| B. Passivation: | $Si_3N_4/SiO_2$ (Silicon nitride/ Silicon dioxide) |
| C. Interconnect: | Aluminum/Si (Si = 1%) |
| D. Backside Metallization: | None |
| E. Minimum Metal Width: | 3 microns (as drawn) |
| F. Minimum Metal Spacing: | 3 microns (as drawn) |
| G. Bondpad Dimensions: | 5 mil. Sq. |
| H. Isolation Dielectric: | $SiO_2$ |
| I. Die Separation Method: | Wafer Saw |

## V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 45 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 24.13 \times 10^{-9}$

$\lambda = 24.13$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-6076) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The RT55-1 die type has been found to have all pins able to withstand a transient pulse of ±1000V per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

**Table 1**
Reliability Evaluation Test Results

**MAX3323ExxE**

| TEST ITEM | TEST CONDITION | FAILURE IDENTIFICATION | PACKAGE | SAMPLE SIZE | NUMBER OF FAILURES |
|---|---|---|---|---|---|
| **Static Life Test** (Note 1) | | | | | |
| | Ta = 135°C<br>Biased<br>Time = 192 hrs. | DC Parameters<br>& functionality | | 45 | 0 |
| **Moisture Testing** (Note 2) | | | | | |
| Pressure Pot | Ta = 121°C<br>P = 15 psi.<br>RH= 100%<br>Time = 168hrs. | DC Parameters<br>& functionality | TSSOP<br>DIP | 77<br>77 | 0<br>0 |
| 85/85 | Ta = 85°C<br>RH = 85%<br>Biased<br>Time = 1000hrs. | DC Parameters<br>& functionality | | 77 | 0 |
| **Mechanical Stress** (Note 2) | | | | | |
| Temperature Cycle | -65°C/150°C<br>1000 Cycles<br>Method 1010 | DC Parameters | | 77 | 0 |

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data

**Attachment #1**

TABLE II. Pin combination to be tested. 1/ 2/

| | Terminal A (Each pin individually connected to terminal A with the other floating) | Terminal B (The common combination of all like-named pins connected to terminal B) |
|---|---|---|
| 1. | All pins except $V_{PS1}$ 3/ | All $V_{PS1}$ pins |
| 2. | All input and output pins | All other input-output pins |

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

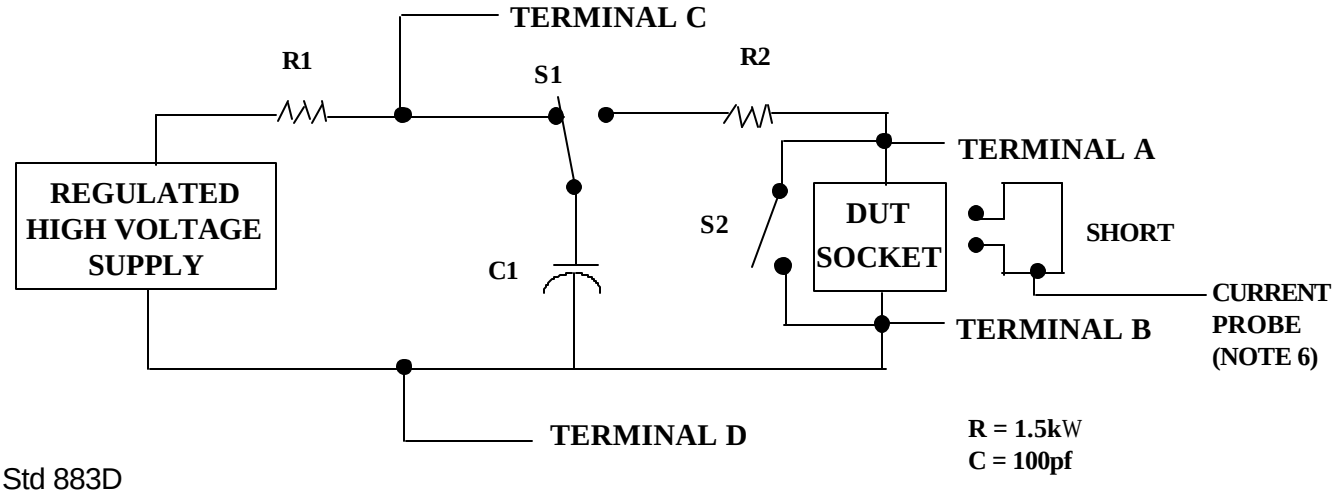
(e.g., where $V_{PS1}$ is $V_{DD}$, $V_{CC}$, $V_{SS}$, $V_{BB}$, GND, $+V_S$, $-V_S$, $V_{REF}$, etc).

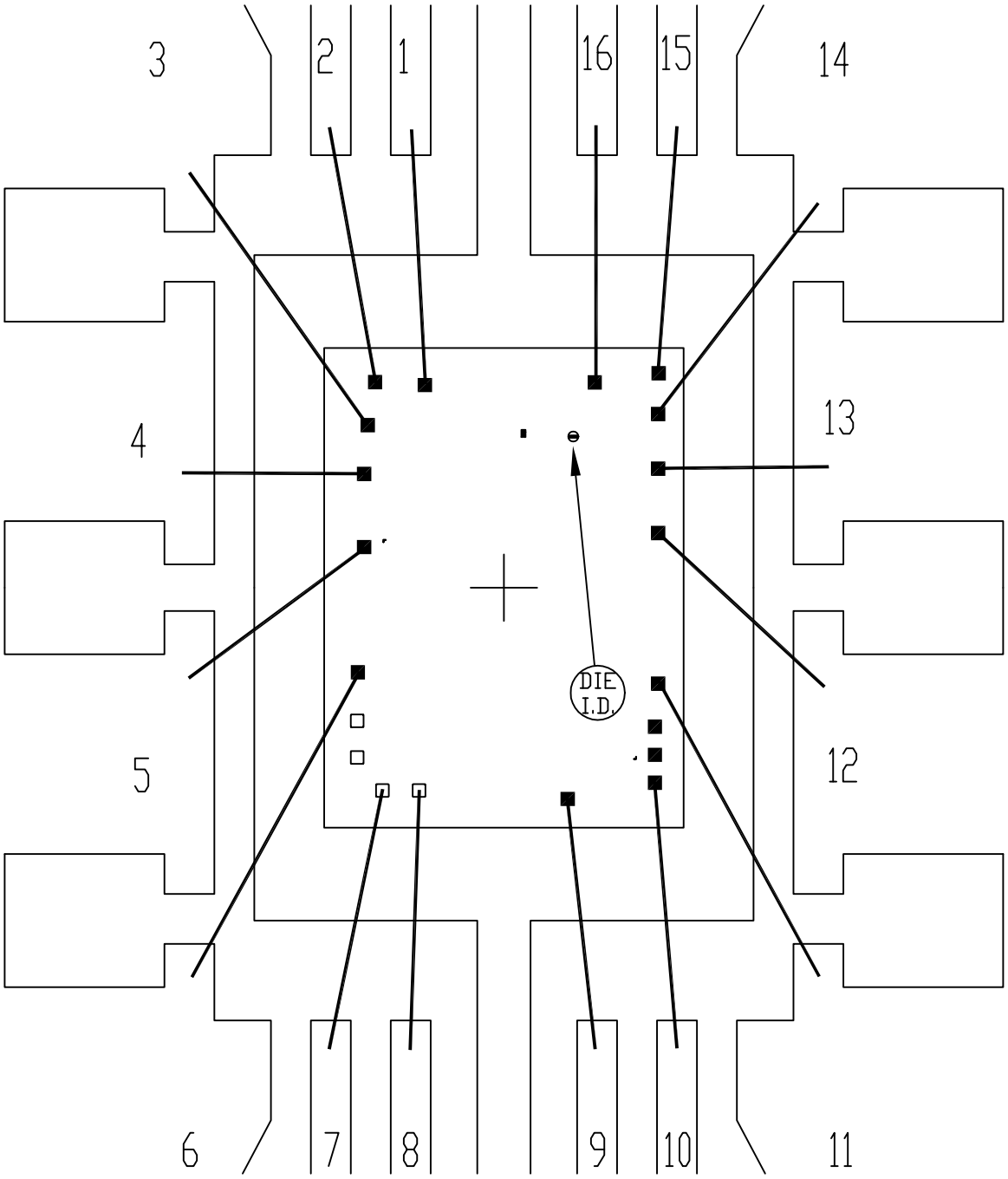
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

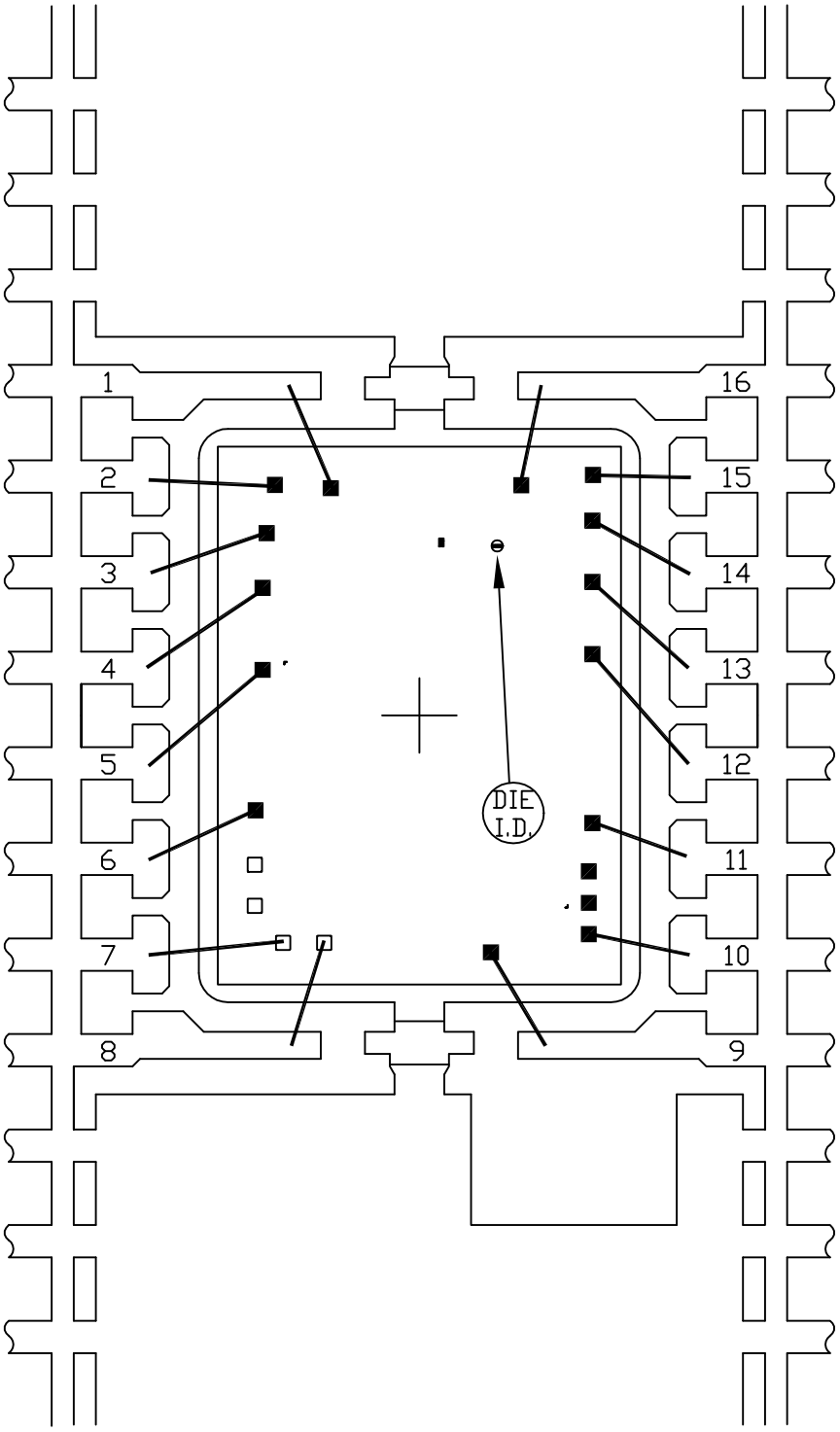
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., $V_{SS1}$, or $V_{SS2}$ or $V_{SS3}$ or $V_{CC1}$, or $V_{CC2}$) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





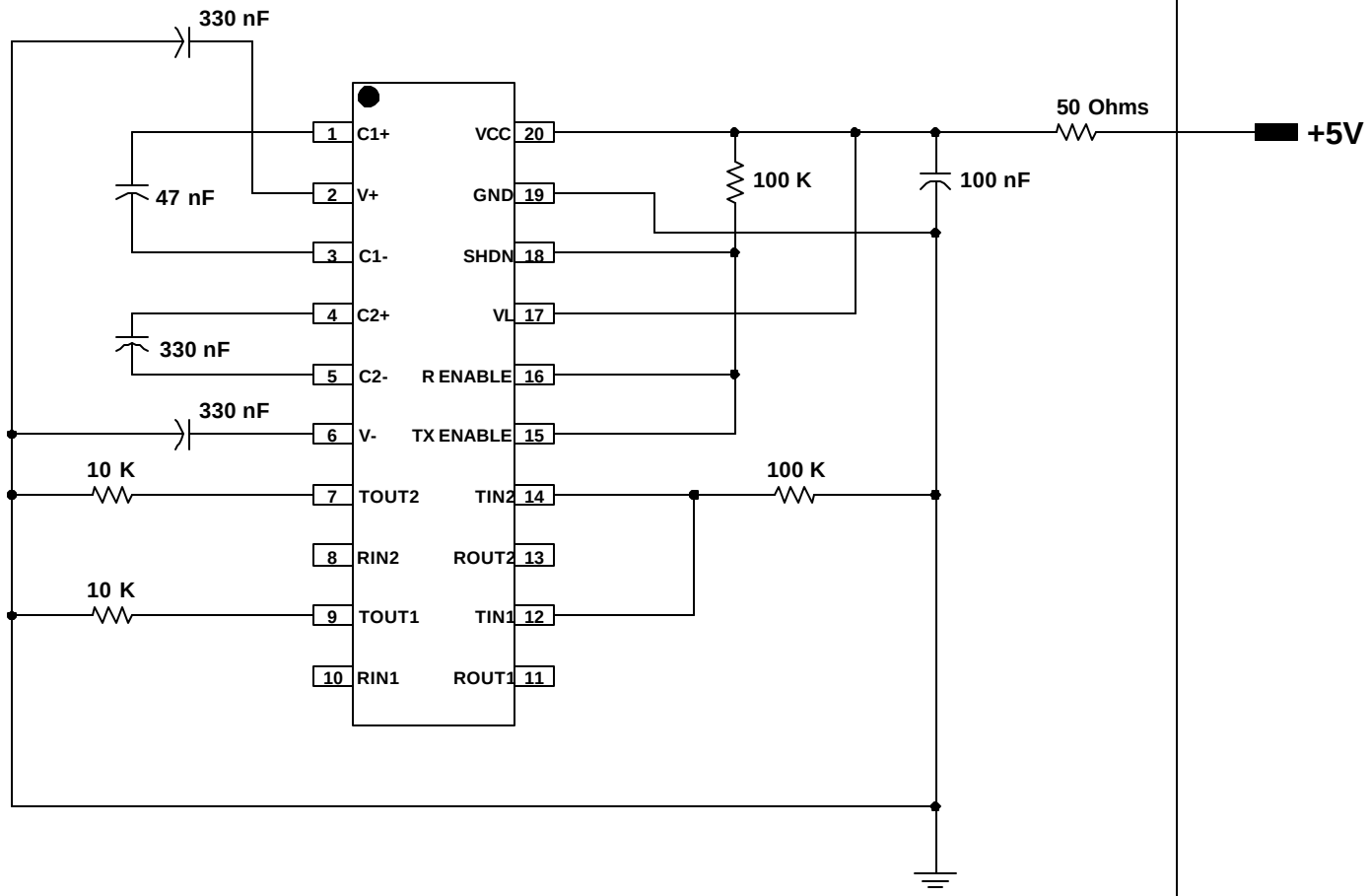

| PKG. CODE: P16-3 | | SIGNATURES | DATE | MAXIM CONFIDENTIAL & PROPRIETARY | |
|---|---|---|---|---|---|
| CAV./PAD SIZE: 150x200 | PKG. | | | BOND DIAGRAM #: 05-9000-0307 | REV: A |
| | DESIGN | | | | |




| PKG. CODE: U16-1 | | SIGNATURES | DATE | MAXIM CONFIDENTIAL & PROPRIETARY | |
|---|---|---|---|---|---|
| CAV./PAD SIZE: 118X154 | PKG. | | | BOND DIAGRAM #: 05-9000-0309 | REV: A |
| | DESIGN | | | | |

## ONCE PER SOCKET

## ONCE PER BOARD




**DEVICES: MAX 3322E (RT55Z)**
**PACKAGE: 20-TSSOP**
**MAX. EXPECTED CURRENT = 10mA**

**DRAWN BY: TEK TAN**
**NOTES:**