RELIABILITY REPORT

FOR

MAX3421EETJ+T / MAX3421EEHJ+T

PLASTIC ENCAPSULATED DEVICES

May 7, 2012

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Quality Assurance
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Conclusion

      The MAX3421EETJ+T / MAX3421EEHJ+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

      A. General

The MAX3421E USB peripheral/host controller contains the digital logic and analog circuitry necessary to implement a full-speed USB peripheral or a full-/low-speed host compliant to USB specification rev 2.0. A built-in transceiver features ±15kV ESD protection and programmable USB connect and disconnect. An internal serial interface engine (SIE) handles low-level USB protocol details such as error checking and bus retries. The MAX3421E operates using a register set accessed by an SPI(tm) interface that operates up to 26MHz. Any SPI master (microprocessor, ASIC, DSP, etc.) can add USB peripheral or host functionality using the simple 3- or 4-wire SPI interface. The MAX3421E makes the vast collection of USB peripherals available to any microprocessor, ASIC, or DSP when it operates as a USB host. For point-to-point solutions, for example, a USB keyboard or mouse interfaced to an embedded system, the firmware that operates the MAX3421E can be simple since only a targeted device is supported. Internal level translators allow the SPI interface to run at a system voltage between 1.4V and 3.6V. USB-timed operations are done inside the MAX3421E with interrupts provided at completion so an SPI master does not need timers to meet USB timing requirements. The MAX3421E includes eight general-purpose inputs and outputs so any microprocessor that uses I/O pins to implement the SPI interface can reclaim the I/O pins and gain additional ones. The MAX3421E operates over the extended -40°C to +85°C temperature range and is available in a 32-pin TQFP package (5mm x 5mm) and a 32-pin TQFN package (5mm x 5mm).

II. Manufacturing Information

A. Description/Function:	USB Peripheral/Host Controller with SPI Interface	
B. Process:	S4	
C. Number of Device Transistors:	101471	
D. Fabrication Location:	USA	
E. Assembly Location:	China, Malaysia, Taiwan and Thailand	Philippines
F. Date of Initial Production:	January 21, 2006	

III. Packaging Information

A. Package Type:	32-pin TQFN 5x5	32-pin TQFP
B. Lead Frame:	Copper	Copper
C. Lead Finish:	100% matte Tin	100% matte Tin
D. Die Attach:	Conductive	Conductive
E. Bondwire:	Au (1 mil dia.)	Au (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-2001	#05-9000-2002
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1	Level 1
J. Single Layer Theta Ja:	47°C/W	
K. Single Layer Theta Jc:	1.7°C/W	
L. Multi Layer Theta Ja:	29°C/W	76.4°C/W
M. Multi Layer Theta Jc:	1.7°C/W	19°C/W

IV. Die Information

A. Dimensions:	105 X 105 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/0.5%Cu with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1 = 0.5 / Metal2 = 0.6 / Metal3 = 0.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1 = 0.45 / Metal2 = 0.5 / Metal3 = 0.6 microns (as drawn)
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

    A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
                                                    Don Lipps (Manager, Reliability Engineering)
                                                      Bryan Preeshl (Vice President of QA)

    B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
                                                        0.1% For all Visual Defects.

    C. Observed Outgoing Defect Rate: < 50 ppm

    D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

    A. Accelerated Life Test

        The results of the 135C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 49 \times 2} \quad \text{(Chi square value for MTTF upper limit)}$$

                  (where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$

$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

        The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the S4 Process results in a FIT Rate of 0.06 @ 25C and 1.00 @ 55C (0.8 eV, 60% UCL)

    B. E.S.D. and Latch-Up Testing (lot TZJ0DQ002D, D/C 0852)

        The RT53 die type has been found to have all pins able to withstand a HBM transient pulse of +/- 2500V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX3421EETJ+T / MAX3421EEHJ+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	TZJ0DQ002D, D/C 0852

Note 1: Life Test Data may represent plastic DIP qualification lots.