RELIABILITY REPORT

FOR

MAX3800UxJ

PLASTIC ENCAPSULATED DEVICES

April 29, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX3800 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX3800 is a +3.3V adaptive cable equalizer and cable driver implemented together on a single chip. It is designed for coaxial and twin-axial cable point-to-point communications applications. The driver features differential current-mode logic (CML) inputs and outputs as well as adjustable output amplitude. The equalizer includes differential CML data inputs and outputs, a loss-of-signal (LOS-bar) output, and a cable integrity monitor (CIM) output.

The adaptive cable equalizer is capable of equalizing differential or single-ended signals at data rates up to 3.2Gbps. It automatically adjusts to attenuation caused by skin-effect losses of up to 30dB at 1.6GHz. The equalizer effectively extends the usable length of copper cable in high-frequency interconnect applications.

The MAX3800 is available in a 32-pin TQFP package with exposed pad and consumes only 200mW at +3.3V. The driver can be disconnected from the power supply when it is not needed, resulting in a 40% reduction in supply current.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage (V_{CC} to GND)	-0.5V to +6V
Voltage at /LOS,CIM,RMOD	-0.5V to (VCC +0.5V)
Voltage at EIN+,EIN-,DIN+,DIN-	(VCC - 1V) to (VCC + 0.5V)
Current Out of EOT+,EOUT-,DOUT+,DOUT-	25mA
Storage Temp.	-55°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continuous Power Dissipation (TA =+85°C)	
32-Pin QFN	1.44W
Derates above +85°C	
32-Pin QFN	44.8mW/°C

II. Manufacturing Information

A. Description/Function:	3.2Gbps Adaptive Equalizer
B. Process:	GST33
C. Number of Device Transistors:	1252
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Korea or Philippines
F. Date of Initial Production:	January, 2002

III. Packaging Information

	32-Pin QFN	**32-Pin TQFP**
A. Package Type:		
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.2 mil dia.)	Gold (1.2 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-7001-0557	Buildsheet # 05-7001-0480
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 3	Level 3

IV. Die Information

A. Dimensions:	81 x 81 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride)
C. Interconnect:	Poly / Au
D. Backside Metallization:	None
E. Minimum Metal Width:	Metal1: 1.2; Metal2: 1.2; Metal3: 2.8; Metal4: 5.6 microns (as drawn)
F. Minimum Metal Spacing:	Metal1: 1.3; Metal2: 1.4; Metal3: 2.6; Metal4: 2.6 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 150°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 9823 \times 42 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 11.55 \times 10^{-8}$ $\lambda = 11.55$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The HF66 die type has been found to have all pins able to withstand a transient pulse of ± 500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX3800UxJ

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 150°C Biased Time = 192 hrs.	DC Parameters & functionality		42	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	QFN TQFP	77 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

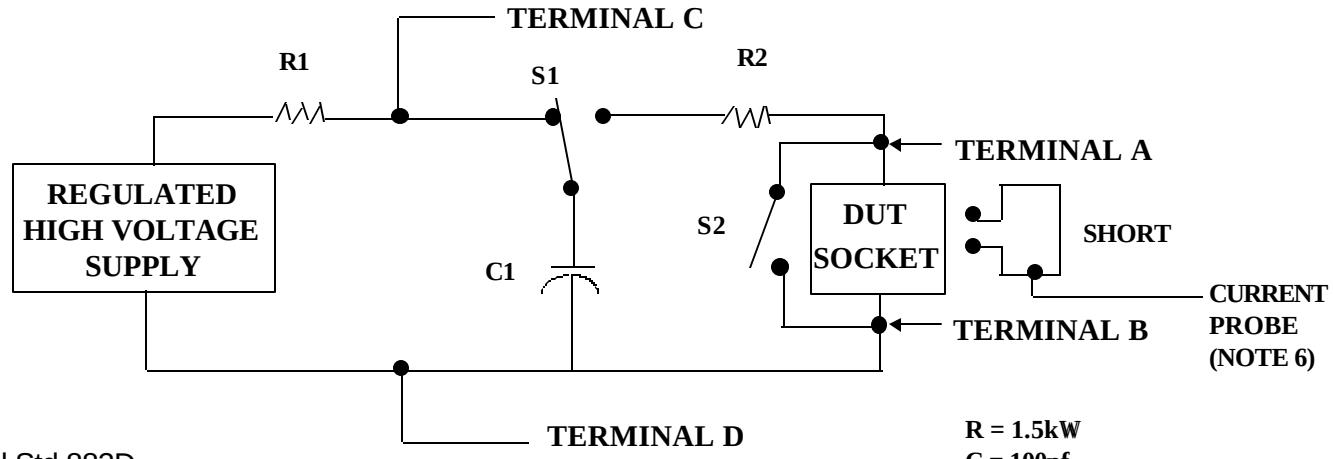
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

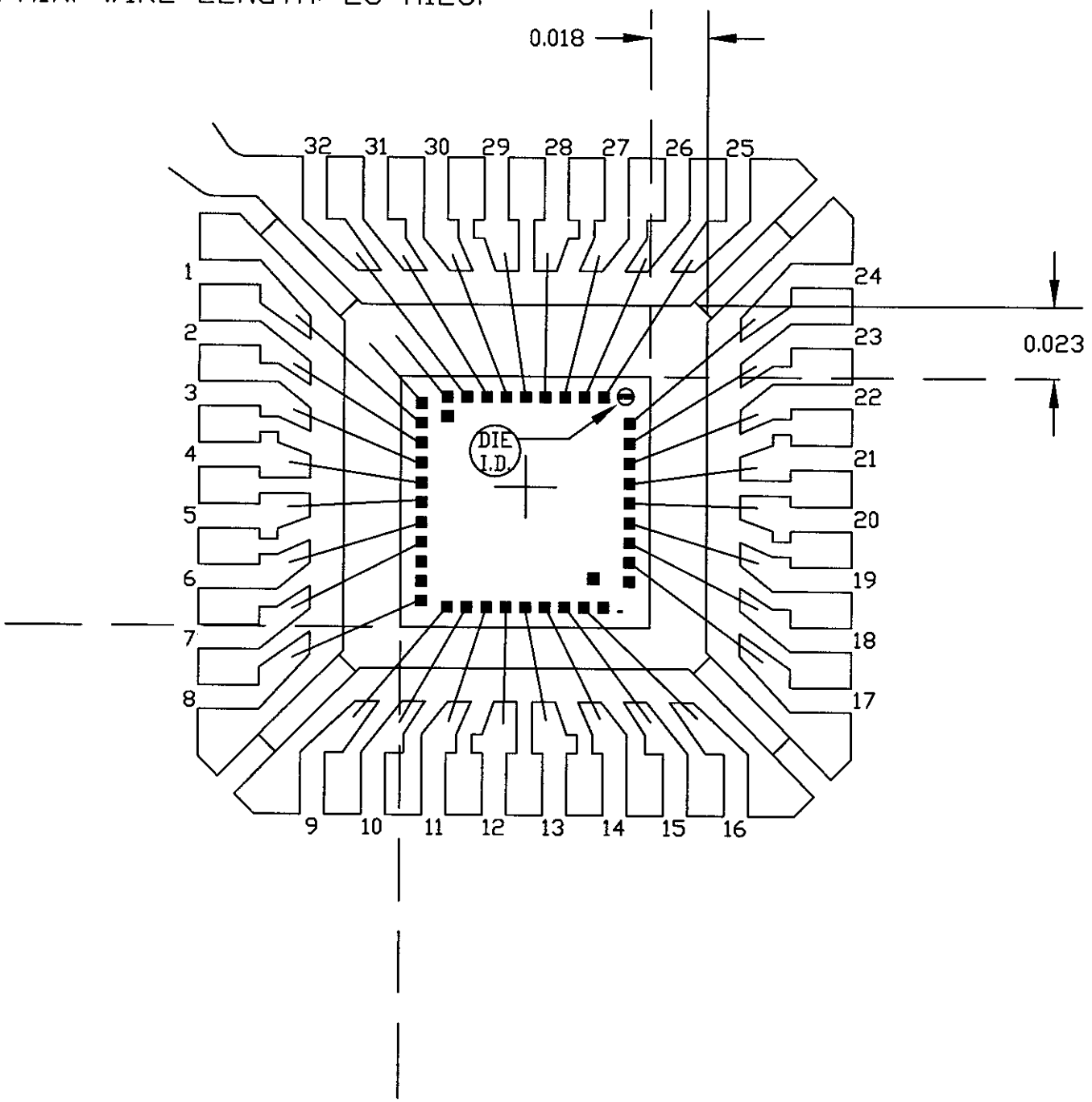
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



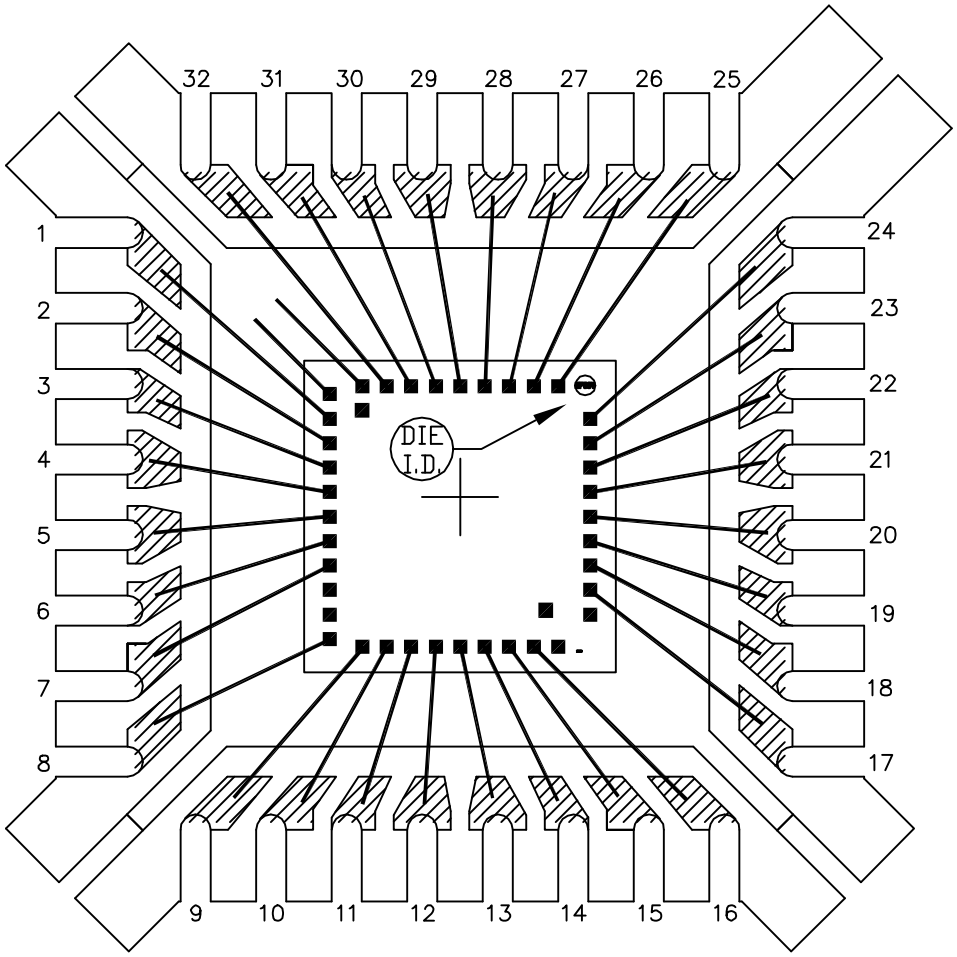
Mil Std 883D
Method 3015.7
Notice 8

NOTES:
1. MAX. DIE SIZE: 108x108
2. MIN. WIRE LENGTH: 25 MILS.



PKG.CODE: H32E-5		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 118x118	PKG. DESIGN			BUILDSHEET NUMBER: 05-7001-0480 / REV.: A

EXPOSED PAD PKG.



BONDABLE AREA

PKG. BODY SIZE: 5x5 mm

PKG. CODE: G3255-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 130x130	PKG.			BOND DIAGRAM #: 05-7001-0557	REV: A
	DESIGN				